LM3370 Dual Synchronous Step-Down DC-DC Converter with Dynamic Voltage Scaling Function

Check for Samples: LM3370

FEATURES

- **I²C-compatible interface**
  - **V_{OUT1} = 1V to 2V in 50 mV Steps**
  - **V_{OUT2} = 1.8V to 3.3V in 100 mV Steps**
  - **Automatic PFM/PWM Mode Switching and Forced PWM Mode for Low Noise Operation**
  - **Spread Spectrum Capability Using I²C**
- **600mA Load Per Channel**
- **2MHz PWM Fixed Switching Frequency (Typ.)**
- **The Bucks Operate 180° Out-of-Phase Timing Offset for Noise and Input Surge Current Abatement**
- **Internal Synchronous Rectification for High Efficiency**
- **Internal Soft Start**
- **Power-on-Reset Function for Both Outputs**
- **2.7V ≤ V_{IN} ≤ 5.5V**
- **Operates from a Single Li-Ion Cell or 3 Cell NiMH/NiCd Batteries and 3.3V/5.5V Fixed Rails**
- **2.2µH Inductor, 4.7µF Input and 10µF Output Capacitor Per Channel**
- **16-lead WSON Package (4 mm x 5 mm x 0.8 mm)**
- **20-Bump DSBGA Package (3.0 mm x 2.0 mm x 0.6 mm)**

APPLICATIONS

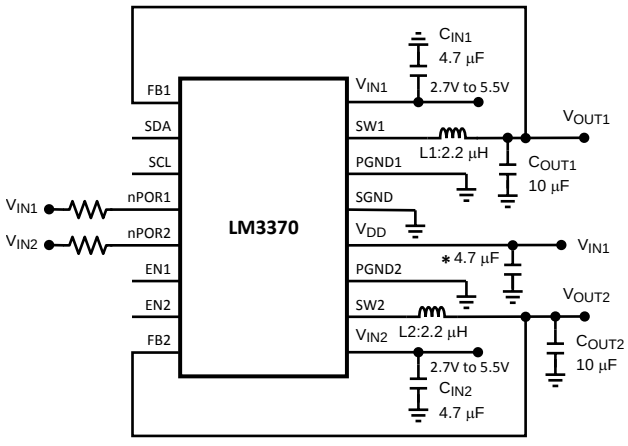
- **Baseband Processors**
- **Application Processors (Video, Audio)**
- **I/O Power**
- **FPGA Power and CPLD**

DESCRIPTION

The LM3370 is a dual step-down DC-DC converter optimized for powering ultra-low voltage circuits from a single Li-Ion battery and input rail ranging from 2.7V to 5.5V. It provides two outputs with 600mA load per channel. The output voltage range varies from 1V to 3.3V and can be dynamically controlled using the I²C-compatible interface. This dynamic voltage scaling function allows processors to achieve maximum performance at the lowest power level. The I²C-compatible interface can also be used to control auto PFM-PWM/PWM mode selection and other performance enhancing features.

The LM3370 offers superior features and performance for portable systems with complex power management requirements. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system efficiency. Internal synchronous rectification enhances the converter efficiency without the use of further external devices.

Typical Application Circuit



∗ Optional Capacitor

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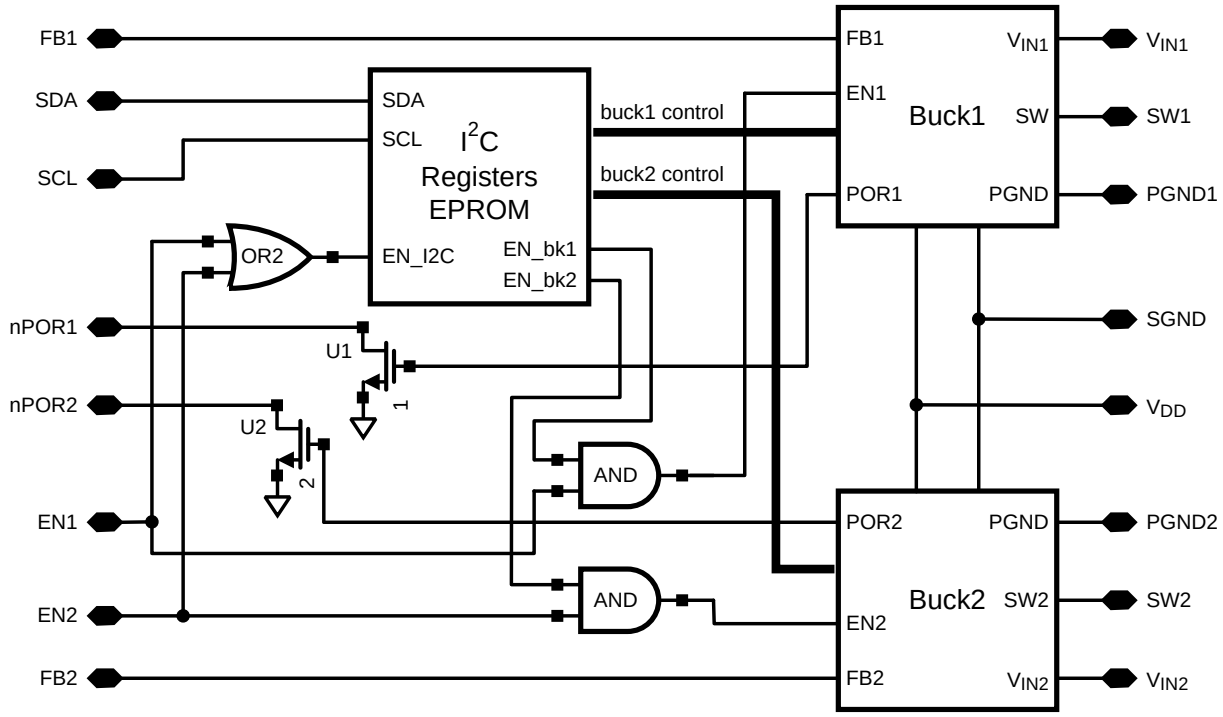
DESCRIPTION (CONTINUED)

There is a power-on-reset function that monitors the level of the output voltage to avoid unexpected power losses. The independent enable pin for each output allows for simple and effective power sequencing.

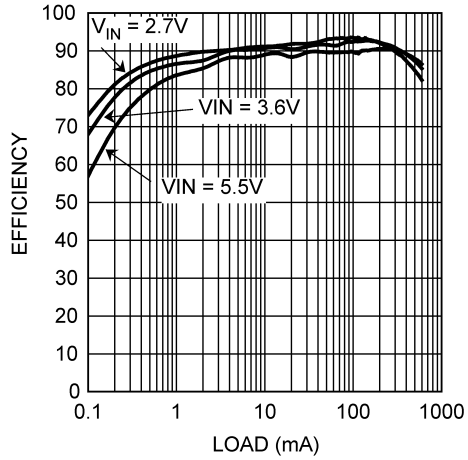
LM3370 is available in a 4mm by 5mm 16-lead non-pullback WSON and a 20-bump DSBGA, 3.0mm x 2.0mm x 0.6mm, package. A high switching frequency—2 MHz (typ)—allows use of tiny surface-mount components including a 2.2µH inductor.

Default fixed voltages for the 2 output voltages combination can be customized to fit system requirements by contacting Texas Instruments.

Functional Block Diagram



Typical Performance Curve



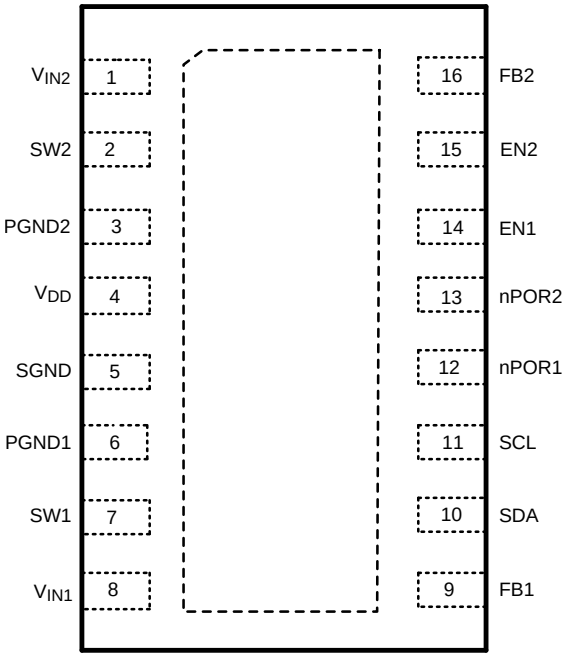


Figure 1. WSON Connection Diagram
(See Package Number NHR0016B)

PIN DESCRIPTIONS (WSON)

Pin #	Name	Description
1	V_{IN2}	Power supply voltage input to PFET and NFET switches for Buck 2
2	SW2	Buck 2 Switch Pin
3	PGND2	Buck 2 Power Ground
4	V_{DD}	Signal supply voltage input, V_{DD} must be equal or greater of the two inputs (V_{IN1} and V_{IN2})
5	SGND	Signal GND
6	PGND1	Buck 1 Power Ground
7	SW1	Buck 1 Switch Pin
8	V_{IN1}	Power supply voltage input to PFET and NFET switches for Buck 1
9	FB1	Analog Feedback Input for Buck 1
10	SDA	I^2C-Compatible Data, a 2 kΩ pull up resistor is required
11	SCL	I^2C-Compatible Clock, a 2 kΩ pull up resistor is required
12	nPOR1	Power ON Reset for Buck 1, Open drain output Low when Buck 1 output is 92% of target output. A 100 kΩ pull up resistor is required
13	nPOR2	Power ON Reset for Buck 2, Open drain output Low when Buck 2 output is 92% of target output. A 100 kΩ pull up resistor is required
14	EN1	Buck 1 Enable
15	EN2	Buck 2 Enable
16	FB2	Analog feedback for Buck 2

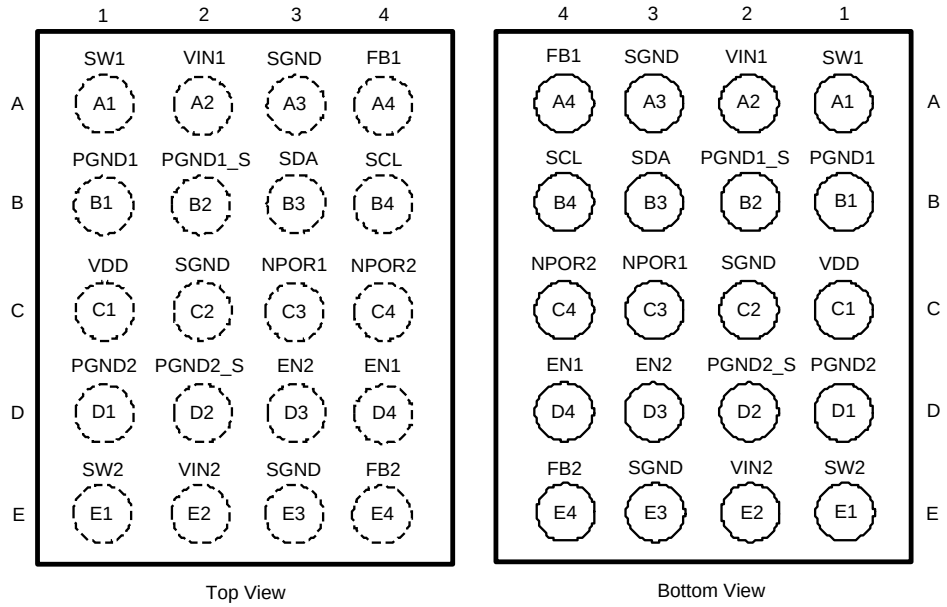


Figure 2. DSBGA Connection Diagram
(See Package Number YZR0020DWA)

PIN DESCRIPTIONS (DSBGA)

Pin #	Name	Description
A1	SW1	Buck 1 Switch Pin
A2	V_{IN1}	Power supply voltage input to PFET and NFET switches for Buck 1
A3	SGND	Signal GND
A4	FB1	Analog Feedback Input for Buck 1
B1	PGND1	Buck 1 Power Ground
B2	PGND1_S	Buck 1 Power Ground Sense
B3	SDA	I^2C-Compatible Data, a 2 kΩ pullup resistor is required
B4	SCL	I^2C-Compatible Clock, a 2 kΩ pullup resistor is required
C1	V_{DD}	Signal supply voltage input, V_{DD} must be equal or greater of the two inputs (V_{IN1} and V_{IN2})
C2	SGND	Signal GND
C3	nPOR1	Power ON Reset for Buck 1, Open drain output Low when Buck 1 output is 92% of target output. A 100 kΩ pullup resistor is required
C4	nPOR2	Power ON Reset for Buck 2, Open drain output Low when Buck 2 output is 92% of target output. A 100 kΩ pullup resistor is required
D1	PGND2	Buck 2 Power Ground
D2	PGND2_S	Buck 2 Power Ground Sense
D3	EN2	Buck 2 Enable
D4	EN1	Buck 1 Enable
E1	SW2	Buck 2 Switch Pin
E2	V_{IN2}	Power supply voltage input to PFET and NFET switches for Buck 2
E3	SGND	Signal GND
E4	FB2	Analog feedback for Buck 2

I²C Controlled Features

Features	Parameter	Comments
Output Voltage	V_{OUT1} and V_{OUT2}	Output voltage is controlled via I²C-compatible
Modes	Buck 1 and Buck 2	Mode can be controlled via I²C compatible by either forcing device in Auto mode or forced PWM mode
Spread Spectrum	Buck 1 and Buck 2	Spread Spectrum capability via I²C-compatible for noise reduction

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)(2)

Ordering Information	Voltage Option (V)
LM3370 (WSON)	
LM3370SD-3013	1.2 and 2.5
LM3370SDX-3013	
LM3370SD-3021	1.2 and 3.3
LM3370SDX-3021	
LM3370SD-3416	1.4 and 2.8
LM3370SDX-3416	
LM3370SD-3621	1.5 and 3.3
LM3370SDX-3621	
LM3370SD-3806	1.6 and 1.8
LM3370SDX-3806	
LM3370SD-4221	1.8 and 3.3
LM3370SDX-4221	
LM3370 (DSBGA)	
LM3370TL-2613/NOPB	1.0 and 2.5
LM3370TLX-2613/NOPB	
LM3370TL-3607/NOPB	1.5 and 1.9
LM3370TLX-3607/NOPB	
LM3370TL-3008/NOPB	1.2 and 2.0
LM3370TLX-3008/NOPB	
LM3370TL-3006/NOPB	1.2 and 1.8
LM3370TLX-3006/NOPB	
LM3370TL-3806/NOPB	1.6 and 1.8
LM3370TLX-3806/NOPB	
LM3370TL-3206/NOPB	1.3 and 1.8
LM3370TLX-3206/NOPB	
LM3370TL-3022/NOPB	1.2 and 1.85
LM3370TLX-3022/NOPB	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Absolute Maximum Ratings[1][2][3]

V_{IN1} , V_{IN2} VDD to PGND and SGND		−0.2V to 6V
PGND to SGND		−0.2V to +0.2V
SDA, SCL, EN, EN2, nPOR1, nPOR2, SW1, SW2, FB1 and FB2		(GND - 0.2) to (V_{IN} + 0.2V)
Maximum Continuous Power Dissipation (P_{D_MAX}) [4]		Internally Limited
Junction Temperature (T_{J-MAX})		125°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering)		[5]
ESD Ratings [6]	All Pins	2 kV HBM 200V MM

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see Electrical Characteristics.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. The thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 140°C(typ.).
(5) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1187: Leadless Leadframe Package (LLP) (SNOA401).
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin. (EAIJ)

Operating Ratings[1][2]

Input Voltage Range ([3])	2.7V to 5.5V
Recommended Load Current Per Channel	0 mA to 600 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range [4]	−30°C to +85°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see Electrical Characteristics.
(2) All voltages are with respect to the potential at the GND pin.
(3) Input voltage range for all voltage options is 2.7V to 5.5V. The voltage range recommended for the specified output voltages: V_{IN} = 2.7V to 5.5V for 1V ≤ V_{OUT} ≤ 1.7V and for V_{OUT} = 1.8V or greater, V_{IN} = V_{OUT} + 1VorV$_{IN,MIN}$ = I_{LOAD} * (R_{DSON_PFET} + $R_{DCR\_INDUCTOR}$) + V_{OUT}
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties(1)

Junction-to-Ambient Thermal Resistance θ_{JA} (WSON-16)	26°C/W
θ_{JA} (20-Bump DSBGA)	50°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2 x 1 array of thermal vias. Thickness of copper layers are 2/1/1/2oz. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to *Application Note 1187: Leadless Leadframe Package (LLP)* (SNOA401).

Electrical Characteristics(1)(2)(3)

Typical limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the entire junction temperature range (T_A = T_J = −30°C to +85°C). Unless otherwise noted, V_{IN1} = V_{IN2} = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	(4)	**−3.5**		**+3.5**	%
V_{OUT}	Line Regulation	2.7V ≤ V_{IN} ≤ 5.5V I_O = 10 mA, V_{OUT} = 1.8V		0.031		%/V
	Load Regulation	100 mA ≤ I_O ≤ 600 mA V_{IN} = 3.6V, V_{OUT} = 1.8V		0.0013		%/mA
I_Q PFM	Quiescent Current “On”	PFM Mode, Both Bucks ON		34		µA
I_Q SD	Quiescent Current “Off”	EN1 = EN2 = 0V		0.2	**3**	µA
I_{LIM}	Peak Switching Current Limit	V_{IN} = 3.6V	**850**	1200	**1400**	mA
R_{DS_ON} (WSON)	PFET	V_{IN} = 3.6V, I_{SW} = 200 mA		390	500	mΩ
	NFET	V_{IN} = 3.6V, I_{SW} = 200 mA		240	350	
R_{DS_ON} (DSBGA)	PFET	V_{IN} = 3.6V, I_{SW} = 200 mA		350	400	mΩ
	NFET	V_{IN} = 3.6V, I_{SW} = 200 mA		170	210	
F_{OSC}	Internal Oscillator Frequency		**1.5**	2.0	**2.4**	MHz
I_{EN}	Enable (EN) Input Current			0.01	**1**	µA
V_{IL}	Enable Logic Low				**0.4**	V
V_{IH}	Enable Logic High		**1.0**			V
POWER ON RESET THRESHOLD/FUNCTION (POR)						
nPOR1 and nPOR2 Delay Time	nPOR1 = Power ON Reset for Buck 1	50 mS (default)		50		mS
	nPOR2 = Power ON Reset for Buck 2	Can be pre-trimmd to 50 uS, 100 mS and 200 mS				
POR Threshold	Percentage of Target V_{OUT}	V_{OUT} Rising		94		%
		V_{OUT} Falling, 85% (default), Can be pre-trimmed to 70% or 94%		85		

(1) All voltages are with respect to the potential at the GND pin.
(2) Min. and Max are specified by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Input voltage range for all voltage options is 2.7V to 5.5V. The voltage range recommended for the specified output voltages: V_{IN} = 2.7V to 5.5V for 1V ≤ V_{OUT} ≤ 1.7V and for V_{OUT} = 1.8V or greater, V_{IN} = V_{OUT} + 1VorV$_{IN,MIN}$ = I_{LOAD} * (R_{DSON_PFET} + $R_{DCR\_INDUCTOR}$) + V_{OUT}
(4) Test condition: for V_{OUT} less than 2.5V, V_{IN} = 3.6V; for V_{OUT} greater than or equal to 2.5V, V_{IN} = V_{OUT} + 1V.

Dissipation Rating Table

θ_{JA}	T_A = 60°C Power Rating	T_A = 85°C Power Rating
26°C/W (4-Layer Board) WSON-16		1538 mW
50°C/W (4-Layer Board) 20-bump DSBGA	1300 mW	800 mW

Typical Performance Characteristics

LM3370, Circuit of Typical Application Circuit, V_{IN} = 3.6V, V_{OUT1} = 1.5V and V_{OUT2} = 2.5V, L = 2.2 µH (NR3015T2R2M), C_{IN} = 4.7 µF (0805) and C_{OUT} = 10 µF (0805) and T_A = 25°C, unless otherwise noted.

IQ_PFM (Non Switching)
Both Channels

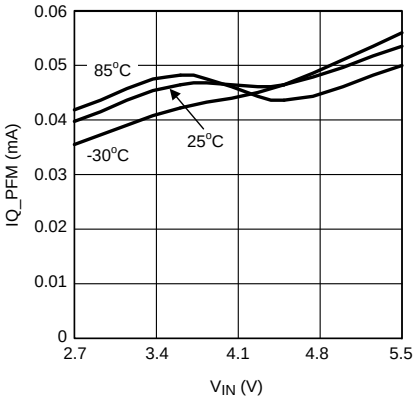


Figure 3.

IQ_PWM (Non Switching)
Both Channels

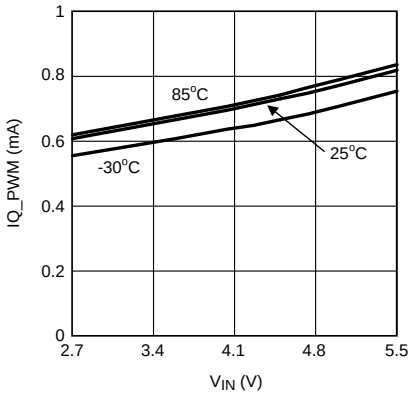


Figure 4.

IQ_PWM (Switching)
Both Channels

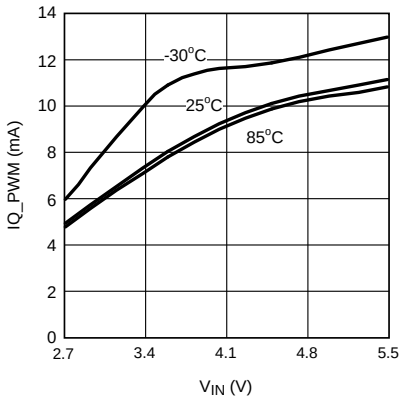


Figure 5.

IQ_SD (EN1 = EN2 = 0V)

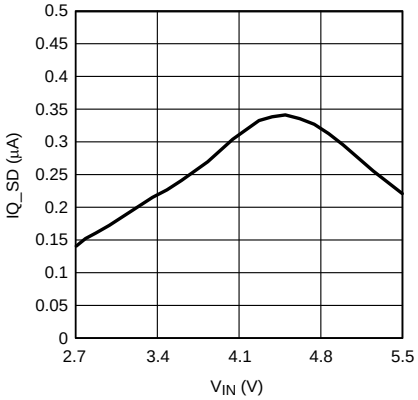


Figure 6.

R_{DS_ON} (PFET)
vs.
Temperature
V_{IN} = 3.6V

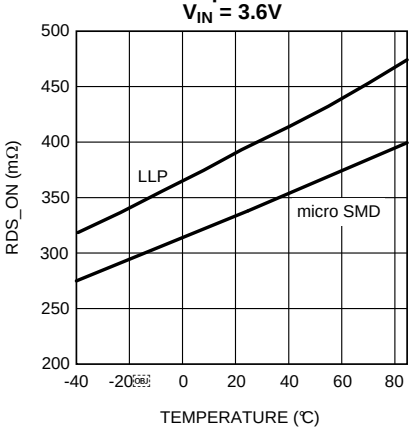


Figure 7.

R_{DS_ON} (NFET)
vs.
Temperature
V_{IN} = 3.6V

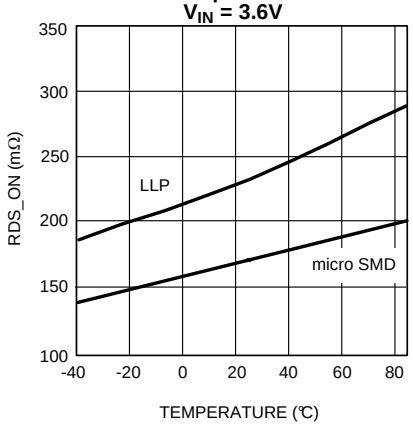


Figure 8.

Typical Performance Characteristics (continued)

LM3370, Circuit of Typical Application Circuit, V_{IN} = 3.6V, V_{OUT1} = 1.5V and V_{OUT2} = 2.5V, L = 2.2 µH (NR3015T2R2M), C_{IN} = 4.7 µF (0805) and C_{OUT} = 10 µF (0805) and T_A = 25°C, unless otherwise noted.

R_{DS_ON} (WSON) vs. V_{IN}

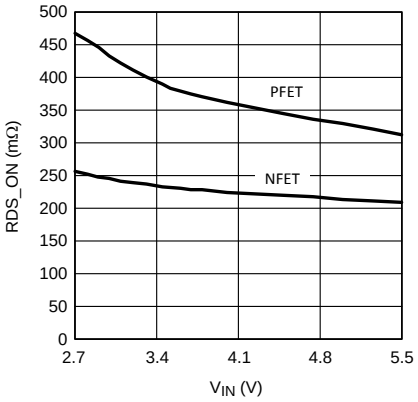


Figure 9.

Current Limit vs. V_{IN}

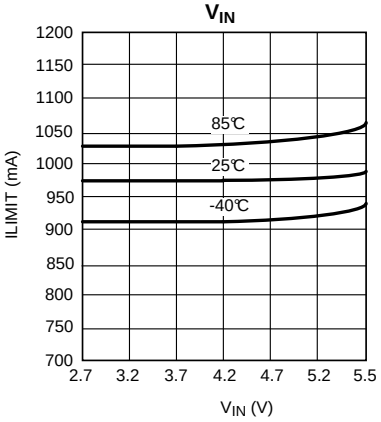


Figure 10.

Switching Frequency vs. V_{IN}

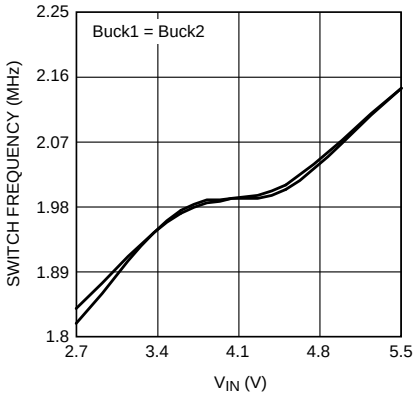


Figure 11.

Output Voltage vs. Output Current V_{IN} = 3.6V (Forced PWM)

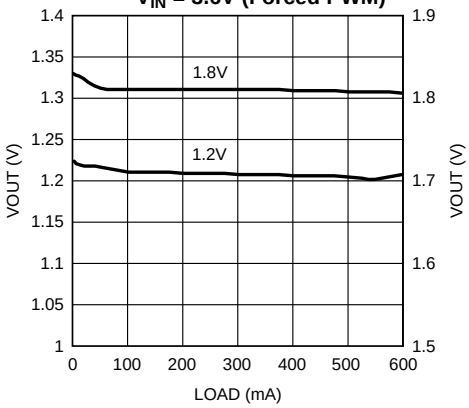


Figure 12.

Efficiency vs. Output Current Forced PWM Mode, V_{OUT1} = 1.2V

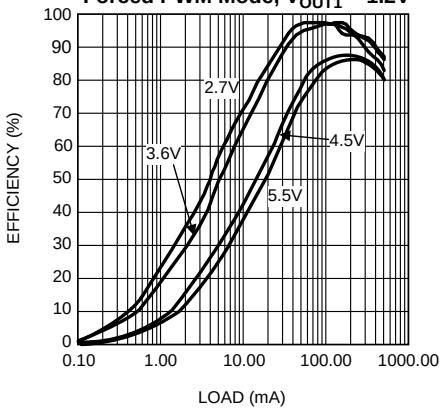


Figure 13.

Efficiency vs. Output Current Forced PWM Mode, V_{OUT1} = 1.8V

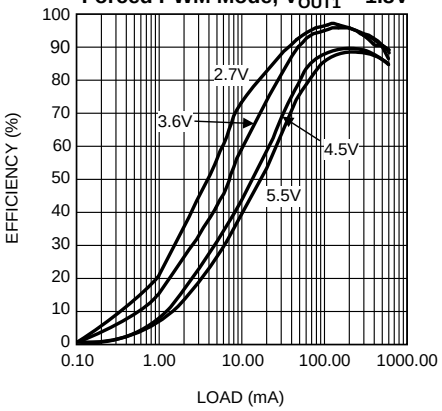


Figure 14.

Typical Performance Characteristics (continued)

LM3370, Circuit of Typical Application Circuit, V_{IN} = 3.6V, V_{OUT1} = 1.5V and V_{OUT2} = 2.5V, L = 2.2 µH (NR3015T2R2M), C_{IN} = 4.7 µF (0805) and C_{OUT} = 10 µF (0805) and T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current Auto Mode, V_{OUT1} = 1.5V

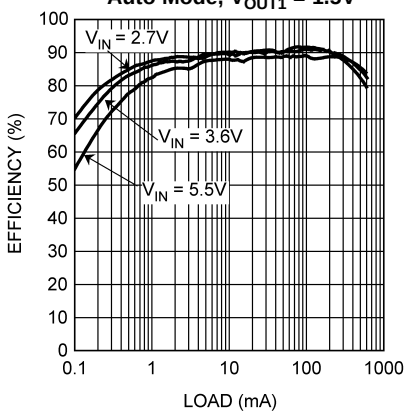


Figure 15.

Efficiency vs. Output Current Auto Mode, V_{OUT2} = 1.9V

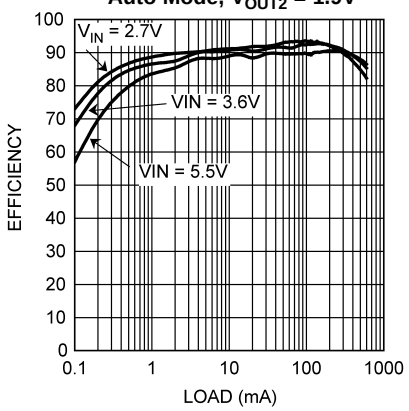


Figure 16.

Efficiency vs. Output Current Auto Mode, V_{OUT2} = 3.3V

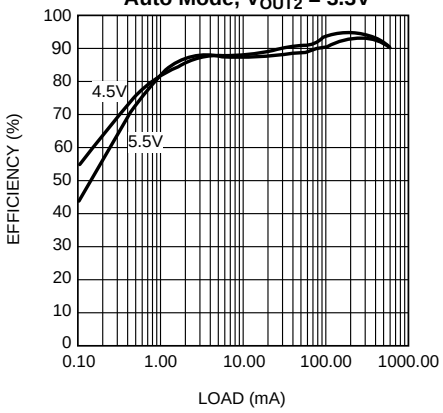


Figure 17.

Efficiency vs. Output Current Forced PWM Mode, V_{OUT2} = 3.3V

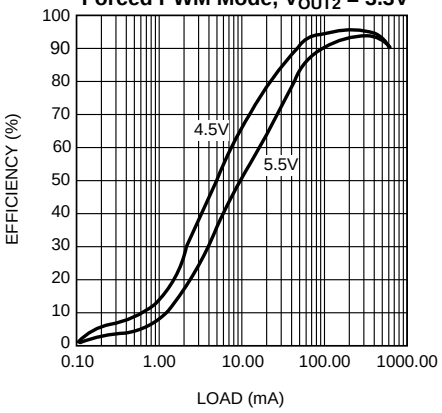


Figure 18.

Typical Operation Waveform V_{IN} = 3.6V, V_{OUT1} = 1.8V and V_{OUT2} = 1.8V Load = 400 mA

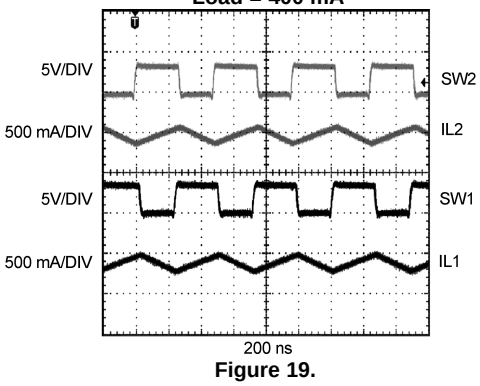


Figure 19.

Typical Operation Waveform V_{IN} = 4.8V, V_{OUT1} = 1V and V_{OUT2} = 3.3V Load = 400 mA

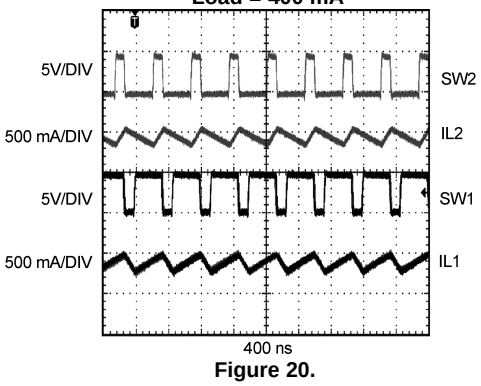


Figure 20.

Typical Performance Characteristics (continued)

LM3370, Circuit of Typical Application Circuit, V_{IN} = 3.6V, V_{OUT1} = 1.5V and V_{OUT2} = 2.5V, L = 2.2 µH (NR3015T2R2M), C_{IN} = 4.7 µF (0805) and C_{OUT} = 10 µF (0805) and T_A = 25°C, unless otherwise noted.

Typical Operation Waveform
V_{IN} = 3.6V, V_{OUT1} = 1.5V, V_{OUT2} = 2.5V, Load = 600 mA Each

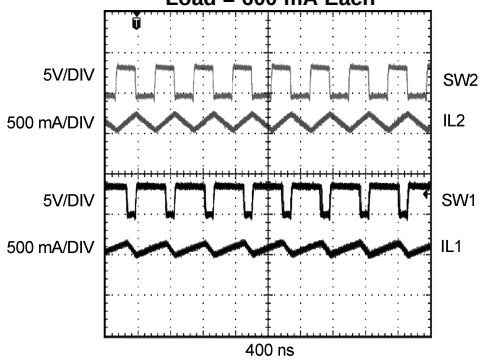


Figure 21.

Startup at PWM for BUCK1
(V_{IN} = 3.6V, V_{OUT} = 1.5V, Load = 200 mA)

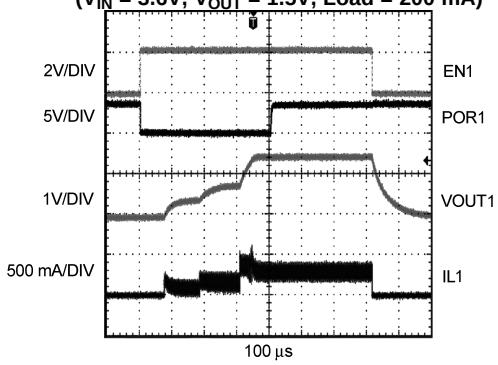


Figure 22.

Startup at PWM for BUCK2
(V_{IN} = 3.6V, V_{OUT} = 2.5V, Load = 200 mA)

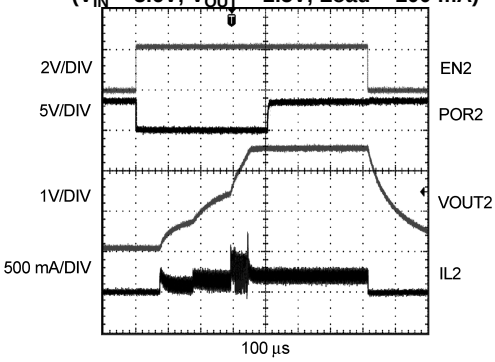


Figure 23.

Line Transient
(V_{OUT1} = 1.2V)

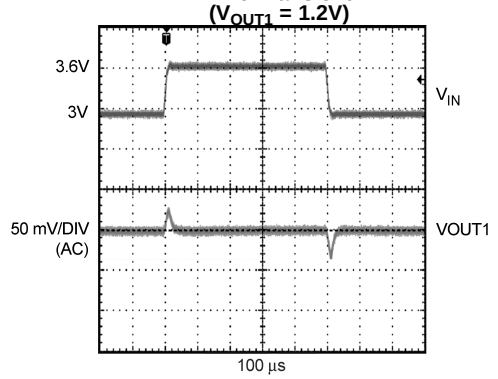


Figure 24.

Line Transient
(V_{OUT2} = 1.8V)

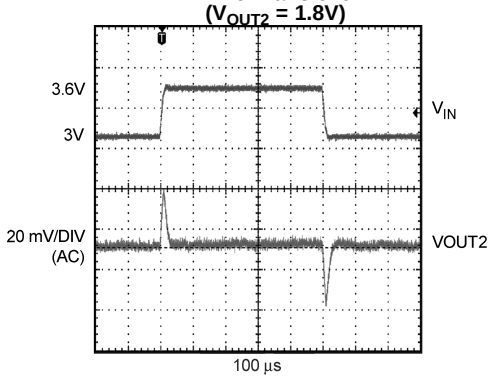


Figure 25.

Load Transient in PFM MODE
(V_{OUT1} = 1.5V)

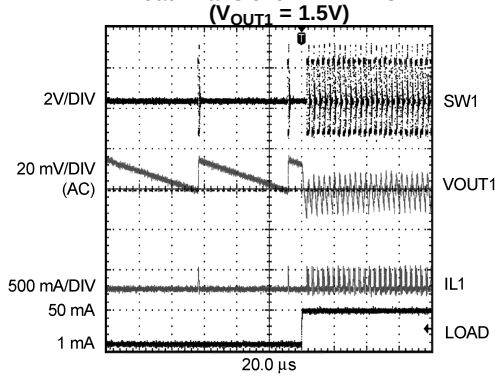


Figure 26.

Typical Performance Characteristics (continued)

LM3370, Circuit of Typical Application Circuit, V_{IN} = 3.6V, V_{OUT1} = 1.5V and V_{OUT2} = 2.5V, L = 2.2 µH (NR3015T2R2M), C_{IN} = 4.7 µF (0805) and C_{OUT} = 10 µF (0805) and T_A = 25°C, unless otherwise noted.

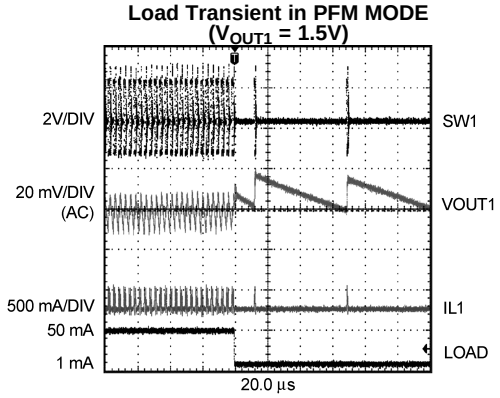


Figure 27.

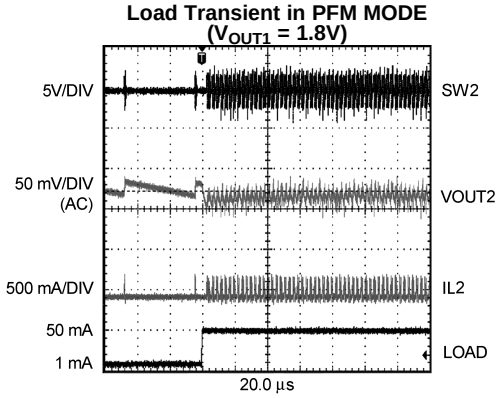


Figure 28.

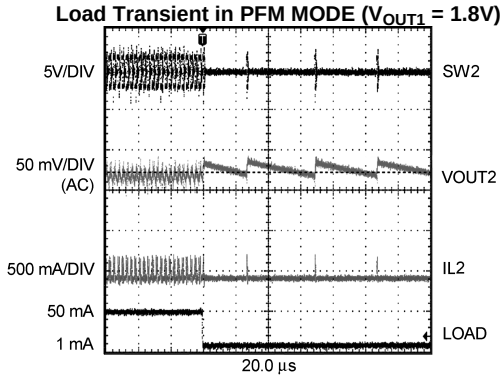


Figure 29.

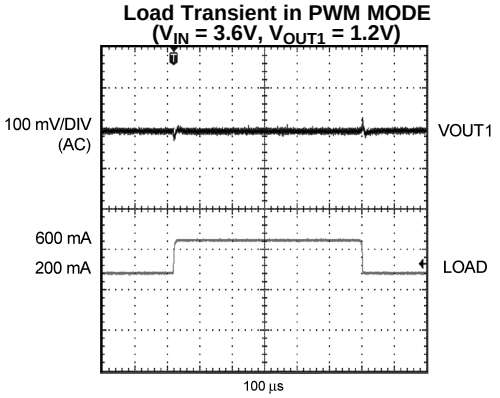


Figure 30.

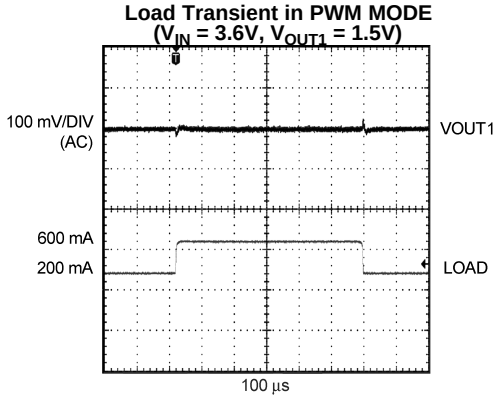


Figure 31.

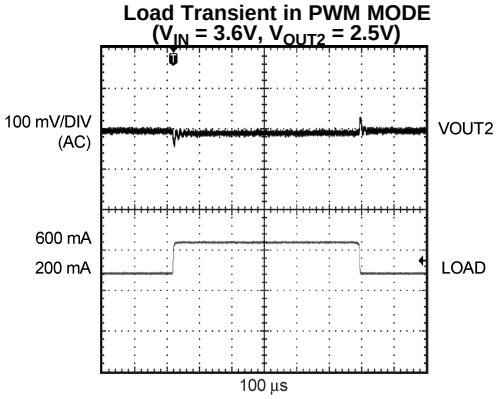


Figure 32.

Typical Performance Characteristics (continued)

LM3370, Circuit of Typical Application Circuit, V_{IN} = 3.6V, V_{OUT1} = 1.5V and V_{OUT2} = 2.5V, L = 2.2 µH (NR3015T2R2M), C_{IN} = 4.7 µF (0805) and C_{OUT} = 10 µF (0805) and T_A = 25°C, unless otherwise noted.

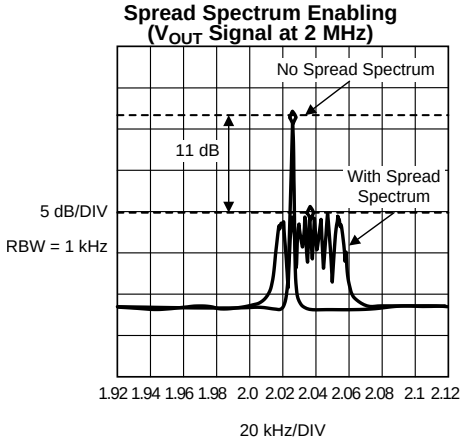


Figure 33.

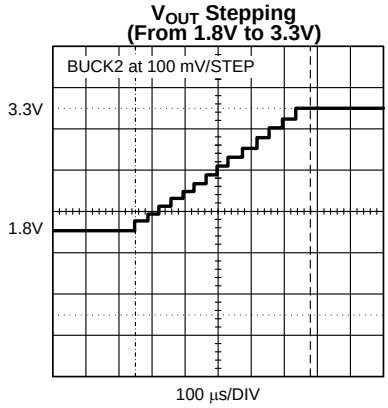


Figure 34.

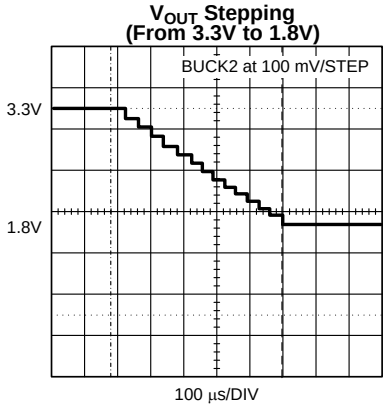


Figure 35.

OPERATION DESCRIPTION

Device Information

The LM3370, a dual high efficiency step-down DC-DC converter, delivers regulated voltages from input rails between 2.7V to 5.5V. Using voltage mode architecture with synchronous rectification, the LM3370 has the ability to deliver up to 600 mA per channel. The performance is optimized for systems where efficiency and space are critical.

There are three modes of operation depending on the current required: PWM, PFM, and shutdown. PWM mode handles loads of approximately 70 mA or higher with 90% efficiency or better. Lighter loads cause the device to automatically switch into PFM mode to maintain high efficiency with low supply current (I_Q = 20µA typ.) per channel.

The LM3370 can operate up to a 100% duty cycle (PFET switch always on) for low drop out control of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

Additional features include soft-start, under-voltage lock-out, current overload protection, and thermal overload protection.

Circuit Operation

During the first portion of each switching cycle, the control block in the LM3370 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of

$$\frac{V_{IN} - V_{OUT}}{L} \quad (1)$$

by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of

$$\frac{-V_{OUT}}{L} \quad (2)$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

Internal Synchronous Rectification

While in PWM mode, the LM3370 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LM3370 to protect itself and external components during overload conditions. PWM mode implements cycle-by-cycle current limiting using an internal comparator that trips at 1200 mA (typ.). If the outputs are shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor has more time to decay, thereby preventing runaway.

PFM Operation

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions are true, for a duration of 32 or more clock cycles:

1. The NFET current reaches zero.
2. The peak PFET switch current drops below the I_{MODE} level .

$$\left(\text{Typically } I_{MODE} < 66\ \text{mA} + \frac{V_{IN}}{160\Omega}\right) \tag{3}$$

Supply current during this PFM mode is less than 20 µA per channel, which allows the part to achieve high efficiency under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.2% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see Figure 36) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PFET power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 115\ \text{mA} + V_{IN}/57\Omega \tag{4}$$

Once the PFET power switch is turned off, the NFET power switch is turned on until the inductor current ramps to zero. When the NFET zero-current condition is detected, the NFET power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 36), the PFET switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NFET switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode.

Forced PWM Mode

The LM3370 auto mode can be bypassed by forcing the device to operate in PWM mode, this can be implemented through the I^2C-compatible interface, see Table 3.

Soft-Start

The LM3370 has a soft start circuit that limits in-rush current during start up. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.7V.

LDO - Low Drop Out Operation

The LM3370 can operate at 100% duty cycle (no switching, PFET switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. The minimum input voltage needed to support the output voltage is

$$V_{IN,MIN} = I_{LOAD}*(R_{DSON,PFET} + R_{INDUCTOR}) + V_{OUT}$$

where

- I_{LOAD} load current
- • $R_{DSON/PFET}$ drain to source resistance of PFET switch in the triode region
- • $R_{INDUCTOR}$ inductor resistance (5)

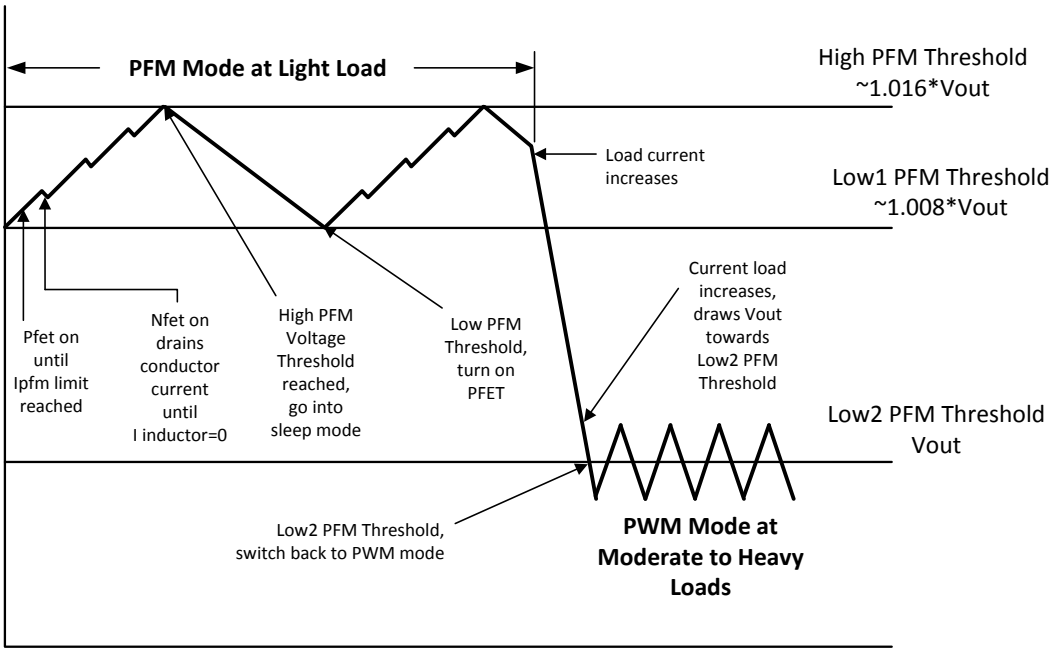


Figure 36. Operation in PFM Mode and Transfer to PWM Mode

Table 1. I²C-Compatible Interface Electrical Specifications (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{CLK}	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time between Start and Stop	(2)	**1.3**			µS
t_{HOLD}	Hold Time Repeated Start Condition	(2)	**0.6**			µS
t_{CLKLP}	CLK Low Period	(2)	**1.3**			µS
t_{CLKHP}	CLK High Period	(2)	**0.6**			µS
t_{SU}	Set Up Time Repeated Start Condition	(2)	**0.6**			µS
$t_{DATAHLD}$	Data Hold Time	(2)	**200**			nS
t_{CLKSU}	Data Set Up Time	(2)	**200**			nS
T_{SU}	Set Up Time for Start Condition	(2)	**0.6**			µS
T_{TRANS}	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both DATA and CLK signals.	(2)		50		nS
VDD_I²C	I²C Logic High Level		1		V_{IN}	V

(1) Unless otherwise noted, V_{BATT} = 2.7V to 5.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −30°C to +125°C.

(2) Input voltage range for all voltage options is 2.7V to 5.5V. The voltage range recommended for the specified output voltages: V_{IN} = 2.7V to 5.5V for 1V ≤ V_{OUT} ≤ 1.7V and for V_{OUT} = 1.8V or greater, $V_{IN} = V_{OUT} + 1V or V_{IN,MIN} = I_{LOAD} * (R_{DSON\_PFET} + R_{DCR\_INDUCTOR}) + V_{OUT}$

I²C-Compatible Interface

In I²C-compatible mode, the SCL pin is used for the I²C clock and the SDA pin is used for the I²C data. Both these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistor are determined by the capacitance of the bus (typ. ~1.8k). Signal timing specifications are according to the I²C bus specification. Maximum frequency is 400 kHz.

I²C-Compatible Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

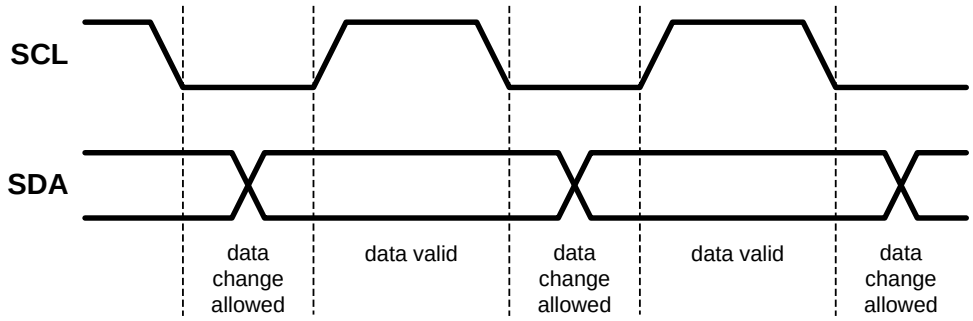


Figure 37.

I²C-Compatible START and STOP Conditions

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

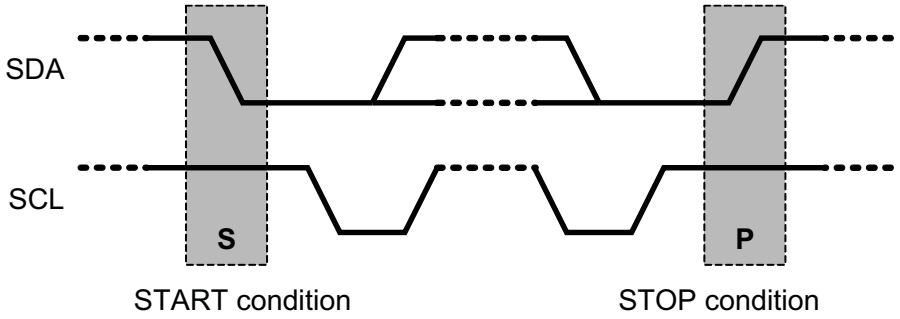


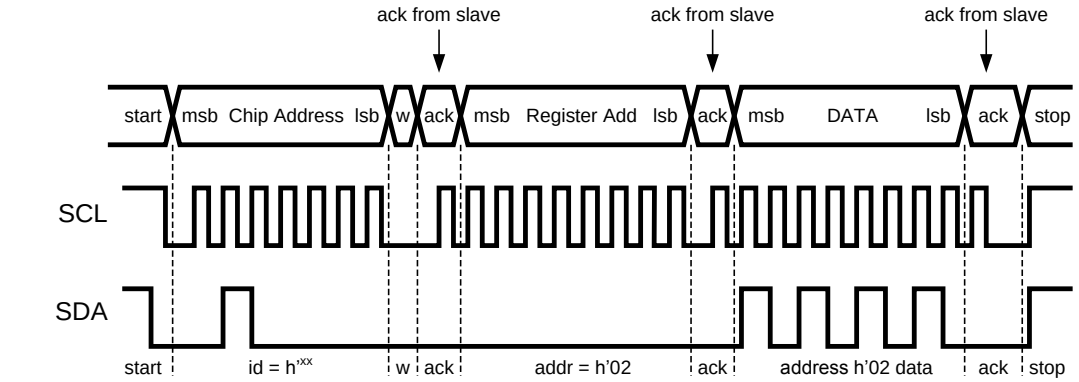
Figure 38.

Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

I²C-Compatible Write Cycle



W = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated startxx=36h

Figure 39.

However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in I²C-Compatible Read Cycle

I²C-Compatible Read Cycle

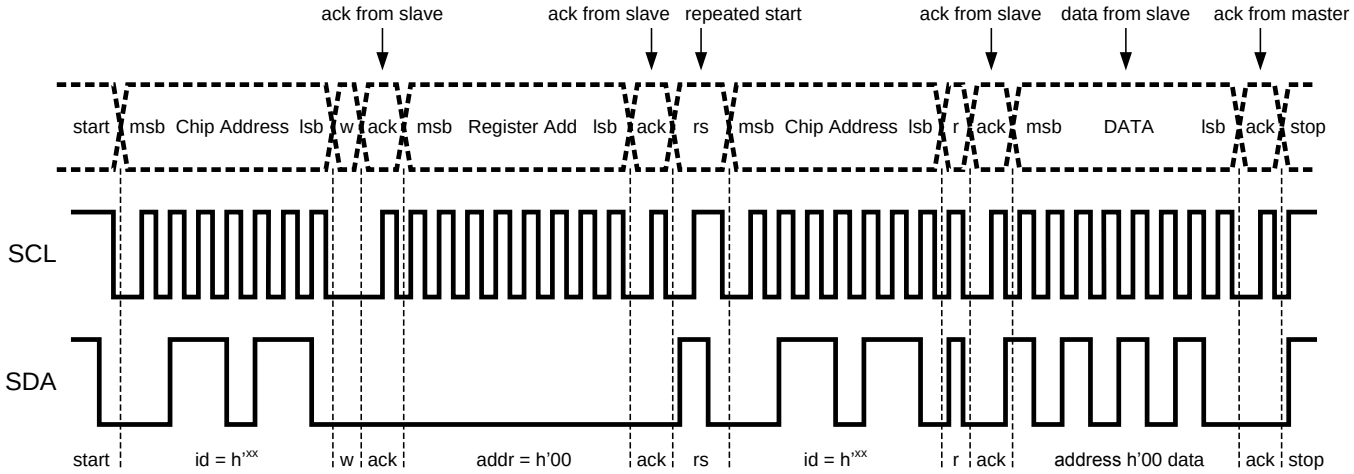


Figure 40.

Device Register Information

Table 2. Register Information

Register Name	Location	Type	Function
Control	00	R/W	Control signal for Buck 1 and Buck 2
Buck 1	01	R/W	Output setting and Mode selection for Buck 1
Buck 2	02	R/W	Output setting and Mode selection for Buck 2 and POR disable

I²C Chip Address Information

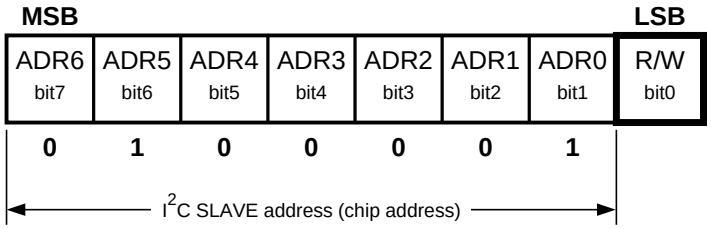
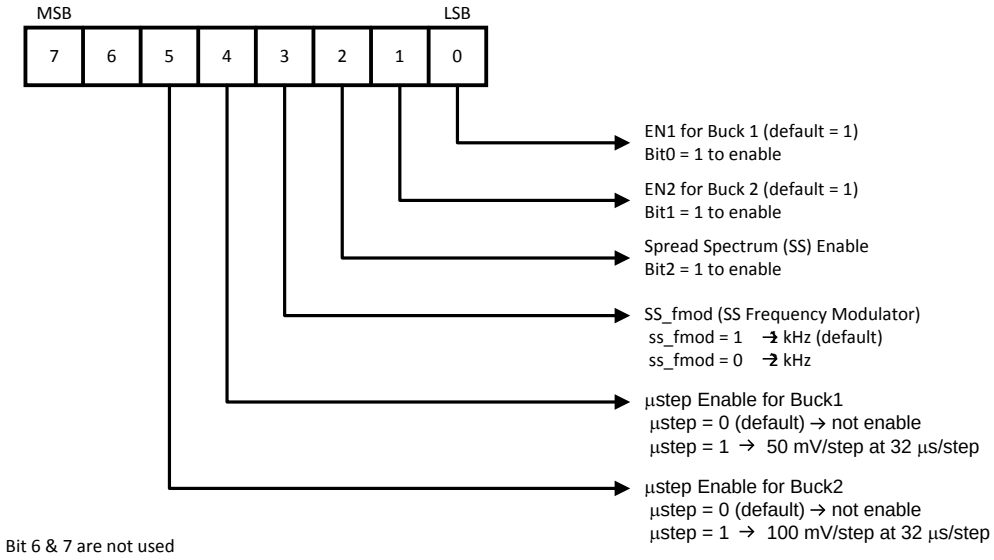


Figure 41.

Register 00



Register 01

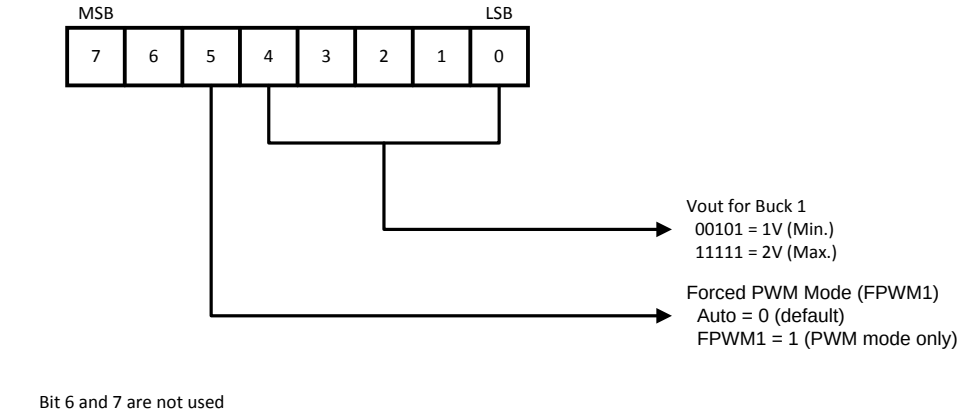


Figure 42.

Register 02

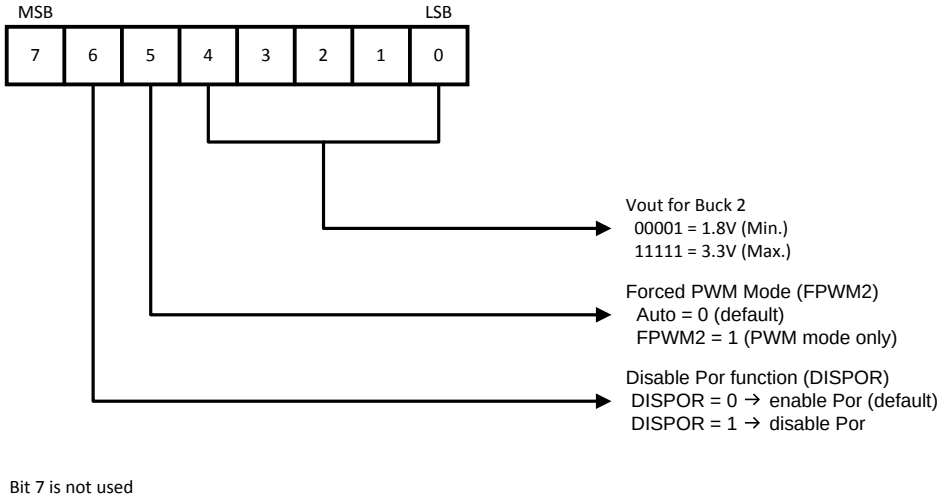


Figure 43.

Table 3. Output Selection Table via I²C Programing

Buck Output Voltage Selection Codes		
Data Code	**Buck_1 (V)**	**Buck_2 (V)**
00000	NA	NA
00001	NA	1.8
00010	NA	1.85 or 1.9(1)
00011	NA	2.0
00100	NA	2.1
00101	1.00	2.2
00110	1.05	2.3
00111	1.10	2.4
01000	1.15	2.5
01001	1.20	2.6
01010	1.25	2.7
01011	1.30	2.8
01100	1.35	2.9
01101	1.40	3.0
01110	1.45	3.1
01111	1.50	3.2
10000	1.55	3.3
10001	1.60	NA
10010	1.65	NA
10011	1.70	NA
10100	1.75	NA
10101	1.80	NA
10110	1.85	NA
10111	1.90	NA
11000	1.95	NA
11001	2.00	NA

(1) Can be trimmed at the factory at 1.85V or 1.9V using the same trim code.

Application Information

Setting Output Voltage via I²C-Compatible

The outputs of the LM3370 can be programmed through Buck 1 and Buck 2 registers via I²C. Buck 1 output voltage can be dynamically adjusted between 1V to 2V in 50 mV steps and Buck 2 output voltage can be adjusted between 1.8V to 3.3V in 100 mV steps. Finer adjustments to the output of Buck 2 can be achieved with the placement of a resistor between VOUT2 and the FB2 pin. Typically by placing a 20 KΩ resistor, R, between these nodes will result in the programmed Output Voltage increasing by approximately 45 mV,ΔV_{TYP}.

$$\Delta V_{TYP} = R \times 500mV / 234K\Omega \quad (6)$$

Please refer to for programming the desire output voltage. If the I²C-compatible feature is not used, the default output voltage will be the pre-trimmed voltage. For example, LM3370SD-3021 refers to 1.2V for Buck 1 and 3.3V for Buck 2.

V_{DD} Pin

V_{DD} is the power supply to the internal control circuit, if V_{DD} pin is not tied to V_{IN} during normal operating condition, V_{DD} must be set equal or greater of the two inputs (V_{IN1} or V_{IN2}). An optional capacitor can be used for better noise immunity at V_{DD} pin or when V_{DD} is not tied to either V_{IN} pins. Additionally, for reasons of noise suppression, it is advisable to tie the EN1/EN2 pins to V_{DD} rather than V_{IN} .

SDA, SCL Pins

When not using I²C the SDA and SCL pins should be tied directly to the V_{DD} pin.

Micro-Stepping:

The Micro-Stepping feature minimizes output voltage overshoot/undershoot during large output transients. If Micro-stepping is enabled through I²C, the output voltage automatically ramps at 50 mV per step for Buck 1 and 100 mV per step for Buck 2. The steps are summarized as follow:

- Buck 1: 50 mV/step and 32 µs/step
- Buck 2: 100 mV/step and 32 µs/step

For example if changing Buck 1 voltage from 1V to 1.8V yields 20 steps [(1.8 - 1)/ 0.05 = 20]. This translates to 640 µs [(20 x 32 µs) = 640 µs] needed to reach the final target voltage.

Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple.

There are two methods to choose the inductor current rating.

method 1:

The total current is the sum of the load and the inductor ripple current. This can be written as

$$I_{MAX} = I_{LOAD} + \left(\frac{I_{RIPPLE}}{2}\right)$$

$$= I_{LOAD} + \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

where

- I_{LOAD} load current
- V_{IN} input voltage
- L inductor
- f switching frequency

(7)

method 2:

A more conservative approach is to choose an inductor that can handle the maximum current limit of 1400 mA.

Given a peak-to-peak current ripple (I_{PP}) the inductor needs to be at least

$$L >= \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \quad (8)$$

A 2.2 µH inductor with a saturation current rating of at least 1400 mA is recommended for most applications. The inductor's resistance should be less than around 0.2Ω for good efficiency. Table 4 lists suggested inductors and suppliers.

For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

Below are some suggested inductor manufacturers that include but are not limited to:

Table 4. Suggested Inductors and Suppliers

Model	Vendor	Dimensions (mm)	I_{SAT}
DO3314-222	Coilcraft	3.3 x 3.3 x 1.4	1.6A
LPO3310-222		3.3 x 3.3 x 1.0	1.1A
SD3114-2R2	Cooper	3.1 x 3.1 x 1.4	1.48A
NR3010T2R2M	Taiyo Yuden	3.0 x 3.0 x 1.0	1.1A
NR3015T2R2M		3.0 x 3.0 x 1.5	1.48A
VLF3010AT- 2R2M1R0	TDK	2.6 x 2.8 x 1.0	1.0A

Input Capacitor Selection

A ceramic input capacitor of 4.7 µF, 6.3V is sufficient for most applications. A larger value may be used for improved input voltage filtering. The input filter capacitor supplies current to the PFET switch of the LM3370 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with a surge current rating sufficient for the power-up surge from the input power source. The power-up surge current is approximately the capacitor's value (µF) times the voltage rise rate (V/µs).

The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case IRMS is:

$$I_{RMS} = \frac{I_{OUTMAX}}{2} \quad \text{(duty cycle = 50\%)} \quad (9)$$

Output Capacitor Selection

DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. The output ripple voltage can be calculated as:

Voltage peak-to-peak ripple due to capacitance =

$$V_{PP-C} = \frac{I_{PP}}{f*8*C} \quad (10)$$

Voltage peak-to-peak ripple due to ESR = $V_{PP-ESR} = I_{PP} * R_{ESR}$

Voltage peak-to-peak ripple, root mean squared =

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2} \quad (11)$$

Note that the output ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent (as well as temperature dependent); make sure that the frequency of the R_{ESR} given is the same order of magnitude as the switching frequency.

Table 5. Suggested Capacitors and Their Suppliers

Model	Description	Case Size	Vendor
4.7 µF for C_{IN}			
C1608X5R0J475	Ceramic, X5R, 6.3V Rating	0603	TDK
C2012X5R0J475	Ceramic, X5R, 6.3V Rating	0805	
JMK212BJ475	Ceramic, X5R, 6.3V Rating	0805	Taiyo Yuden
GRM21BR60J475	Ceramic, X5R, 6.3V Rating	0805	muRata
GRM219R60J-475KE19D	Ceramic, X5R, 6.3V Rating	0805(Thin) <1mm Height	
10µF C_{OUT}			
C2012X5R0J106	Ceramic, X5R, 6.3V Rating	0805	TDK
JMK212BJ106	Ceramic, X5R, 6.3V Rating	0805	Taiyo Yuden
GRM21BR60J106	Ceramic, X5R, 6.3V Rating	0805	muRata
GRM219R60J-106KE19D	Ceramic, X5R, 6.3V Rating	0805(Thin) < 1mm Height	

POR (Power on Reset)

The LM3370 has an independent POR functions (nPOR) for each buck converter. The nPOR1 and nPOR2 are open drain circuits which pull low when the outputs are below 94% (rising V_{OUT}) or 85% (falling V_{OUT}) of the desire output. The inherent delay between the output (at 94% of V_{OUT}) to the time at which the nPOR is enabled is about 50 ms. A pullup resistor of 100 kΩ at nPOR pin is required. Please refer to the electrical specification table for other timing options. The diagram below illustrates the timing response of the POR function.

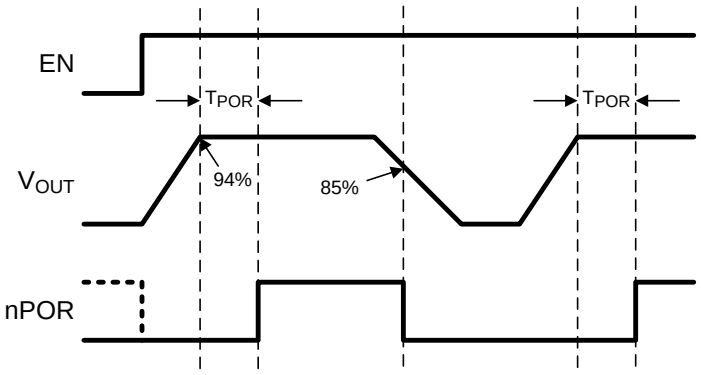


Figure 44.

Spread Spectrum (SS)

The LM3370 features Spread Spectrum capability, via I^2C, to reduce the noise amplitude of the switching frequency during data transmission. The feature can be enabled by activating the appropriate control register bit (see Table 2 for details). The main clock of the LM3370 features spread spectrum at F_{OSC} = 2 MHz ± 22 kHz (peak frequency deviation) with the modulation frequency of either 1 kHz (default) or 2 kHz via I^2C. This help reduce noise caused by the harmonics present in the waveforms at the switch pins of the buck regulators. It is controlled by I^2C in the following manner:

I^2C bit	Modulation Frequency
SS_fmod = 1 (default)	1 kHz
SS_fmod = 0	2 kHz

Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Good layout for the LM3370 can be implemented by following a few simple design rules:

1. *Place the LM3370, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2 in. (5mm) of the LM3370.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor, through the LM3370 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3370 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the LM3370, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3370 by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit*. This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3370 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112 (SNVA009). Refer to the section *Surface Mount Technology Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 (SNVA009) for specific instructions how to do this. The 20-bump DSBGA package used for the LM3370 has 300 micron solder balls and requires 10.82 mils pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90°

entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7 mil wide, for a section approximately 7 mil long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criteria is symmetry. This ensures the solder bumps on the LM3370 DSBGA package re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A2/B1 of V_{OUT1}, and E2/D1 of V_{OUT2}, because V_{IN} and PGND are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

REVISION HISTORY

Changes from Revision M (May 2013) to Revision N	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3370SD-3013/NOPB	ACTIVE	WSON	NHR	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	S0003UB	Samples
LM3370SD-3021/NOPB	ACTIVE	WSON	NHR	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	S0003TB	Samples
LM3370SD-3416/NOPB	ACTIVE	WSON	NHR	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	S0003VB	Samples
LM3370SD-4221/NOPB	ACTIVE	WSON	NHR	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	S0003YB	Samples
LM3370SDX-3013/NOPB	ACTIVE	WSON	NHR	16	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	S0003UB	Samples
LM3370SDX-4221/NOPB	ACTIVE	WSON	NHR	16	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	S0003YB	Samples
LM3370TL-3006/NOPB	ACTIVE	DSBGA	YZR	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SPUB	Samples
LM3370TL-3022/NOPB	ACTIVE	DSBGA	YZR	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		STHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

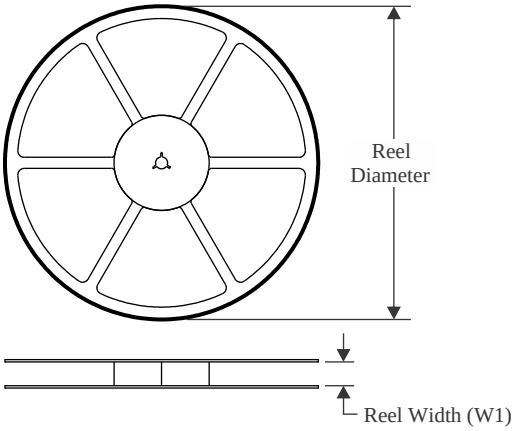
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

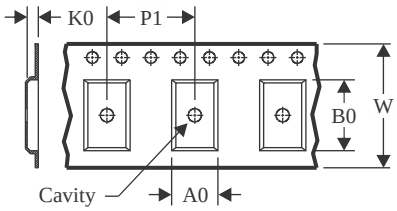
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

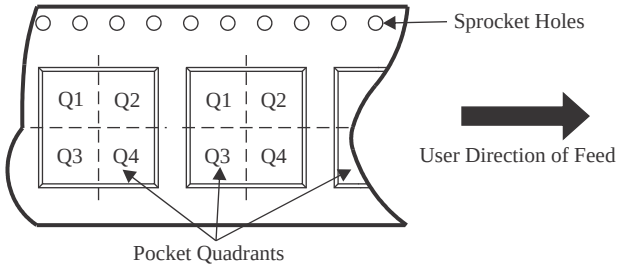


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

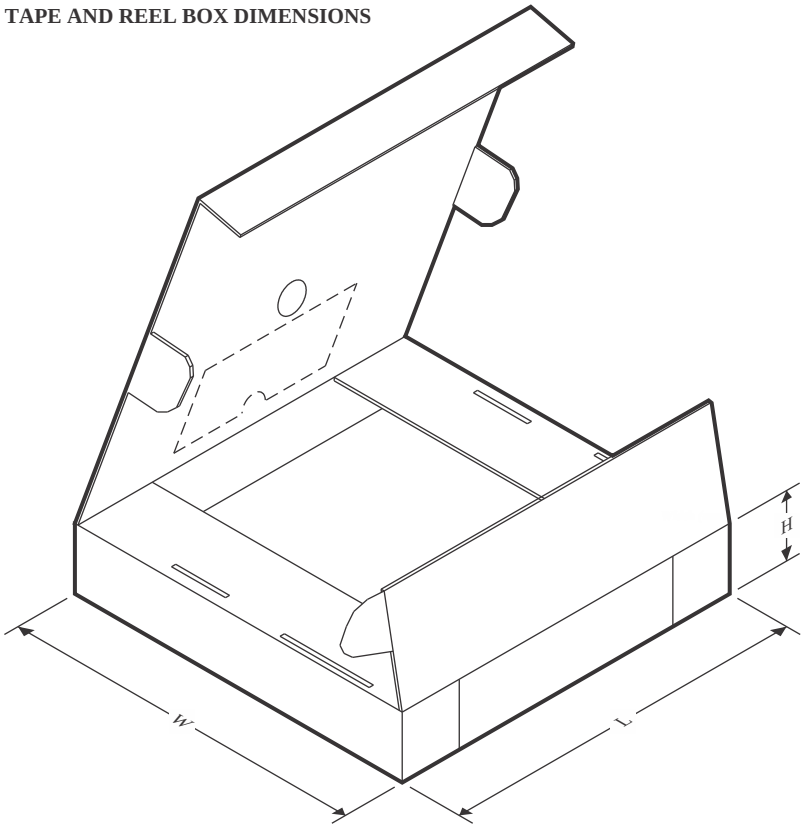
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3370SD-3013/NOPB	WSON	NHR	16	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM3370SD-3021/NOPB	WSON	NHR	16	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM3370SD-3416/NOPB	WSON	NHR	16	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM3370SD-4221/NOPB	WSON	NHR	16	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM3370SDX-3013/NOPB	WSON	NHR	16	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM3370SDX-4221/NOPB	WSON	NHR	16	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM3370TL-3006/NOPB	DSBGA	YZR	20	250	178.0	8.4	2.18	3.12	0.76	4.0	8.0	Q1
LM3370TL-3022/NOPB	DSBGA	YZR	20	250	178.0	8.4	2.18	3.12	0.76	4.0	8.0	Q1

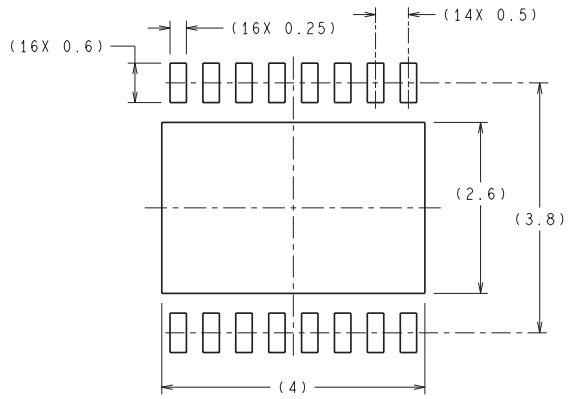
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

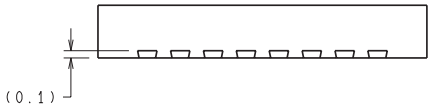
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3370SD-3013/NOPB	WSON	NHR	16	1000	208.0	191.0	35.0
LM3370SD-3021/NOPB	WSON	NHR	16	1000	208.0	191.0	35.0
LM3370SD-3416/NOPB	WSON	NHR	16	1000	208.0	191.0	35.0
LM3370SD-4221/NOPB	WSON	NHR	16	1000	210.0	185.0	35.0
LM3370SDX-3013/NOPB	WSON	NHR	16	4500	367.0	367.0	35.0
LM3370SDX-4221/NOPB	WSON	NHR	16	4500	367.0	367.0	35.0
LM3370TL-3006/NOPB	DSBGA	YZR	20	250	208.0	191.0	35.0
LM3370TL-3022/NOPB	DSBGA	YZR	20	250	208.0	191.0	35.0

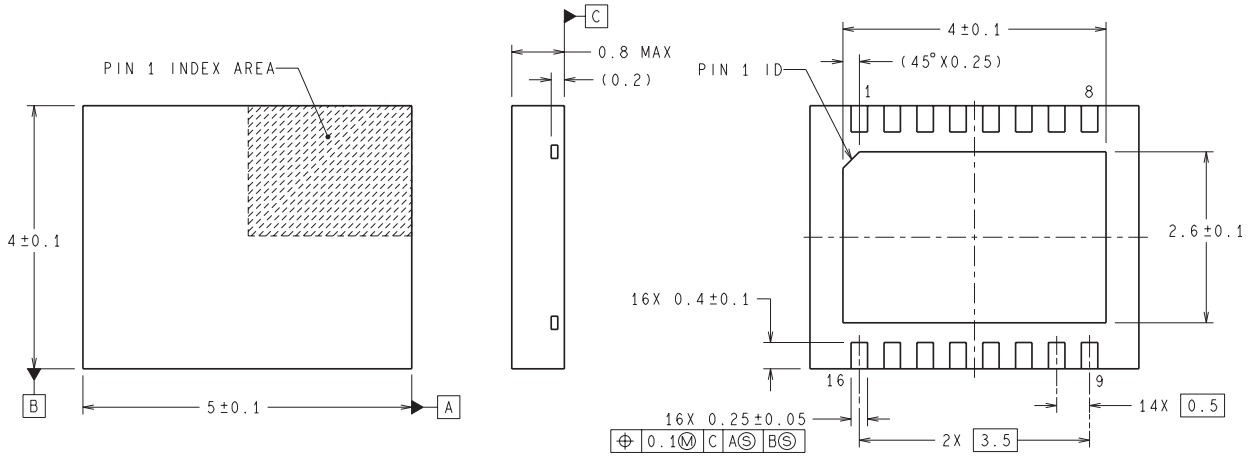
NHR0016B



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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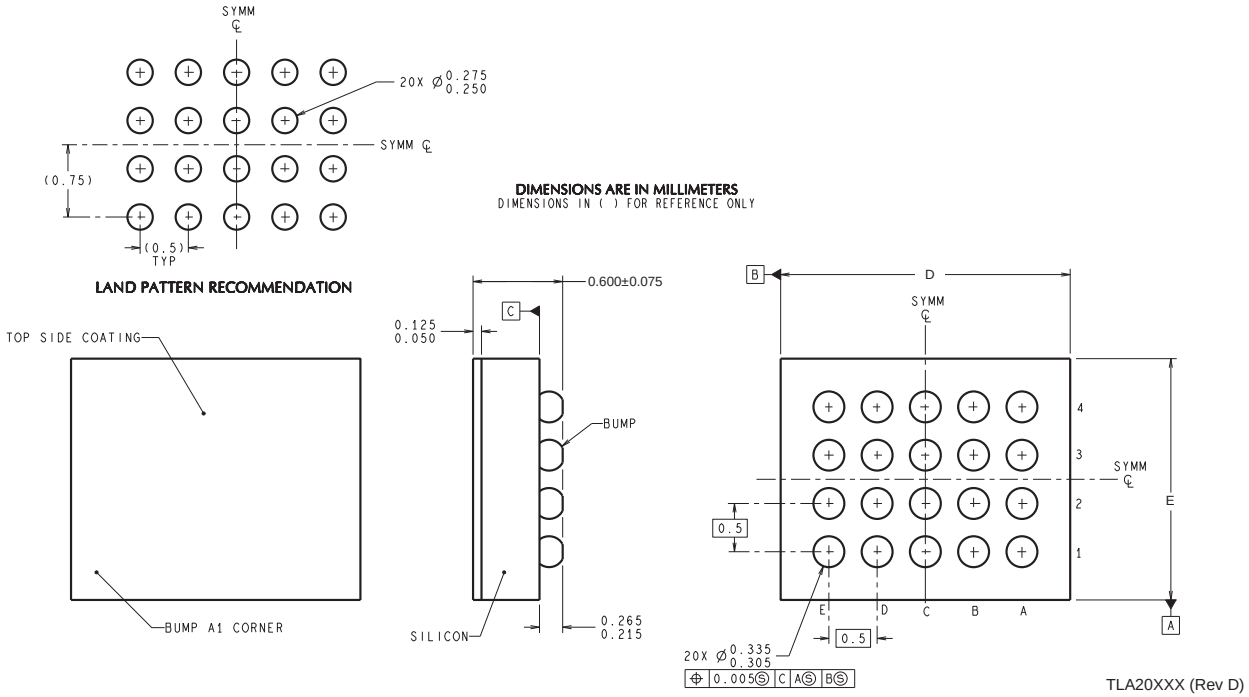

D: Max = 3.025 mm, Min =2.965 mm

E: Max = 2.086 mm, Min =2.026 mm

4215053/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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