

Differential Line Receiver

FEATURES:

- Meets or exceeds EIA-422B and RS-485 requirements
- Suited for single-point or multipoint bus transmission
- Common mode input voltage from 0 to 30V
- Differential input voltages from 0 to 30V
- Differential input switching threshold < 200mV
- Failsafe output for floating, shorted and terminated inputs
- Three-state output
- Fully compatible with LS7272 series line drivers
- Pin compatible with SN65175 and SN75175 receivers
- 5V supply
- Available in SOIC-16 and TSSOP-16

APPLICATIONS:

- Data communication

GENERAL DESCRIPTION:

LS7372 is a monolithic CMOS quadruple differential line receiver with 3-state outputs. The receivers meet the specifications of EIA-422B and RS-485 in respect of balanced multipoint bus transmission at rates up to 10Mbits/s. Each of the two pairs of receivers have a separate enable input. The receivers feature high input impedance and input hysteresis for increased noise immunity. The inputs have differential threshold of 200mV over the common-mode input range of 0 to 30V allowing it to be effective complement of LS7272 series of line drivers. LS7372 is fully pin compatible with SN65175 and SN75175 line drivers for direct replacements.

Failsafe operation of LS7372 allows its application in multipoint bus transmission by switching the output to logic high whenever the inputs are shorted or open for cases of either terminated or un-terminated inputs. In multipoint bus connection the failsafe operation is necessitated by the fact that individual drivers take turn in getting hold of the bus with float state of the bus while switching control from one driver to another. The high state of the receiver output in this condition allows for correct start bit at the beginning of transmission.

INPUTS/OUTPUTS:

IN0, **IN1**, **IN2**, **IN3** (PINS 2, 6, 10, 14). Non-inverting differential inputs for receivers 0, 1, 2 and 3. The inputs have internal soft pull-up of 500K.

IN0/, **IN1/**, **IN2/**, **IN3/** (PINS 1, 7, 9, 15). Inverting differential inputs for receivers 0, 1, 2 and 3. The inputs have internal soft pull-up of 500K.

OUT0, **OUT1**, **OUT2**, **OUT3** (PINS 3, 5, 11, 13). Receivers 0, 1, 2 and 3 outputs.

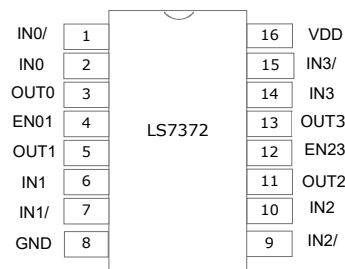


Fig 1 (SOIC-16 and TSSOP-16)

EN01 (PIN 4). Enable input for receivers 0 and 1. A logic low at this pin disables receivers 0 and 1, driving OUT0 and OUT1 to high impedance state. A logic high at the input enables receivers 0 and 1 with OUT0 and OUT1 states as per table 1.

EN23 (PIN 12). Enable input for receivers 2 and 3. A logic low at this pin disables receivers 2 and 3, driving OUT2 and OUT3 to high impedance state. A logic high at the input enables receivers 2 and 3 with OUT2 and OUT3 states as per table 1

TABLE 1

DIFFERENTIAL VOLTAGE $V_{ID} = (V_{IN} - V_{IN/})$	EN	OUT
$V_{ID} \geq 0.2V$	HI	HI
$-0.2V < V_{ID} < 0.2V$	HI	?
$V_{ID} \leq -0.2V$	HI	LO
SHORT	HI	HI
OPEN	HI	HI
X	LO	Z

HI = high level, LO = low level, ? = indeterminate
X = don't care, Z = high impedance

GND (Pin 8). Supply voltage negative terminal.

VDD (Pin 16). Supply voltage positive terminal.

ABSOLUTE MAXIMUM RATINGS:
(All voltages are referenced to GND; T_A = +25°C unless otherwise specified)

Supply Voltage.....-0.3V min, +7V max
 Differential input voltage..... -5.0V min, +35V max
 All other input voltage. -0.3V min, VDD+0.3V max
 Operating temperature.....-40°C to +125°C
 Storage temperature.....-65°C to +150°C

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, or for any infringements of patent rights of others which may result from its use

ELECTRICAL CHARACTERISTICS; VDD = 5V, T _A = 25°C unless specified otherwise						
Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	VDD	4.5	-	5.5	Volt	
Supply Current	I _{DD}					
Common-mode input voltage	V _{IC}	0	-	30.0	Volt	
Differential-mode input voltage	V _{ID}	0	-	30.0	Volt	
Differential input switching threshold, (V _{INX} - V _{INX})	V _{IDST}	-	±200	-	mV	V _{INX} = 5.0V
Differential input hysteresis	V _{Ihyst}	-	30	-	mV	
Inputs EN01 and EN23 logic low	V _{ELO}	-	0.3VDD	-	Volt	
Inputs EN01 and EN23 logic high	V _{EHI}	-	0.7VDD	-	Volt	
Inputs EN01 and EN23 hysteresis	V _{Ehyst}	-	0.33VDD	-	Volt	VDD = 3.0 to 5.5V _{ff}
EN01, N23 logic low input current	I _{ELO}	-	-	-50	nA	Leakage current
EN01, N23 logic high input current	I _{EHI}	-	-	50	nA	Leakage current
Input current: driver inputs IN0, IN1, IN2, IN3, IN0/, IN1/, IN2/, IN3/	I _{INX}	-	-20	-25	uA	V _{INX} = 0V (note 1)
		-	30	50	uA	V _{INX} = 5V (note 1)
		-	125	140	uA	V _{INX} = 15V (note 1)
		-	275	310	uA	V _{INX} = 30V (note 1)
Input impedance: driver inputs	R _{IN}	100	120	150	KΩ	
High-level output current	I _{OH}	-	-16	-	mA	V _O = VDD - 1V
Low-level output current	I _{OL}	-	16	-	mA	V _O = 0.9V
High-impedance-state output current	I _{OT}	-	-	±100	nA	

SWITCHING CHARACTERISTICS; VDD = 5V, T _A = 25°C, output load = 15pF						
Parameter	Symbol	Min	Typ	Max	Unit	Condition
Driver input-to-output propagation delay, low to high	T _{PLH}		45		ns	Input voltage differential = 2.0V
			60		ns	Input voltage differential = 1.0V
			250		ns	Input voltage differential = 0.2V
Driver input-to-output propagation delay, high to low	T _{PHL}		45		ns	Input voltage differential = 2.0V
			60		ns	Input voltage differential = 1.0V
			375		ns	Input voltage differential = 0.2V
Enable input to driver output propagation delay	T _{PEO}		55		ns	Output switching state: high or low or high impedance.

Note 1. V_{INX} = input voltage at any inverting or non-inverting driver input.

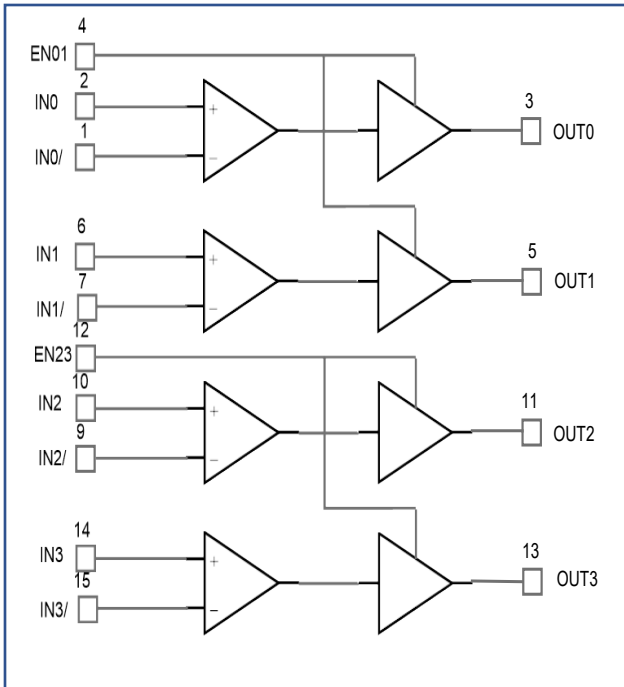


Fig 2. LS7372 Logic diagram

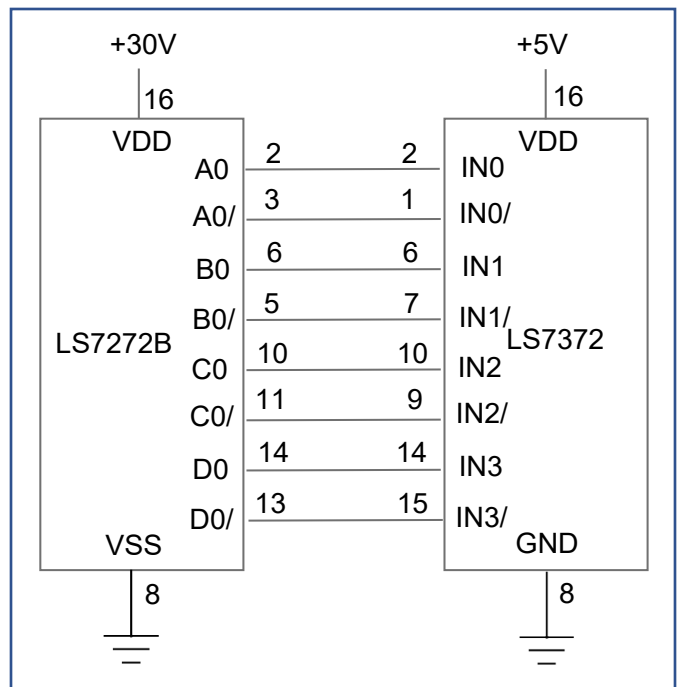
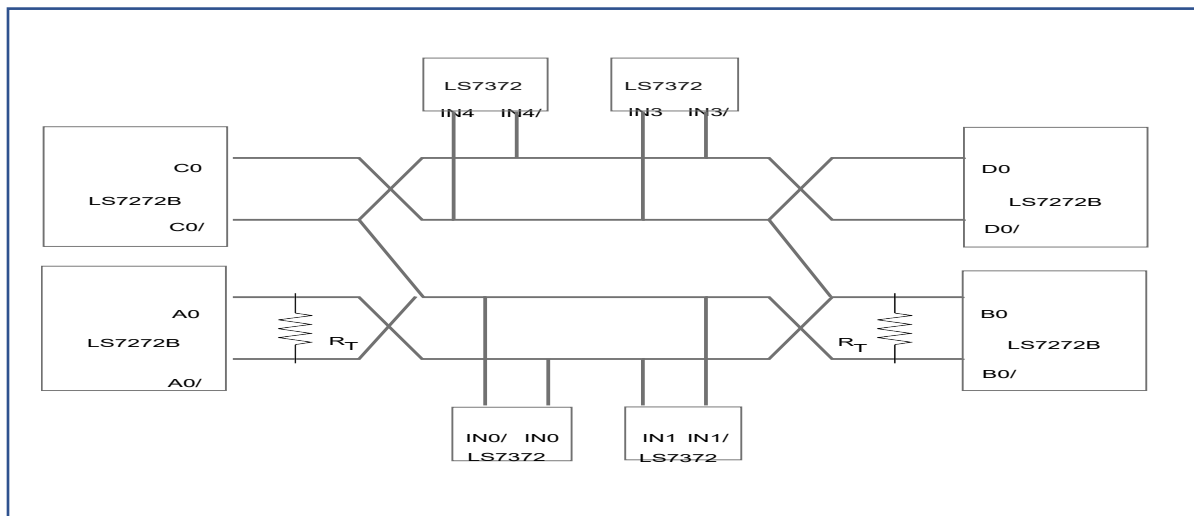


Fig 3. Single-point driver-receiver connection



Note. The line should be terminated at both ends in its characteristic impedance, $R_T = Z_0$

Fig 3. Multipoint driver-receiver bus connection

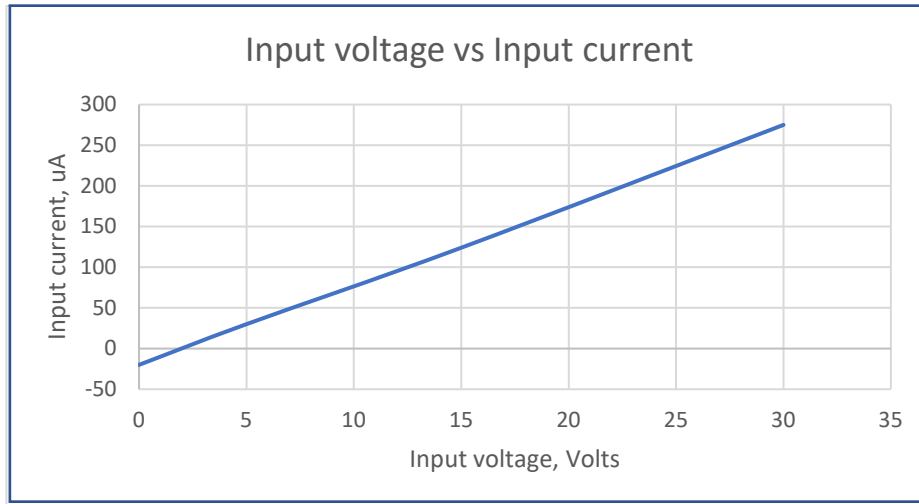
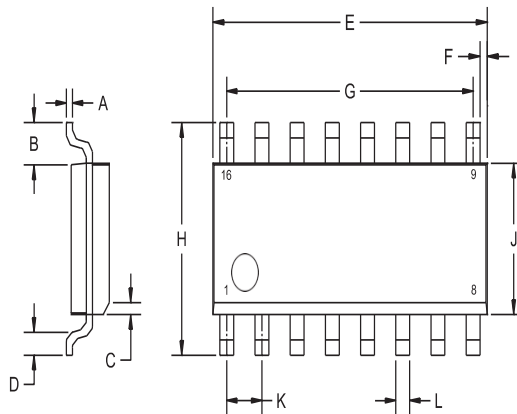


Fig 5. Driver Input-voltage vs Input-current

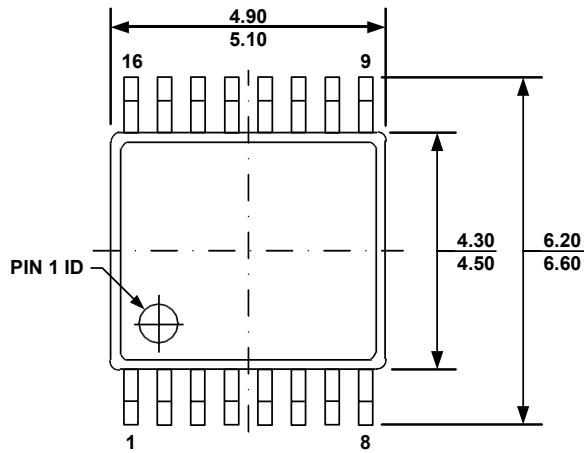
16L SOIC:



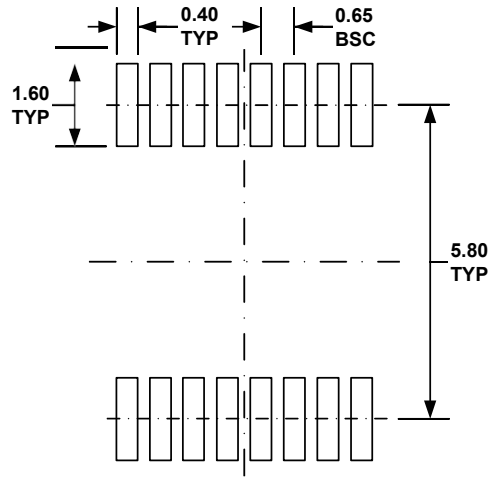
SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.010	0.19	0.25
B	0.041		1.04	
C	0.010	0.020	0.25	0.50
D	0.020	0.035	0.50	0.90
E	0.386	0.394	9.80	10.00
F	0.010		0.25	
G	0.350		8.89	
H	0.228	0.244	5.80	6.20
J	0.150	0.157	3.80	4.00
K	0.050		1.27	
L	0.0138	0.0201	0.35	0.51
M	0.0531	0.0689	1.35	1.75
N	0.0039	0.0098	0.10	0.25

SOIC-16 (REV:R2)

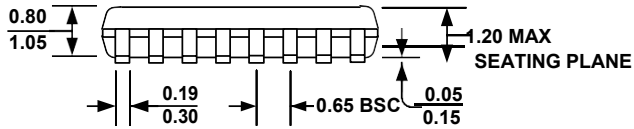
16L TSSOP:



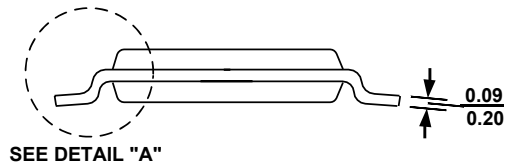
TOP VIEW



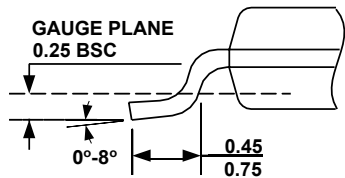
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.