Mars XU3 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mars XU3 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mars XU3 SoC module.

Summary

This document first gives an overview of the Mars XU3 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	MA-XU3	Mars XU3 SoC Module

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Document History

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05	16.02.2021	DIUN	Added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
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1 Overview

1.1 General

1.1.1 Introduction

The Mars XU3 SoC module combines the Xilinx Zynq® UltraScale+ MPSoC (Multiprocessor System-on-Chip) device with USB 3.0, PCIe® Gen2 ×4, USB 2.0 On-The-Go PHY, Gigabit Ethernet, DDR4 SDRAM, eMMC flash, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The use of the Mars XU3 SoC module, in contrast to building a custom MPSoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mars base boards, the Mars XU3 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [15] is available for the Mars XU3 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target and download all the required binaries, such as bitstream and FSBL (First Stage Boot Loader). It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mars XU3 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mars XU3 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars XU3 SoC module.

1.1.5 Safety Recommendations and Warnings

Mars modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mars XU3 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

Warning!

Use the Mars XU3 SoC module only with base boards designed for the Enclustra Mars module family. Inserting the Mars XU3 SoC module into a SO-DIMM connector designed for memory (e.g. a computer main board) may damage the module and the carrier board.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mars XU3 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Xilinx Zynq® UltraScale+™ MPSoC
  - XCZU2CG/XCZU2EG/XCZU3EG device
  - SBVA484 package
  - Quad-core/dual-core ARM® Cortex™-A53 MPCore™ up to 1.33 GHz
  - Dual-core ARM® Cortex™-R5 MPCore™ up to 533 MHz
  - Mali-400 MP2 GPU (not for CG variants)
  - Xilinx 16nm FinFET+ FPGA fabric
- 108 user I/Os
  - 12 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 76 FPGA I/Os (single-ended, differential or analog)
    - 52 HP I/Os (up to 1.8 V)
    - 24 HD I/Os (up to 3.3 V)
  - 20 GTR MGT signals (clock and data)
- 4 GTR MGTs @ 5 Gbit/sec and 2 reference input clock differential pairs
- PCIe Gen2 ×4 (Xilinx built-in PCIe hard block using GTR lines)
- Up to 2 GB DDR4 SDRAM
- 64 MB quad SPI flash
- 16 GB eMMC flash
- Gigabit Ethernet
- USB 2.0 On-The-Go (OTG)
- USB 3.0 (Xilinx built-in USB 3.0 hard block using GTR lines)
- Real-time clock
- SO-DIMM form factor (30 × 67.6 mm, 200 pins)

1.3 Deliverables

- Mars XU3 SoC module
- Mars XU3 SoC module documentation, available via download:
  - Mars XU3 SoC Module User Manual (this document)
  - Mars XU3 SoC Module Reference Design [2]
  - Mars XU3 SoC Module IO Net Length Excel Sheet [3]
  - Mars XU3 SoC Module FPGA Pinout Excel Sheet [4]

- Mars XU3 SoC Module User Schematics (PDF) [5]
- Mars XU3 SoC Module Known Issues and Changes [6]
- Mars XU3 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
- Mars XU3 SoC Module 3D Model (PDF) [8]
- Mars XU3 SoC Module STEP 3D Model [9]
- Mercury Mars Module Pin Connection Guidelines [10]
- Mars Master Pinout [11]
- Mars Heat Sink Mounting Guide [18]
- Enclustra Build Environment [15] (Linux build environment; refer to Section 1.4.2 for details)
- Enclustra Build Environment How-To Guide [16]

1.4 Accessories

1.4.1 Reference Design

The Mars XU3 SoC module reference design features an example configuration for the Zynq Ultrascale+ MPSoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from Github: `https://github.com/enclustra`.

1.4.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [15] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [16] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.4.3 Enclustra Heat Sink

For Mars modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.11.6 for further information on the available cooling options.

1.4.4 Mars ST3 Base Board

- Mars 200-pin SO-DIMM socket
- MIPI D-PHY connector (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- USB 3.0 host connector
- RJ45 Ethernet connector
- 2 × 40-pin GPIO connector (Anios)
- 1 × 8-pin and 1 × 4-pin GPIO connectors (Pmod™ compatible pinout)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder

- User LEDs
- Integrated Xilinx compatible JTAG adapter
- Support for low I/O voltages (1.2 V, 1.8 V)
- Single 12 V DC supply voltage
- Form factor: 100 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.5 Mars EB1 Base Board

- Mars 200-pin SO-DIMM socket
- 2 × Mini Camera Link connectors (requires FPGA support)
- HDMI 1.3 connector (requires FPGA support)
- 40-pin GPIO connector (Anios)
- 3 × 12-pin GPIO connector (two of the connectors with Pmod™ compatible pinout)
- RJ45 Ethernet connector
- USB 2.0 A host connector
- Micro USB 2.0 device connector (shared)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder
- Various switches and LEDs
- Integrated Xilinx compatible JTAG adapter
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 120 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.6 Mars PM3 Base Board

The current Mars PM3 base board revision does not support the Mars XU3 SoC module. Please contact Enclustra for further information.

1.5 Xilinx Tool Support

The MPSoC devices equipped on the Mars XU3 SoC module are supported by the Vivado HL WebPACK Edition software, which is available free of charge. Please contact Xilinx for further information.

2 Module Description

2.1 Block Diagram

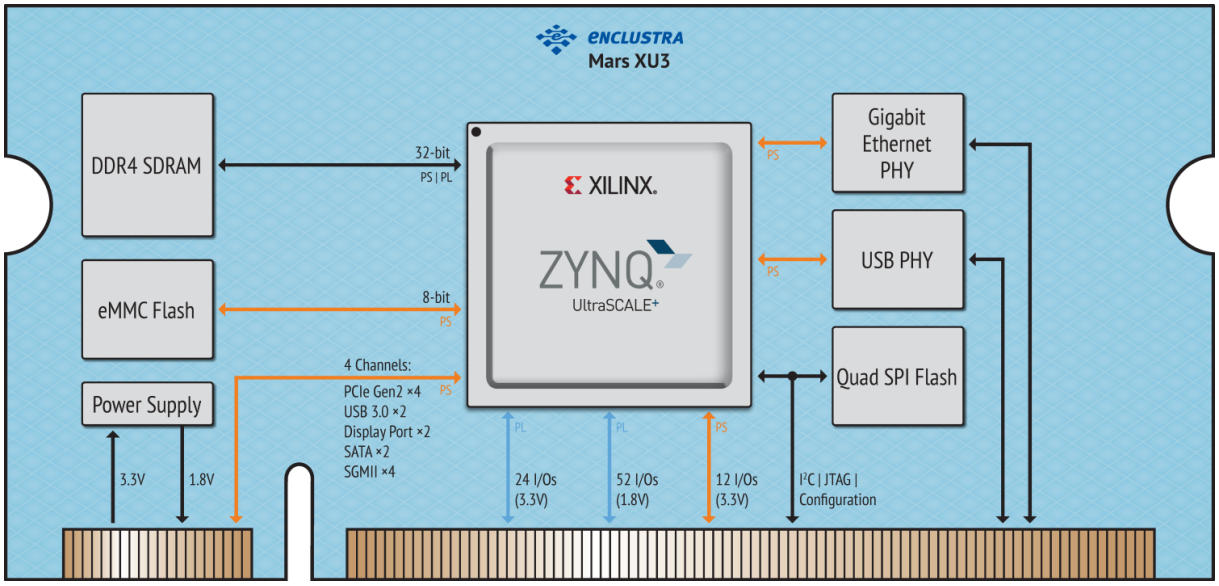

Figure 1: Hardware Block Diagram

The main component of the Mars XU3 SoC module is the Xilinx Zynq Ultrascale+ MPSoC device. Most of its I/O pins are connected to the Mars module connector, making 88 regular user I/Os available to the user. Further, four MGT GTR pairs are available on the module connector, making possible the implementation of several high-speed protocols such as PCIe Gen2 ×4 and USB 3.0 (simultaneous usage of all the interfaces is limited to the available hardware resources i.e. number of transceivers and lane mapping).

The MPSoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mars module connector.

The available standard configurations include a 16 GB eMMC flash, a 64 MB quad SPI flash and 1 GB or 2 GB DDR4 SDRAM.

Further, the module is equipped with a Gigabit Ethernet PHY and a USB 2.0 OTG PHY, making it ideal for communication applications.

A real-time clock is available on the Xilinx Zynq Ultrascale+ MPSoC device.

On-board clock generation is based on a 33.33 MHz crystal oscillator. In addition, two oscillators delivering 100 MHz and 27 MHz reference clocks for the MGT GTR lines, are equipped on the module.

The module can be operated using a 3.3 V DC input, from which all necessary supply voltages are generated. Some of these voltages are available on the Mars module connector to supply circuits on the base board, or can be used as voltage inputs for the FPGA banks.

Four LEDs are connected to the MPSoC pins for status signaling.

2.2 Module Configuration and Product Codes

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	MPSoC	DDR4 SDRAM	Temperature Range
MA-XU3-2CG-1E-D10	XCZU2CG-1SBVA484E	1 GB	0 to +85° C
MA-XU3-2EG-1I-D10	XCZU2EG-1SBVA484I	1 GB	-40 to +85° C
MA-XU3-3EG-2I-D11	XCZU3EG-2SBVA484I	2 GB	-40 to +85° C

Table 1: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

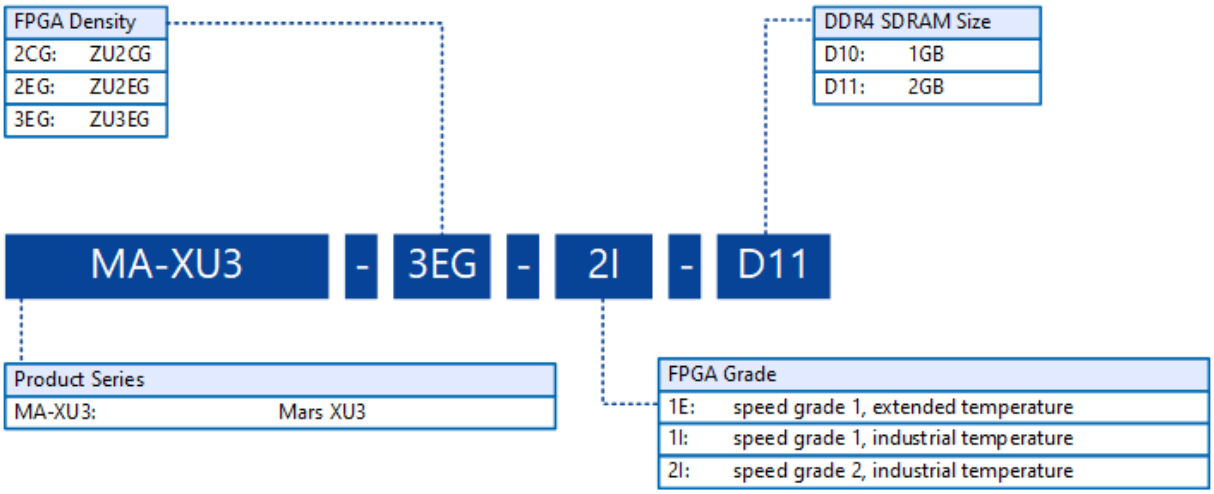

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

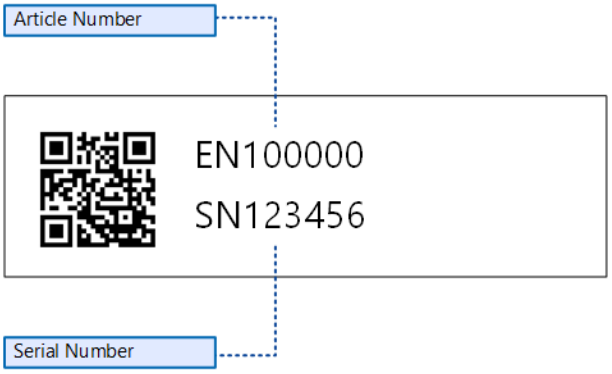

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 2. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mars XU3 SoC Module Known Issues and Changes document [6].

Article Number	Article Code
EN101824	MA-XU3-3EG-1EES-D10-R1
EN101801	MA-XU3-2CG-1E-D10-R1
EN101814	MA-XU3-3EG-2I-D11-R1
EN101981	MA-XU3-2CG-1E-D10-R2
EN101982	MA-XU3-2EG-1I-D10-R2
EN101983	MA-XU3-3EG-2I-D11-R2
EN103302	MA-XU3-2CG-1E-D10-R3
EN103303	MA-XU3-2EG-1I-D10-R3
EN103304	MA-XU3-3EG-2I-D11-R3

Table 2: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

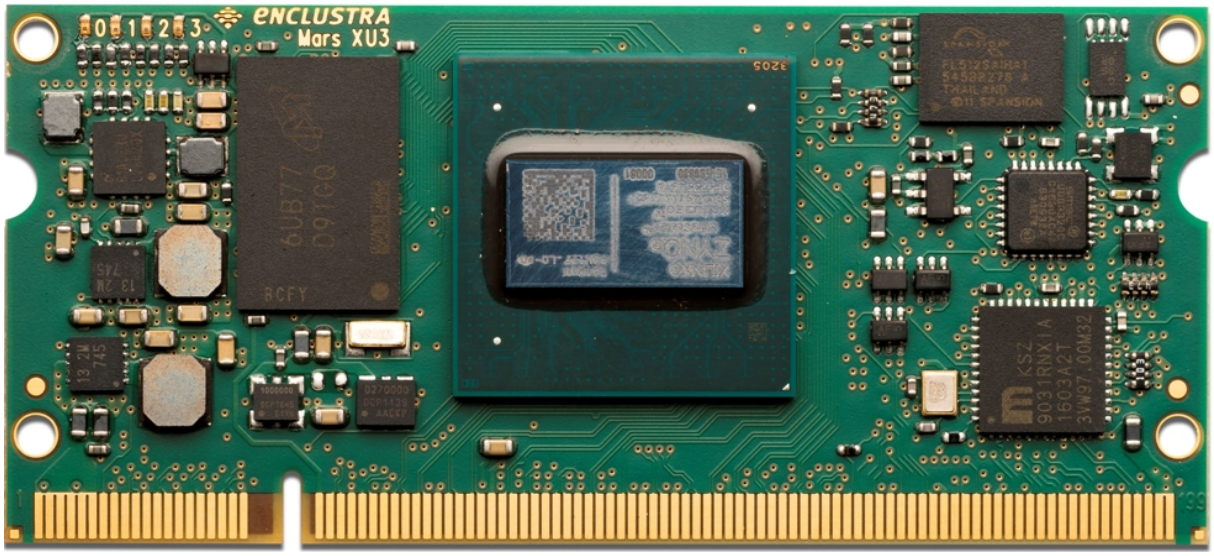

Figure 4: Module Top View

2.4.2 Bottom View

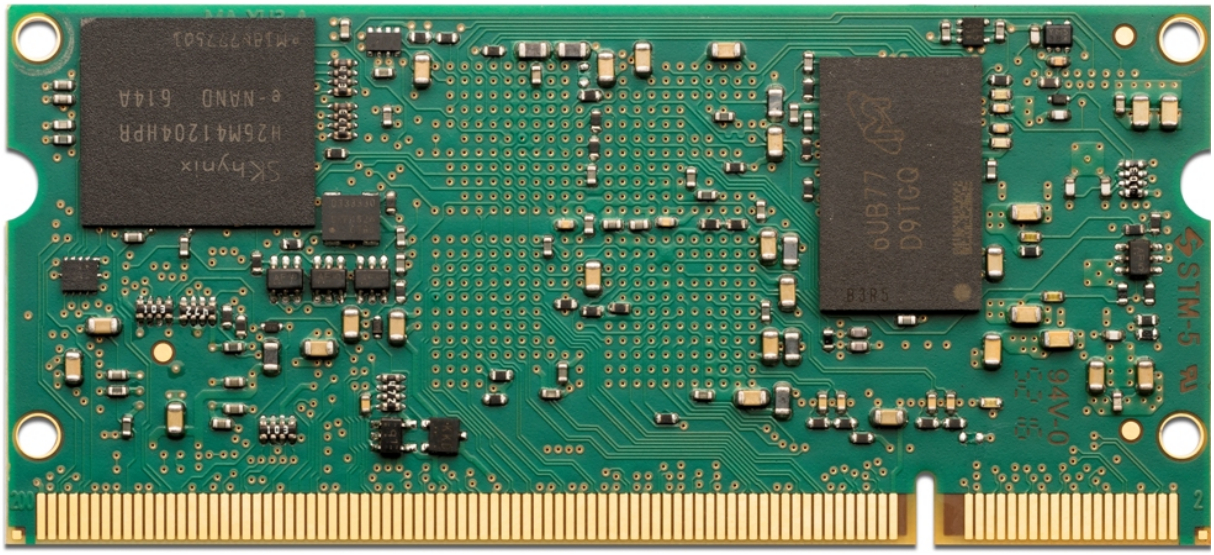

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

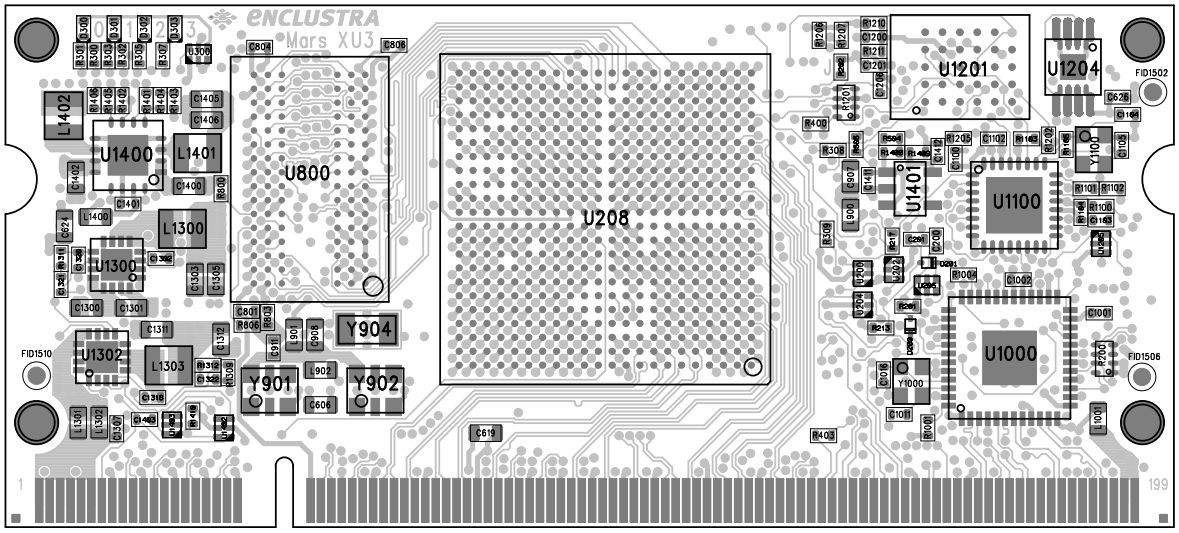

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

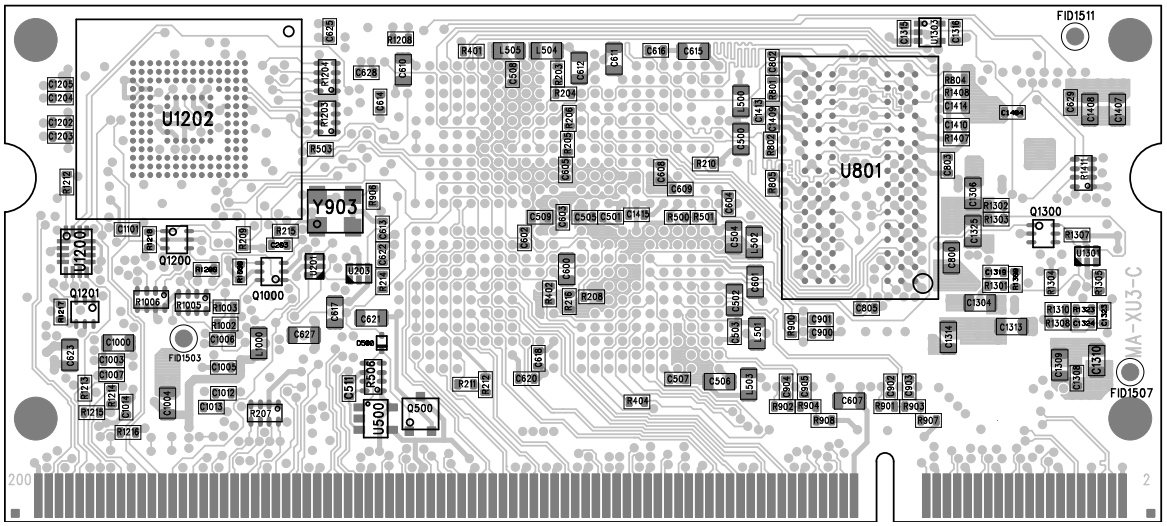

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

The maximum component height under the module is dependent on the connector type - refer to Section 2.8 for detailed connector information.

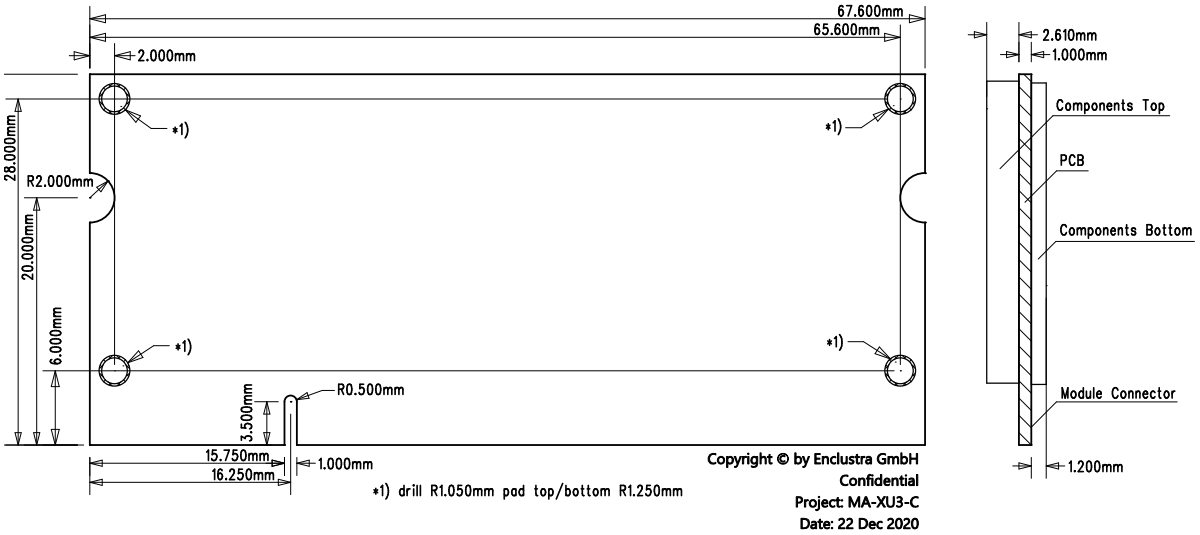

Figure 8: Module Footprint - Top View

The footprint of the module connector is available for different PCB design tools (Altium, Eagle, Orcad, PADS) [7].

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mars XU3 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	67.6 × 30 mm
Component height top	2.61 mm
Component height bottom	1.2 mm
Weight	9 g

Table 3: Mechanical Data

2.8 Module Connector

The Mars XU3 SoC module fits into a 200-pin DDR2 SO-DIMM (1.8 V) socket. Up to four M2 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mars Master Pinout Excel Sheet [11]. The connector to be mounted on the base board is available in different heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Height	Type	Description	Max component height under the module
4.0 mm	TE 292406-4	DDR2-SODIMM, 1.8 V	0 mm
5.2 mm	TE 1565917-4	DDR2-SODIMM, 1.8 V	1 mm
6.5 mm	TE 5-1746530-4	DDR2-SODIMM, 1.8 V	2 mm
8.0 mm	TE 1827341-4	DDR2-SODIMM, 1.8 V	4 mm

Table 4: Module Connector Types

2.9 User I/O

2.9.1 Pinout

Information on the Mars XU3 SoC module pinout can be found in the Enclustra Mars Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mars XU3 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR><_SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B65_L6_AD6_P5_P is located on pin P5 of I/O bank 65, pair 6, it is a System Monitor differential auxiliary analog input capable pin and it has positive polarity, when used in a differential pair.

The global clock capable pins are marked with "GC" (HP I/O banks) or with "HDGC" (HD I/O banks) in the signal name. For details on their function and usage, please refer to the Xilinx documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_B65_<...>	48	24	In/Out	In/Out	65 (HP)[1]
IO_B66_<...>	4	2	In/Out	In/Out	66 (HP)[1]
IO_B26_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 2.9.3 for details.	In/Out	26 (HD)[1]
Total	**76**	**38**	-	-	-

Table 5: User I/Os

The multi-gigabit transceiver (MGT) are described in section 2.10.

[1] HD = high density pins, HP = high performance pins; Refer to the Zynq UltraScale+ MPSoC Overview [23] for details.

2.9.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mars boards they may have a specific role).

PCIe Reset Signal (PERST#)

Table 6 lists the I/O pin exceptions on the Mars XU3 SoC module related to the PCIe reset connection.

I/O Name	Module Connector Pin	Description
PS_MIO42_PERST#	148	Connected via a 1 kΩ resistor to MIO pin 30 for PCIe PERST# connection implementation

Table 6: I/O Pin Exceptions - PERST

The PERST# connection to module connector pin 148 is implemented for future support of PCIe interface on Enclustra Mars base boards.

2.9.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the MPSoC device to the module connector is available in Mars XU3 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mars XU3 SoC module. Please use the information provided in the Mars XU3 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

The I/Os in the HD bank (26) can be used only as differential inputs when LVDS/LVPECL standards are used; LVDS/LVPECL outputs are not supported.

Internal differential termination is not supported for the HD pins; differential input pairs on the module connector may be terminated by external termination resistors on the base board (close to the module pins).

2.9.4 I/O Banks

Table 7 describes the main attributes of the FPGA and PS I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

[2] I2C on PL side is available starting with revision 2 modules.

Bank	Connectivity	VCC_IO	VREF
Bank 65	Module connector, I2C[2], LEDs	User selectable VCC_IO_B65	GND
Bank 66	Module connector, Ethernet PHY	User selectable VCC_IO_B65	GND
Bank 26	Module connector	User selectable VCC_IO_B26	-
Bank 503	FPGA PS Configuration	User selectable VCC_CFG_MIO	-
PS DDR Bank 504	DDR4 SDRAM	1.2 V	-
PS Bank 500	eMMC and QSPI flash devices, I2C, LEDs, GTR oscillators	1.8 V	-
PS Bank 501	Module connector, power circuitry	User selectable VCC_CFG_MIO	-
PS Bank 502	Gigabit Ethernet PHY and USB PHYs	1.8 V	-
PS GTR Bank 505	Module connector, GTR oscillators	VCC_PSINT	-

Table 7: I/O Banks

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mars base boards and modules, it is recommended to use a single I/O voltage.

Signal Name	MPSoC Pins	Supported Voltages	Connector Pins
VCC_CFG_MIO	VCCO_PSIO1_501, VCCO_PSIO3_503	1.8 V - 3.3 V ±5%	137, 146
VCC_IO_B26	VCCO_26	1.2 V - 3.3 V ±5%[3]	53, 62, 73
VCC_IO_B65	VCCO_65	1.0 V - 1.8 V[4] ±5%	82, 117, 126

Table 8: VCC_IO Pins

[3] For voltages of 3.3 V for VCC_IO_B26, the tolerance range is -5% to +3%.

[4] When using voltages lower than 1.8 V for VCC_IO_B65, the I2C bus on FPGA bank 65 is not operational (I2C on PL side is available starting with revision 2).

Warning!

Use only VCC_IO voltages compliant with the equipped MPSoC device; any other voltages may damage the equipped MPSoC device, as well as other devices on the Mars XU3 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped MPSoC device, as well as other devices on the Mars XU3 SoC module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 9 illustrates the VCC_IO power requirements.

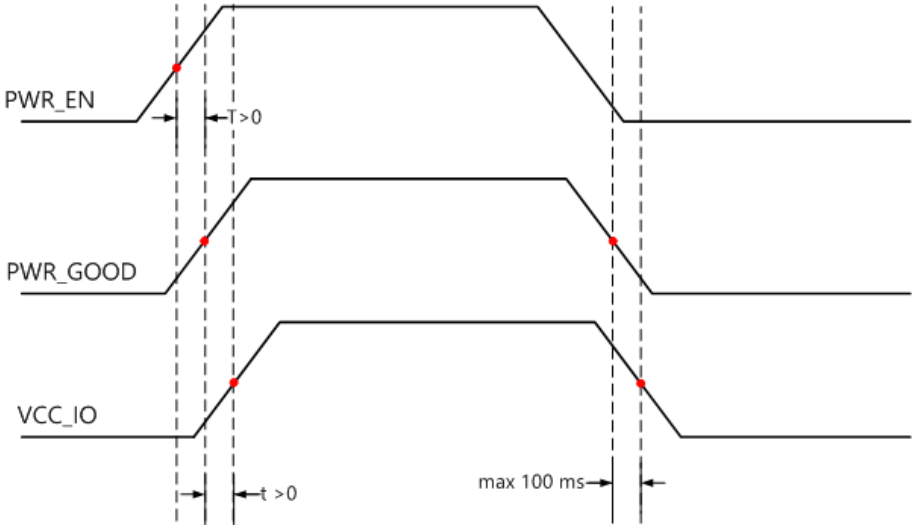

Figure 9: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.6 Signal Terminations

Differential Inputs

Internal differential termination is not supported for the HD pins (bank 26). Differential input pairs on the module connector may be terminated by external termination resistors on the base board (close to the module pins).

Single-Ended Outputs

There are no series termination resistors on the Mars XU3 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

Some of the MIO pins on the Mars XU3 SoC module are connected to on-board peripherals, while others are available as GPIOs; the suggested functions below are for reference only - always verify your MIO pinout with the Xilinx device handbook.

Table 9 gives an overview over the MIO pin connections on the Mars XU3 SoC module. Only the pins marked with "user functionality" are available on the module connector.

MIO Group	Function	Connection
0-5	QSPI flash	QSPI flash
6	QSPI feedback clock	-
7-9	LEDs 0-2	On-board LEDs
10-11	I2C	On-board I2C bus and module connector via level shifter
12	I2C interrupt	On-board I2C bus
13-22	eMMC flash	eMMC flash
23	LED3	On-board LEDs
24	Enable signal for the 100 MHz oscillator	On-board GTR 100 MHz oscillator
25	Enable signal for the 27 MHz oscillator	On-board GTR 27 MHz oscillator
26-29, 32-37, 40-41	Unused	-
30	PCIe block PERST# signal/user functionality	Module connector and MIO42 via series resistor
31	Enable low power mode (PWR_LP_EN# signal)	Power generation circuitry; refer to Section 2.11.1 for details
38 39	UART RX[5]/user functionality UART TX[5]/user functionality	Module connector
42	PCIe block PERST# signal/user functionality	Module connector
43-44	User functionality	Module connector
45-51	SD card/user functionality	Module connector
52-63	USB	USB 2.0 PHY
64-75	Ethernet	Gigabit Ethernet PHY
76-77	Ethernet MDIO	Gigabit Ethernet PHY

Table 9: MIO Pins Connections Overview

2.9.8 Analog Inputs

The Zynq Ultrascale+ MPSoC devices contain a system monitor in the PL and an additional system monitor block in the PS. These are used to sample analog inputs and to collect information on the internal voltages and temperatures.

The system monitor block in the PL provides a 10-bit ADC, which supports up to 17 external analog lines (1 dedicated differential input, 16 auxiliary differential inputs). The auxiliary analog lines of the MPSoC device

[5]UART RX is an MPSoC input; UART TX is an MPSoC output.

are available on the module connector; these I/Os have the abbreviation "AD" followed by the ADC channel in the signal name. The ADC lines are always used differentially; for single-ended applications, the *_N line must be connected to GND. The dedicated channel is not available on the module connector.

The analog input signals can be connected to any normal I/O FPGA bank, provided that all analog pins belong to the same bank. Note that the HD I/O banks have a limited number of analog inputs and they must be connected directly to the SYSMONE4 primitive instead of to the Xilinx System Management Wizard IP core.

For detailed information on the ADC and system monitor, refer to the UltraScale Architecture System Monitor document [20], Zynq UltraScale+ MPSoC Technical Reference Manual [19] and System Management Wizard Product Guide [22].

Table 10 presents the ADC Parameters for the PL System Monitor. The PS System Monitor is only used for monitoring the on-chip power supply voltages and die temperature.

Parameter	Value (PL Sysmon)
VCC_ADC	1.8 V
VREF_ADC	Internal
ADC Range	0-1 V
Sampling Rate per ADC	0.2 MSPS
Total number of channels available on the module connector	16 (only auxiliary inputs)

Table 10: System Monitor (PL) Parameters

2.10 Multi-Gigabit Transceiver (MGT)

GTR Transceivers

There are four GTR MGT pairs and two reference input clock differential pairs on the Mars XU3 SoC module connected to I/O bank 505, available on the module connector.

The naming convention for the GTR MGT I/Os is:
MGTPS_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGTPS_RX2_D22_N is located on pin D22 of PS GTR bank (bank 505), it is a receive pin and it has negative polarity.

All Mars XU3 SoC module variants support the implementation of a PCIe Gen2 ×4 interface.

The PCIe reset signal (PERST#) is available on module connector pin 148. Please note that when the PCIe hard block is used, it is not possible to use PS MIO pin 42 for other functions. Refer to Section 2.9.2 for details on the PERST# connection.

The GTR pairs on the MPSoC device support data rates of up to 6 Gbit/sec and can be used for the implementation of several interfaces such as PCIe Gen2 ×4, USB 3.0, DisplayPort, SATA, or Ethernet SGMII. Please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [19] and to the Zynq UltraScale+ MPSoC Overview [23] for details.

Note that the maximum bandwidth of the GTR lines is limited to 5 Gbit/sec by the module connector.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. Please refer to Section 2.12 for details.

Warning!

The maximum data rate on the MGT lines on the Mars XU3 SoC module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using MGTs at high performance rates.

Warning!

No AC coupling capacitors are placed on the Mars XU3 SoC module on the MGT lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent MGT lines from being damaged.

2.11 Power

2.11.1 Power Generation Overview

The Mars XU3 SoC module uses a 3.3 - 5.0 V DC power input for generating the on-board supply voltages (0.85 V, 0.85 V, 1.2 V, 1.8 V, 2.5 V). Some of these internally-generated voltages are accessible on the module connector. In addition, a separate 3.3 V power input is used to supply peripherals, such as the Ethernet PHY, USB PHY, QSPI flash, eMMC flash, and EEPROM. The 3.3 V input is also used to generate a 2.5 V voltage required to supply the DDR chips, LEDs and oscillators.

Besides the required VCC_IO and VCC_CFG voltages, the Mars XU3 SoC module can be powered using a single power supply. In this case, the two voltage supply inputs VCC_MOD and VCC_3V3 must be connected together to a 3.3 V supply. Please refer to Section 2.11.3 for details on the voltage supply inputs. For the VCC_IO pins usage, please refer to Section 2.9.5.

Table 11 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_INT	0.85 V (PL core supply)	5 A[6]	VCC_MOD	Yes	Yes
VCC_PSINT	0.85 V (PS core supply)	5 A[6]	VCC_MOD	Yes	Yes
VCC_BAT_FPGA	1.5 V[7]	10 mA	VCC_BAT	No	No
VCC_1V2	1.2 V	2 A	VCC_MOD	Yes	Yes
VCC_1V8	1.8 V	2 A	VCC_MOD	Yes	Yes
VCC_2V5	2.5 V	0.2 A	VCC_3V3	Yes	No

Table 11: Generated Power Supplies

[6] This voltage was rated 3 A in previous revisions.
[7] Starting with revision 3 modules use a 1.5 V LDO, earlier revisions use a 1.2 V LDO.

Starting with revision 3, the support for lower power MPSoC devices (speedgrade -2LE or -1LI) has been removed. The PWR_LP_EN# signal has no effect on VCC_INT.

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

2.11.2 Power Enable/Power Good

The Mars XU3 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters and LDOs for 0.85 V, 0.85 V, 1.2 V, 1.8 V and 2.5 V, leaving the MPSoC device and the DDR4 SDRAM unpowered.

The PWR_EN input is pulled to VCC_3V3 on the Mars XU3 SoC module with a 4.7 kΩ[8] resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mars XU3 SoC module with a 4.7 kΩ[8] resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.11.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	13	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	40	0 V: Module supply not ok 3.3 V: Module supply ok

Table 12: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mars XU3 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 9.

2.11.3 Voltage Supply Inputs

Table 13 describes the power supply inputs on the Mars XU3 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

[8] Starting with revision 3 modules use a 4.7 kΩ pull-up resistor, earlier revisions use 10 kΩ.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	1, 3, 5, 7, 9, 11	3.3 - 5.0 V ±10%	Supply for the 0.85 V, 1.2 V and 1.8 V voltage regulators. The input current is rated at 1.8 A (0.3 A per connector pin).
VCC_3V3	197, 199	3.3 V ±5%	Supply for Ethernet PHY, QSPI flash, eMMC flash and EEPROM
VCC_BAT	200	2.0 - 5.5 V	Battery voltage for MPSoC battery-backed RAM and battery-backed RTC

Table 13: Voltage Supply Inputs

2.11.4 Voltage Supply Outputs

Table 14 presents the supply voltages generated on the Mars XU3 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[9]
VCC_PSINT	42	0.85 V ±5%	0.3 A
VCC_1V2	41	1.2 V ±5%	0.3 A
VCC_1V8	89, 94, 101, 106	1.8 V ±5%	1 A (and max 0.3 A per connector pin)

Table 14: Voltage Supply Outputs

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mars XU3 SoC module.

2.11.5 Power Consumption

Please note that the power consumption of any MPSoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Xilinx Power Estimator available on the Xilinx website.

2.11.6 Heat Dissipation

High performance devices like the Xilinx Zynq Ultrascale+ MPSoC need cooling in most applications; always make sure the MPSoC is adequately cooled.

For Mars modules an Enclustra heat sink is available for purchase along with the product. It represents an optimal solution to cool the Mars XU3 SoC module - it is low profile (less than 7 mm tall) and covers the whole module surface. It comes with a gap pad for the MPSoC device and four screws to attach it to the

[9] The maximum available output current depends on your MPSoC design. See sections 2.11.1 and 2.11.5 for details.

module PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, mounting material).

Table 15 lists the heat sink and thermal pad part numbers that are compatible with the Mars XU3 SoC module. Details on the Mars heat sink kit can be found in the Mars Heat Sink Mounting Guide [18].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mars XU3	SBVA484 [24]	HS-MA3	ATS-52190G-C1-R0	TG-A6200-20-20-1

Table 15: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module in used in environments subject to vibrations, a heat sink with mounting screws or clips may be required for optimal fixation.

Warning!

Depending on the user application, the Mars XU3 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the MPSoC is adequately cooled by installing a heat sink and/or providing air flow.

2.11.7 Voltage Monitoring

Several pins on the module connector on the Mars XU3 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 16 presents the VMON pins on the Mars XU3 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_INT	198	VCC_INT	PL core voltage (default) / MPSoC battery voltage (assembly option) / VCC_2V5 (assembly option)

Table 16: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.12 Clock Generation

A 33.33 MHz oscillator is used for the Mars XU3 SoC module clock generation; the 33.33 MHz clock is fed to the PS.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. The enable signals for these two oscillators are connected to MIO pins 24 and 25. Please refer to Section 2.9.7 for details on the MIO connections.

A 24 MHz clock and a 25 MHz clock are used for the USB PHY and Ethernet PHY respectively. The crystal pads for the MPSoC RTC are connected to a 32.768 kHz oscillator on the Mars XU3 SoC module.

Table 17 describes the clock connections to the MPSoC device.

Signal Name	Frequency	Package Pin	MPSoC Pin Type
CLK33	33.33 MHz	H14	PS_REF_CLK
CLK27_GTR_P	27 MHz	E19	PS_MGTREFCLK3P_505
CLK27_GTR_N		E20	PS_MGTREFCLK3N_505
CLK100_GTR_P	100 MHz	G19	PS_MGTREFCLK2P_505
CLK100_GTR_N		G20	PS_MGTREFCLK2N_505
PS_PADI	32.768 kHz	H17	PS_PADI (crystal pad input for MPSoC built-in RTC)
PS_PADO		J17	PS_PADO (crystal pad output for MPSoC built-in RTC)

Table 17: Module Clock Resources

2.13 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the MPSoC device are available on the module connector.

Pulling PS_POR# low resets the MPSoC device, the Ethernet and the USB PHYs, and the QSPI and eMMC flash devices. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling PS_SRST# low resets the MPSoC device and enables the connection between QSPI flash and module connector, allowing the flash to be programmed from an external SPI master.

For details on the functions of the PS_POR_B and PS_SRST_B signals refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

Table 18 presents the available reset signals. Both signals, PS_POR# and PS_SRST#, have on-board 4.7 kΩ[10] pull-up resistors to VCC_CFG_MIO. For on-board devices using 1.8 V signaling, a PS_POR# low voltage variant is generated (PS_POR#_LV).

[10] Starting with revision 3 modules use a 4.7 kΩ pull-up resistor, earlier revisions use 10 kΩ.

Signal Name	Connector Pin	Package Pin	FPGA Pin Type	Description
PS_POR#	196	K12	PS_POR_B	Power-on reset
PS_SRST#	192	K13	PS_SRST_B	System reset

Table 18: Reset Resources

Please note that PS_POR# is automatically asserted if PWR_GOOD is low.

2.14 LEDs

There are four active-low user LEDs on the Mars XU3 SoC module - two of them are connected to both PS and PL and two of them are connected to PS only. On revision 1 modules, all LEDs are connected to both PL and PS.

For the LEDs that can be driven from both PL and PS, it is recommended to drive the FPGA pins to a high impedance state before driving the PS pins and vice versa.

PS Signal Name	PS Signal Location	PL Signal Name	PL Signal Location	Remarks
PS_LED0#	V4 (MIO7)	LED0#	P2	User function/active-low
PS_LED1#	V3 (MIO8)	LED1#	N3	User function/active-low
PS_LED2#	V5 (MIO9)	-[11]	-[11]	User function/active-low
PS_LED3#	AB5 (MIO23)	-[12]	-[12]	User function/active-low

Table 19: LEDs

2.15 DDR4 SDRAM

There is a single DDR4 SDRAM channel on the Mars XU3 SoC module attached directly to the PS side and is available only as a shared resource to the PL side.

The DDR4 SDRAM is connected to PS I/O bank 504. Two 16-bit memory chips are used to build an 32-bit wide memory.

The maximum memory bandwidth on the Mars XU3 SoC module is:
1066 Mbit/sec × 32 bit = 4264 MB/sec

2.15.1 DDR4 SDRAM Type

Table 20 describes the memory availability and configuration on the Mars XU3 SoC module.

[11] LED2# is connected in parallel to PL, FPGA package pin H3, on revision 1 modules.
[12] LED3# is connected in parallel to PL, FPGA package pin F4, on revision 1 modules.

Module	SDRAM Type	Density	Configuration	Manufact.
MA-XU3-D10 (extended)	MT40A256M16GE-083E	4 Gbit	256 M × 16 bit	Micron
MA-XU3-D10 (extended)	H5AN4G6NAFR-UHC	4 Gbit	256 M × 16 bit	SK Hynix
MA-XU3-D10 (industrial)	MT40A256M16GE-083E-IT-B	4 Gbit	256 M × 16 bit	Micron
MA-XU3-D10 (industrial)	K4A4G165WE-BIRC	4 Gbit	256 M × 16 bit	Samsung
MA-XU3-D11 (industrial)	K4A8G165WB-BIRC	8 Gbit	512 M × 16 bit	Samsung

Table 20: DDR4 SDRAM Types

Warning!

Other DDR4 memory devices may be equipped in future revisions of the Mars XU3 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

In custom configurations up to 4 GB of SDRAM memory may be equipped on the module.

2.15.2 Signal Description

Please refer to the Mars XU3 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

2.15.3 Termination

Warning!

No external termination is implemented for the data and command signals on the Mars XU3 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR4 SDRAM device.

2.15.4 Parameters

Please refer to the Mars XU3 SoC module reference design [2] for DDR4 settings guidelines.

The DDR4 SDRAM parameters to be set in the Vivado project are presented in Table 21. The values given in Table 21 are for reference only. Depending on the equipped memory device on the Mars XU3 SoC module and on the DDR4 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory type	DDR4
DRAM bus width	32 bit
ECC	Disabled
DRAM chip bus width	16 bits
DRAM chip capacity	4096-8192 Mbits
Bank group address count	1
Rank address count	0
Bank address count	2
Row address count	15-16
Column address count	10
Speed bin	DDR4 1600J
Operating frequency	533 MHz
CAS latency	10
CAS write latency	9
Additive latency	0
RAS to CAS delay	10
Precharge time	10
tRC	47.5 ns
tRASmin	35 ns
tFAW	30 ns

Table 21: DDR4 SDRAM Parameters

2.16 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.16.1 QSPI Flash Type

Table 22 describes the memory availability and configuration on the Mars XU3 SoC module.

As there is one QSPI flash chip equipped on the Mars XU3 SoC module, type “single” must be selected when programming the flash from Vivado tools.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 22: QSPI Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mars XU3 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.16.2 Signal Description

The QSPI flash is connected to the PS MIO pins 0-5. Some of these signals are available on the module connector, allowing the user to program the QSPI flash from an external source.

The reset of the QSPI flash is connected to the PS_POR#_LV power-on reset signal.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the MPSoC and the flash device.

2.16.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, please refer to the flash device datasheet.

Note that the "Feedback Clk" option on pin MIO6 must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

Please refer to Zynq UltraScale+ MPSoC Technical Reference Manual [19] for details on booting from the QSPI flash.

2.16.4 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [25], [26].

2.17 eMMC Flash

The eMMC flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.17.1 eMMC Flash Type

Table 23 describes the memory availability and configuration on the Mars XU3 SoC module.

Module	Flash Type	Size	Manufacturer
MA-XU3 - R1	H26M41204HPR	8 GB	SK Hynix
MA-XU3 - R2 and newer	H26M52208FPRI	16 GB	SK Hynix
MA-XU3 - R2 and newer	EMMC16G-W525-X01U	16 GB	Kingston
MA-XU3 - R2 and newer	EMMC16G-IB29-PZ90	16 GB	Kingston

Table 23: eMMC Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mars XU3 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.17.2 Signal Description

The eMMC flash signals are connected to the MIO pins 13-22 for 8-bit data transfer mode. The command signal has a 4.7 kΩ pull-up resistor to 1.8 V and the data lines have 47 kΩ pull-up resistors to 1.8 V.

2.18 SD Card

An SD card can be connected to the PS MIO pins 45-51. The corresponding MIO pins are available on the module connector. Information on this boot mode is available in Section 3.8.

Please note that external pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_MIO, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

For booting from an Ultra High Speed (UHS) SD card, an SD 3.0 compliant level shifter is required on the base board and VCC_CFG_MIO must be set to 1.8 V. Please note that this boot mode has not been tested, but it may be supported in the future.

2.19 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mars XU3 SoC module, connected to the PS via RGMII interface.

2.19.1 Ethernet PHY Type

Table 24 describes the equipped Ethernet PHY device type on the Mars XU3 SoC module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 24: Gigabit Ethernet PHY Type

2.19.2 Signal Description

The Ethernet PHY is connected to ETH 3 controller from the PS I/O bank 501, to MIO signals 64-75. The interrupt output of the Ethernet PHYs is connected to the ETH_INT# (FPGA pin A2) and to the I2C interrupt line routed to the module connector.

2.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.19.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3.

The MDIO signals are mapped to MIO pins 76-77.

2.19.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 25.

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 25: Gigabit Ethernet PHYs Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

2.19.6 RGMII Delays Configuration

The Ethernet PHY is connected directly to the hard MAC controller present in the MPSoC device. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the pad skew delays as specified in Table 26. These values have been successfully tested on Enclustra side.

The delays can be adjusted by programming the RGMII pad skew registers of the Ethernet PHY; please refer to the PHY datasheet for details.

PHY Register Name	Register Value [binary]	Delay Value
RXD0-RXD3	0111	0 ps
RX_DV	0111	0 ps
RX_CLK	01111	0 ps
TXD0-TXD3	0111	0 ps
TX_EN	0111	0 ps
GTX_CLK	11110	900 ps

Table 26: Gigabit Ethernet PHYs Configuration - RGMII Delays

2.20 USB 2.0

The Mars XU3 SoC module has an on-board USB 2.0 PHY connected to the MPSoC device, to the PS to I/O bank 502. The USB interface can be configured for USB host, USB device and USB On-The-Go (host and device capable) operations.

2.20.1 USB PHY Type

Table 27 describes the equipped USB PHY device type on the Mars XU3 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 27: USB 2.0 PHY Type

2.20.2 Signal Description

The ULPI interface is connected to MIO pins 52-63 for use with the integrated USB controller.

Warning!
When generating the FSBL in certain SDK versions the power management of the USB interface is not done properly, causing the USB interface not to work as expected. A patch to psu_init.c file fixing this issue (required for SDK 2017.4) is available upon request.

2.21 USB 3.0

Xilinx Zynq Ultrascale+ devices feature two built-in USB 3.0 controllers and PHYs, configurable as host or device. The PHY interface used by the USB 3.0 controller is PIPE3, supporting a 5 Gbit/sec data rate in host or device modes. The interface of each USB 3.0 controller uses one of the PS GTR lanes.

A 100 MHz differential clock is available on the module and connected to PS_MGTREFCLK2 pins, to be used as a reference clock for the USB 3.0 interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in USB 2.0/3.0 controller and on the usage of the PS GTR lanes are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [19] and in the Zynq UltraScale+ MPSoC Overview [23].

Figure 10 shows an example of a USB 3.0 implementation using the built-in Xilinx USB 3.0 interface and the USB 2.0 signals from the PHY, all routed to a USB 3.0 connector on the base board.

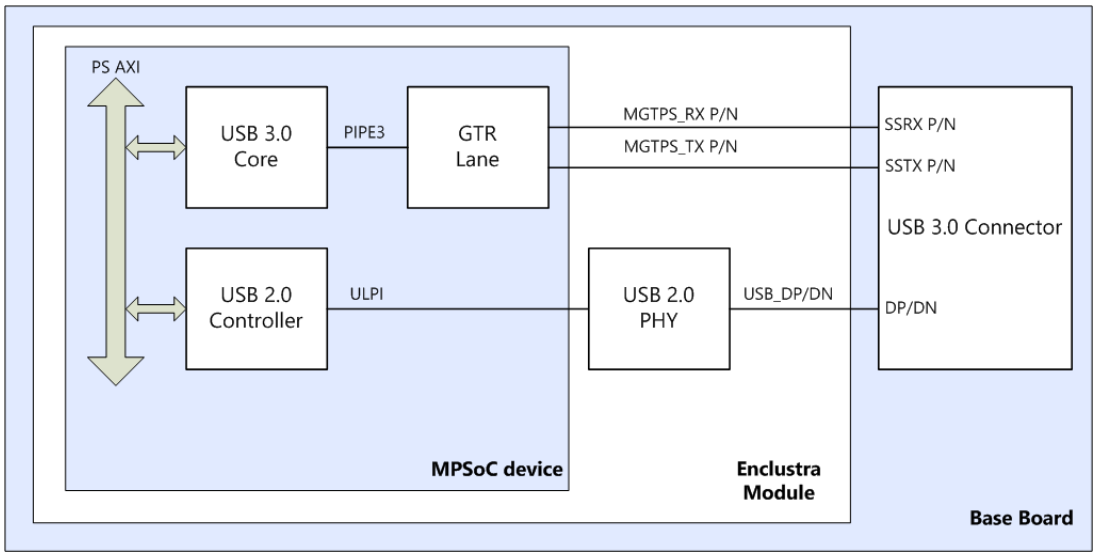

Figure 10: USB 3.0 Implementation Example

2.22 Display Port

Xilinx Zynq Ultrascale+ devices feature two built-in DisplayPort controllers and PHYs, supporting up to two lanes at a 5.4 Gbit/sec line rate. Each lane is represented by one of the PS GTR lines, available on the module connector.

Warning!

The maximum bandwidth of the GTR transceivers on the Mars XU3 SoC module is limited to 5 Gbit/sec by the module connector. For DisplayPort implementation, a link rate of 2.7 Gbit/sec per lane may be used.

A 27 MHz differential clock is available on the module and connected to PS_MGTREFCLK3 pins, to be used as a reference clock for the DisplayPort interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in DisplayPort controller and on the usage of the PS GTR lanes is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [19] and in the Zynq UltraScale+ MPSoC Overview [23].

2.23 Real-Time Clock (RTC)

Zynq Ultrascale+ devices include an internal real-time clock. The internal RTC can be accessed by the platform management unit (PMU) - more information on the PMU is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

The RTC crystal pad input and crystal pad output are connected on the Mars XU3 SoC module to a 32.768 kHz oscillator.

A 1.5 V LDO[13] is used to generate the battery voltage for the built-in RTC (supplied to VCC_PSBATT pin), based on the VCC_BAT voltage mapped to the module connector. This pin can be connected directly to a 3 V battery on the base board. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

2.24 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data. Please refer to Section 4.4 for details on the content of the EEPROM.

2.24.1 EEPROM Type

Table 28 describes the equipped EEPROM device type on the Mars XU3 SoC module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Atmel
DS28CN01 (assembly option)	Maxim

Table 28: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mars XU3 SoC module reference design [2].

[13] Starting with revision 3 modules use a 1.5 V LDO, earlier revisions use a 1.2 V LDO.

3 Device Configuration

3.1 Configuration Signals

The PS of the MPSoC needs to be configured before the FPGA logic can be used. Xilinx Zynq devices need special boot images to boot from QSPI flash, eMMC flash or SD card. For more information, please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

Table 29 describes the most important configuration pins and their location on the module connector. These signals allow the MPSoC to boot from QSPI flash, eMMC flash or SD card, and can be used to program the QSPI flash from an external master. Please refer to Section 3.11 for details.

Signal Name	MPSoC Pin Type	Mod. Conn. Pin	Description	Comments
FLASH_CLK	MIO0	182	SPI CLK	4.7 kΩ pull-up to VCC_CFG_MIO
FLASH_DO	MIO1	184	SPI MISO	4.7 kΩ pull-up to VCC_CFG_MIO
FLASH_DI	MIO4	186	SPI MOSI	4.7 kΩ pull-up to VCC_CFG_MIO
FLASH_CS#	MIO5	188	SPI CS#	4.7 kΩ pull-up to VCC_CFG_MIO
PS_DONE	PS_DONE	194	MPSoC device configuration done	1 kΩ pull-up to VCC_CFG_MIO
PS_POR#	PS_POR_B	196	MPSoC power-on reset	4.7 kΩ[14] pull-up to VCC_CFG_MIO
PS_SRST#	PS_SRST_B	192	MPSoC system reset	4.7 kΩ[14] pull-up to VCC_CFG_MIO
BOOT_MODE0	-	190	Boot mode selection	4.7 kΩ[14] pull-up to VCC_CFG_MIO
BOOT_MODE1	-	170	Boot mode selection	4.7 kΩ[14] pull-up to VCC_CFG_MIO

Table 29: MPSoC Configuration Pins

[14] Starting with revision 3 modules use 4.7 kΩ pull-up resistors, earlier revisions use 10 kΩ.

Warning!

All configuration signals except for BOOT_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped MPSoC device, as well as other devices on the Mars XU3 SoC module.

3.2 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to GND on the module; as PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing R204 component and by mounting R203 - in this configuration the PUDC pin is connected to 1.8 V.

Figure 11 illustrates the configuration of the I/O signals during power-up. Figure 12 indicates the location of the pull-up/pull-down resistors on the module PCB - upper middle part on the bottom view drawing.

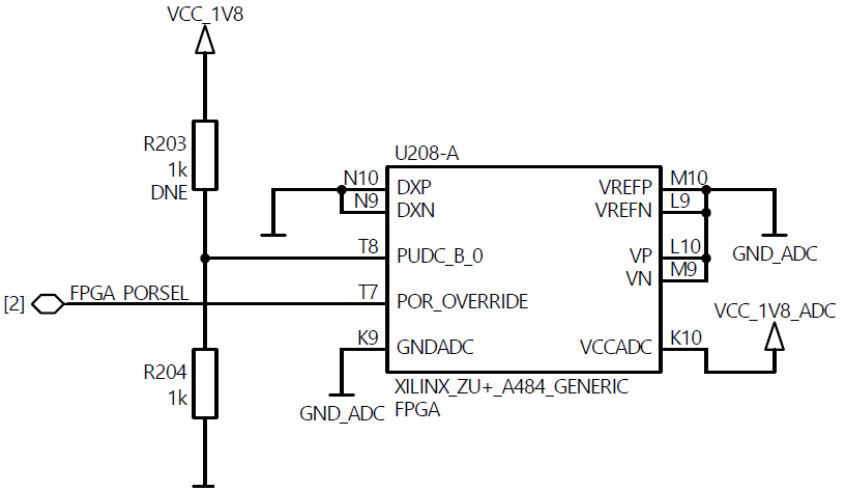

Figure 11: Pull-Up During Configuration (PUDC)

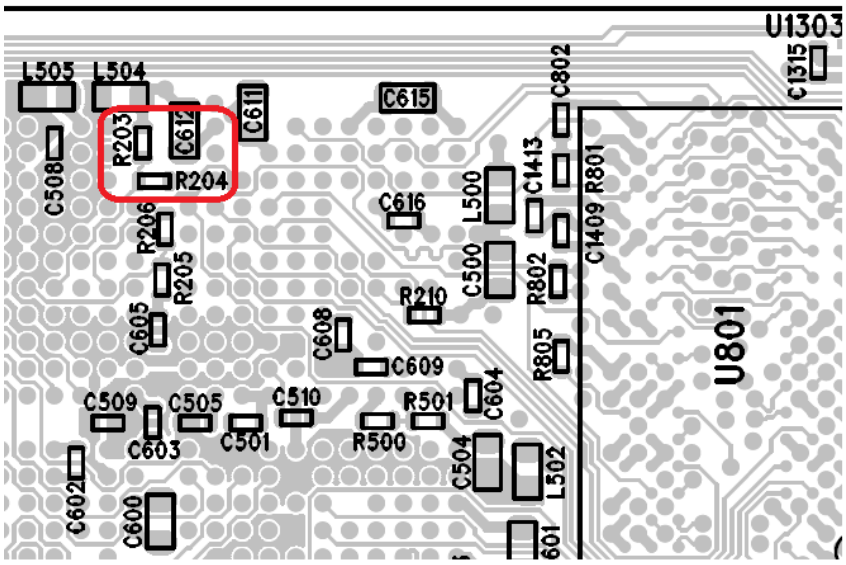

Figure 12: Pull-Up During Configuration (PUDC) Resistors - Assembly Drawing Bottom View (upper middle part)

For details on the PUDC signal please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

3.3 Power-on Reset Delay Override

The power-on reset delay override MPSoC signal (POR_OVERRIDE) is pulled to GND on the module, setting the PL power-on delay time to the default standard time.

If the application requires faster PL power-on delay time, this can be achieved by removing R206 component and by mounting R205.

Figure 13 illustrates the configuration of the I/O signals during power-up. Figure 14 indicates the location of the pull-up/pull-down resistors on the module PCB - upper middle part on the bottom view drawing.

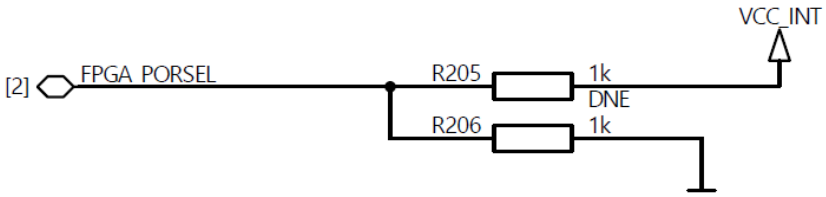

Figure 13: Power-on Reset Delay Override (PORSEL)

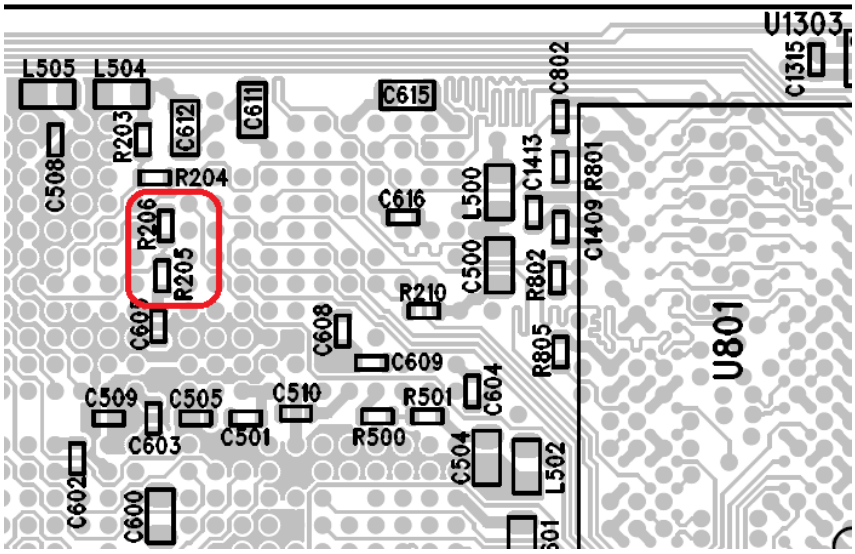

Figure 14: Power-on Reset Delay Override (PORSEL) Resistors - Assembly Drawing Bottom View (upper middle part)

For details on the POR_OVERRIDE signal please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

3.4 Boot Mode

The boot mode can be selected via two signals available on the module connector.

Table 30 describes the available boot modes on the Mars XU3 SoC module.

BOOT MODE1	BOOT MODE0	Mode Straps [3:0]	Description	Remarks
0	0	0110	Boot from eMMC flash	-
0	1	1110	Boot from SD card (with an external SD 3.0 compliant level shifter; only available when VCC_CFG_MIO is 1.8 V)	Not supported (may be supported in the future)
1	0	0010	Boot from QSPI flash	-
1	1	0101	Boot from SD card (default mode)	-
1	0	0000	Boot from JTAG	Available only starting with revision 3 modules in certain conditions (refer to Section 3.5.3 for details).

Table 30: Boot Modes

3.5 JTAG

The Zynq Ultrascale+ devices include two separate JTAG controllers: the Zynq Ultrascale+ TAP and the ARM DAP. The first one uses the PS dedicated JTAG pins and has access to both PS and PL and the second one uses the PS PJTAG pins and is used for loading programs, system test, and PS debug.

Details on JTAG and on system test and debug are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

Certain Xilinx tool versions support QSPI flash programming via JTAG only when JTAG boot mode is used. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

3.5.1 JTAG on Module Connector

The PL and the PS JTAG interfaces are connected into one single chain available on the module connector. The PS_JTAG pins are used by the Zynq Ultrascale+ TAP controller - the controller has full functionality only after the PS boot is complete. In order to enable the ARM DAP controller, special commands must be sent to the Zynq Ultrascale+ TAP.

The MPSoC device and the flash devices can be configured via JTAG from Xilinx SDK or Xilinx Vivado Hardware Manager - for this operation, the ARM DAP must be enabled.

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	158	4.7 kΩ[15] pull-up to VCC_CFG_MIO
JTAG_TMS	162	4.7 kΩ[15] pull-up to VCC_CFG_MIO
JTAG_TDI	160	4.7 kΩ[15] pull-up to VCC_CFG_MIO
JTAG_TDO	164	4.7 kΩ[15] pull-up to VCC_CFG_MIO

Table 31: JTAG Interface

3.5.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_MIO.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.5.3 JTAG Boot Mode

Starting with revision 3, support for JTAG boot mode has been added to increase the usability of the module with Xilinx tools, for example for QSPI flash programming or FPGA bitstream loading.

The following steps are required in order to boot the module in JTAG mode:

- Set the boot mode selection signals for QSPI boot
- Short-circuit R202 (see Figure 15) while powering-up the module (in order to sample the MPSoC boot selection pins correctly for JTAG boot mode)

[15] Starting with revision 3 modules use 4.7 kΩ pull-up resistors, earlier revisions use 10 kΩ.

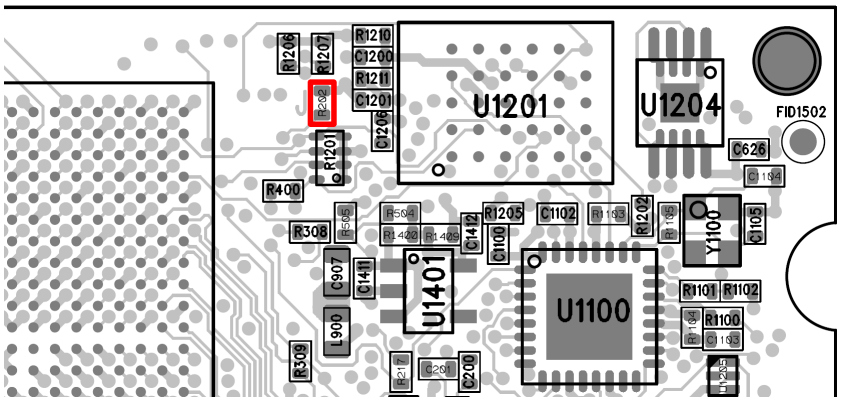

Figure 15: JTAG Boot Mode Resistor - Assembly Drawing Top View (top right part) for Revision 3 Modules

3.6 eMMC Boot Mode

In the eMMC boot mode, the PS boots from the eMMC flash located on the module. The flash device is connected to the PS MIO pins 13-22 for 8-bit data transfer mode.

3.7 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 0-5.

3.8 SD Card Boot Mode

In the SD card boot mode the PS boots from the SD card located on the base board. There are two SD card boot modes available on the Mars XU3 SoC module. Please note that the SD boot mode with level shifter is currently not supported.

The SD boot mode with level shifter is used with Ultra High Speed (UHS) SD cards. The controller will start the communication at 3.3 V and afterwards it will command the card to drop from 3.3 V operation to 1.8 V operation. For this mode, an external SD 3.0 compliant level shifter is required. This boot mode may be supported in the future by Enclustra modules and base boards.

BOOT_MODE1	BOOT_MODE0	Description	VCC_CFG_MIO
0	1	Boot from SD card (with an external SD 3.0 compliant level shifter; currently not supported)	1.8 V
1	1	Boot from SD card (default mode)	Refer to Section 2.9.5

Table 32: SD Card Boot Modes

For the SD card boot mode, the following requirements must be met:

- The SD card must be connected to MIO pins 45-51
- A Zynq boot image must be generated from an MPSoC design having the SDIO controller enabled
- The boot image must be named "boot.bin" and then copied to the SD card
- The SDIO controller must be fed with a reasonable clock frequency. Please refer to the reference design for guidelines on SDIO settings.

For details on SD card boot, please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [19].

3.9 eMMC Flash Programming

The eMMC flash can be formatted and/or programmed in u-boot or Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

Certain Xilinx tool versions support eMMC flash programming via JTAG.

3.10 QSPI Flash Programming via JTAG

The Xilinx Vivado and SDK software offer QSPI flash programming support via JTAG.

Certain Xilinx tools versions support QSPI flash programming via JTAG only when JTAG boot mode is used. For more information, please refer to the Xilinx documentation [19] and support. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

3.11 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the MPSoC device as well, the MPSoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the PS_SRST# signal to GND followed by a pulse on PS_POR#, which puts the MPSoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Figure 16 shows the signal diagrams corresponding to flash programming from an external master.

In addition, a non-QSPI boot mode must be used during QSPI flash programming, otherwise the MPSoC device will attempt to boot from the flash and will disturb the clock.

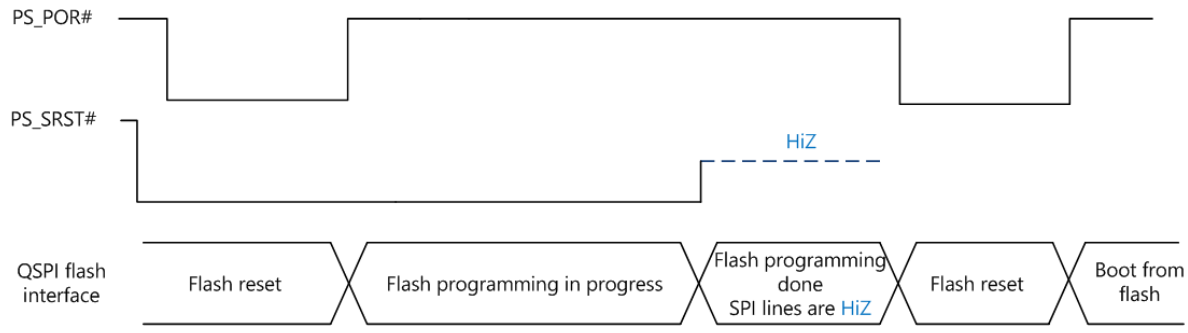

Figure 16: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the MPSoC device into reset may damage the equipped MPSoC device, as well as other devices on the Mars XU3 SoC module.

3.12 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using Enclustra Module Configuration Tool (MCT) [17]. For this method, a non-QSPI boot mode must be used during QSPI flash programming. The entire procedure is described in the reference design documentation, and is only available starting with revision 2 modules.

Please note that the Xilinx Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mars XU3 SoC module.

4 I2C Communication

4.1 Overview

The I2C bus on the Mars XU3 SoC module is connected to the MPSoC device and to the EEPROM, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 33 describes the signals of the I2C interface - the pins are connected to the PS. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the MPSoC and must not be driven from the MPSoC device.

Starting with revision 2 modules, the I2C bus is connected to both PS and PL sides (and not only to the PS), to offer extra flexibility and help on future development. I2C on PL side is functional only when the VCC_IO_B65 voltage is 1.8 V.

Level shifters are used between the I2C bus and MPSoC pins, as I/O banks 500 and 65 are supplied with 1.8 V. Please make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	PS Pin	PL Package Pin	Connector Pin	Resistor
I2C_SDA	MIO11	F4	176	2.2 kΩ pull-up
I2C_SCL	MIO10	H3	178	2.2 kΩ pull-up
I2C_INT#	MIO12	-	174	4.7 kΩ pull-up

Table 33: I2C Signal Description

4.3 I2C Address Map

Table 34 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.24)

Table 34: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mars XU3 SoC module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 35: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mars XU3 SoC module	0x0330	0x[XX]	0x[YY]	0x0323 [XX][YY]

Table 36: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	MPSoC type	0	3	See MPSoC type table (Table 38)
	3-0	MPSoC device speed grade	0	3	See MPSoC speed grade table (Table 39)
0x09	7-6	Temperature range	0	2	See temperature range table (Table 40)
	5	Power grade	0 (Normal)	1 (Low power)	
	4-3	Gigabit Ethernet port count	0	1	
	2-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	1	
0x0B	7-4	DDR4 RAM size (GB)	0 (0 GB)	3 (4 GB)	Resolution = 1 GB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
0x0C	7-4	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1 GB
	3-0	Reserved	-	-	

Table 37: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 1 GB, DRAM=2: 2 GB, DRAM=3: 4 GB, etc).

Table 38 shows the available MPSoC types.

Value	MPSoC Device Type
0	XCZU3EG ES
1	XCZU2EG
2	XCZU2CG
3	XCZU3EG

Table 38: MPSoC Device Types

Table 40 shows the available MPSoC speed grades.

Value	MPSoC Speed Grade
0	1L
1	1
2	2
3	3

Table 39: MPSoC Speed Grades

Table 40 shows the available temperature ranges.

Value	Module Temperature Range
0	Commercial
1	Extended
2	Industrial

Table 40: Module Temperature Range

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 41 indicates the absolute maximum ratings for Mars XU3 SoC module. The values given are for reference only; for details please refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [21].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 6	V
VCC_3V3	3.3 V supply voltage relative to GND	-0.5 to 3.6	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	0 to 5.5	V
VCC_IO_B26	Output drivers supply voltage relative to GND	-0.5 to 3.4	V
VCC_CFG_MIO	Output drivers supply voltage relative to GND	-0.5 to 3.63	V
VCC_IO_B65	Output drivers supply voltage relative to GND	-0.5 to 2.0	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.55	V
V_ADC	Analog I/O input voltage for the ADC	-0.5 to 2.3	V
Temperature	Temperature range for commercial modules (C)*	0 to +70	°C
	Temperature range for industrial modules (I)*	-40 to +85	°C

Table 41: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 42 indicates the recommended operating conditions for Mars XU3 SoC module. The values given are for reference only; for details please refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [21].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	3.0 to 5.5	V
VCC_3V3	3.3 V supply voltage relative to GND	3.15 to 3.45	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	2.0 to 5.5	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
V_ADC	Analog I/O input voltage for the ADC	0 to 1.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 42: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

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