6A, 23V, 500kHz, ACOT™ Synchronous Buck Converter

General Description

The RT6220DH is a synchronous Buck converter with Advanced Constant On-Time (ACOT™) mode control, which provides a very fast transient response with no external compensators. The RT6220DH operates from 4.5V to 23V input voltage, provides complete protection functions including Over Current Protection (OCP), Under Voltage Protection (UVP) and Over Voltage Protection (OVP). This IC also provides a 1.5ms internal soft-start function and an open-drain power good indicator.

Ordering Information

RT6220DH□□

- Package Type
  QUF : UQFN-16L 3x3 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

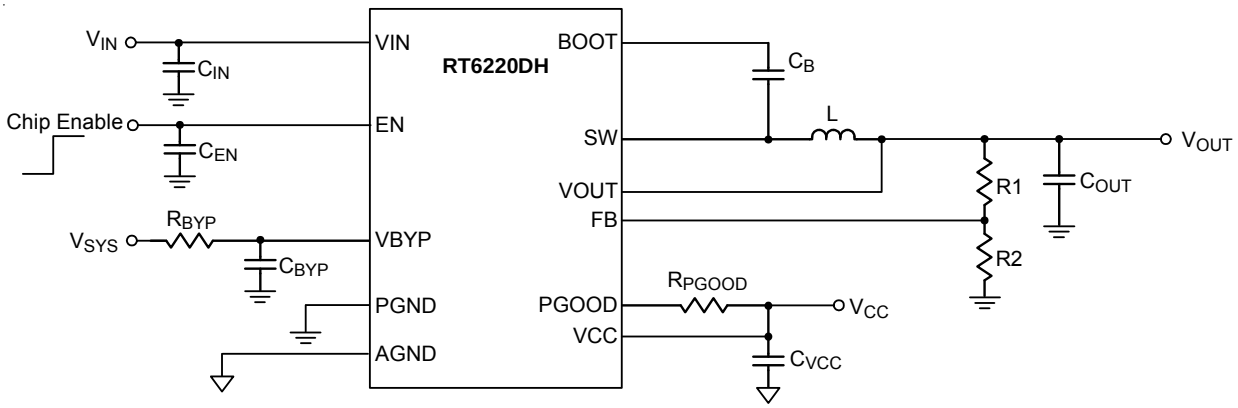
Features

- **4.5V to 23V Input Voltage Range**
- **Adjustable from 0.6V to 5V Output Range**
- **500kHz Switching Frequency**
- **ACOT™ Mode Performs Fast Transient Response**
- **Integrated MOSFETs**
  - **31mΩ of High-Side MOSFET**
  - **20mΩ of Low-Side MOSFET**
- **Supports MLCC Output Capacitors**
- **Internal Soft-Start (1.5ms typ)**
- **Built-in OVP/UVP/OCP**
- **Power Good Indicator**
- **Thermal Shutdown**

Applications

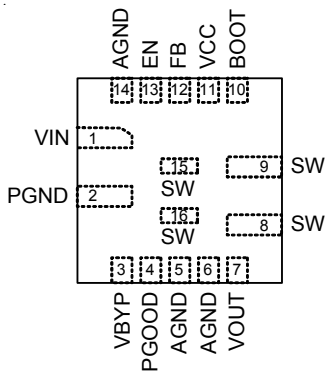
- Laptop Computers
- Tablet PCs
- Networking Systems
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

Simplified Application Circuit



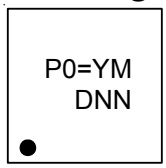
Pin Configuration

(TOP VIEW)



UQFN-16L 3x3 (FC)

Marking Information



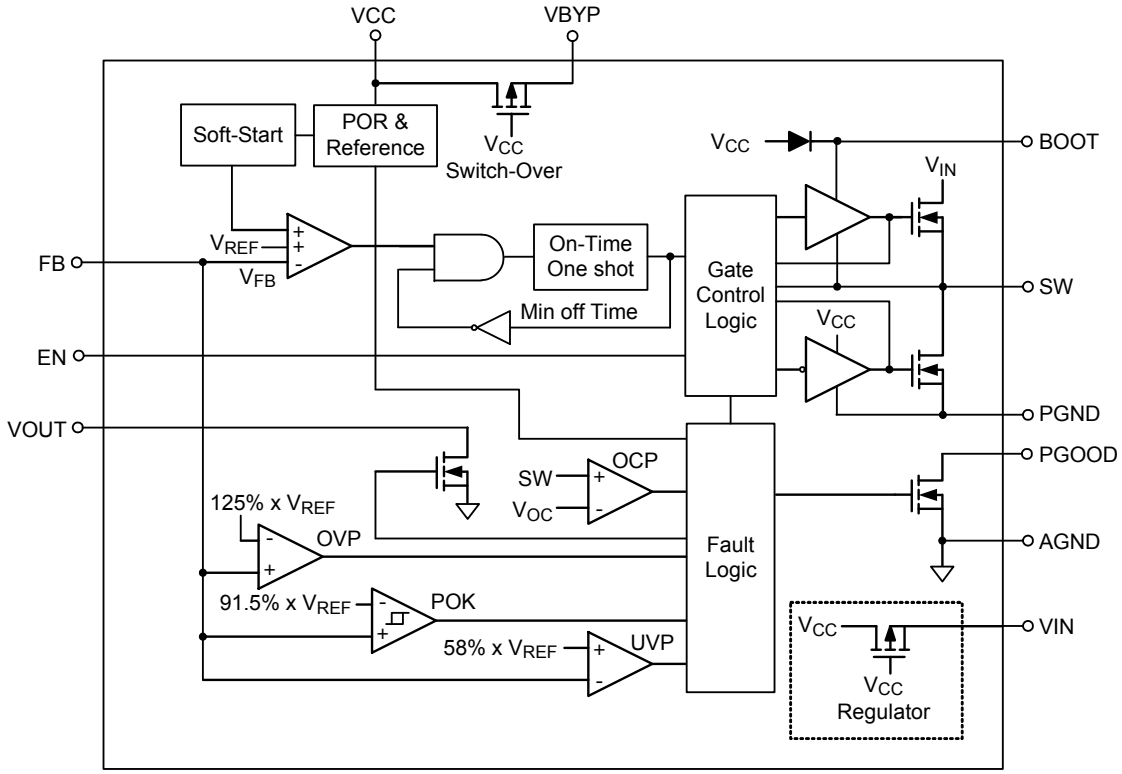
P0= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Power input connect to high-side MOSFET drain.
2	PGND	Power ground.
3	VBYP	Switch over input supply voltage for VCC. A low pass filter should be connected to AGND, if VBYP is applied. If VBYP is not used, then connect to AGND. Do not connect to VCC pin.
4	PGOOD	Open-drain power good indicator output.
5, 6, 14	AGND	Analog ground.
7	VOUT	Output voltage sense input. An internal discharging circuit is connected to this pin.
8, 9, 15, 16	SW	Switch node.
10	BOOT	Bootstrap supply for high-side gate driver. A capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BOOT pins to form a floating supply across the power switch driver.
11	VCC	5V linear regulator output for internal control circuit. Bypass V_{CC} to AGND with a 2.2μF capacitor. V_{CC} can only supply internal circuits. Do not connect to external loads.
12	FB	Feedback voltage input.
13	EN	Enable control input. Do not leave this pin floating. The slew rate of EN is recommended to be slower than 4.8V/μs.

Functional Block Diagram



Operation

Overall

The RT6220DH is a synchronous step-down converter with advanced constant on-time control mode. Using the ACOT™ control mode can reduce the output capacitance and provide fast transient response. It can minimize the component size without additional external compensation network.

Internal VCC Regulator

The regulator provides 5V power to supply the internal control circuit. Connecting a 2.2μF ceramic capacitor for decoupling and stability is required.

Soft-Start

In order to prevent the converter output voltage from overshooting during the startup period, the soft-start function is necessary. The soft-start time is internal setting and the duration is around 1.5ms.

OCP

The inductor valley current is monitored cycle-by-cycle via the internal switches, preventing an on-time until the current drops below the current limit.

Power Good

After soft-start is finished, the power good output goes high. The PGOOD pin is an open-drain output.

VCC Switch-Over

The internal regulator output will switch over to VBYP if VBYP level is higher than 4.6V.

Power Off

There is an internal discharging circuit to discharge the residual charge of output capacitor when converter is power off.

Absolute Maximum Ratings (Note 1)

- VIN to PGND ---------- –0.3V to 27V
- SW to PGND
  - DC ---------- –0.3V to 27.3V
  - AC (<30ns) ---------- –5V to 28V
- BOOT to PGND
  - DC ---------- –0.6V to 33.3V
  - AC (<30ns) ---------- –5V to 34V
- BOOT to SW ---------- –0.3V to 6V
- EN, FB to AGND ---------- –0.3V to 27V
- VBYP to AGND ---------- –0.3V to 5.3V
- VCC, PGOOD, VOUT to AGND ---------- –0.3V to 6V
- PGND to AGND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  - UQFN-16L 3x3 (FC) ---------- 1.4W
- Package Thermal Resistance (Note 2)
  - UQFN-16L 3x3 (FC), θ_{JA} ---------- 70°C/W
  - UQFN-16L 3x3 (FC), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 23V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Shutdown Current		V_{EN} = 0V	--	2.5	5	μA
Quiescent Current		V_{EN} = 2V, no switching	--	110	150	μA
BOOT to SW Leakage Current						
BOOT to SW Leakage Current		V_{BYP} = 5V, V_{EN} = 0V	--	--	2.5	μA
Switch On-Resistance						
Switch On-Resistance	$R_{DS(ON)\_H}$	V_{BOOT} – V_{SW} = 5V	--	31	--	mΩ
	$R_{DS(ON)\_L}$		--	20	--	
High-Side MOSFET Leakage Current	$I_{Leakage\_H}$	V_{IN} = 12V, V_{EN} = 0V	--	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit						
Current Limit	I_{LIM}	Valley current of low-side switch	7.6	--	11.4	A
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}		450	500	550	kHz
Minimum Off-Time	t_{OFF_MIN}		--	200	--	ns
Protections						
OVP Trip Threshold	V_{OVP}	With respect to output voltage	120	125	130	%
OVP Propagation Delay	t_{OVPDLY}		--	5	--	μs
UVP Trip Threshold	V_{UVP}	With respect to output voltage	53	58	63	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	μs
Reference and Soft-Start						
Feedback Reference Voltage	V_{REF}		0.594	0.600	0.606	V
Soft-Start Time	t_{SS}	From EN high to PGOOD high	1	1.5	2	ms
Enable and UVLO						
EN Input High Voltage	V_{ENH}		1.25	1.35	1.45	V
EN Hysteresis	V_{ENHYS}		50	200	250	mV
EN Input Current	I_{EN}	V_{EN} = 2V	--	1	--	μA
		V_{EN} = 0V	--	0	--	
VCC UVLO Rising	V_{CCUVLO}		3.8	4.2	4.45	V
VCC UVLO Hysteresis	V_{CCHYS}		75	400	650	mV
VCC Regulator						
VCC Regulator	V_{VCC}		4.805	5	5.295	V
VCC Switch Over Threshold to VBYP		V_{BYP} rising edge	4.4	4.6	4.8	V
VCC Switch Over Hysteresis			150	200	400	mV
Switch Over On-Resistance			--	3	5	Ω
Power Good Indicator						
PGOOD Threshold From Lower		V_{OUT} rising	86.5	91.5	96.5	%
PGOOD Low Hysteresis		V_{OUT} falling	--	10	--	%
PGOOD Low to High Delay	t_{PGDLY}		--	0.5	--	ms
PGOOD Sink Current Capability	V_{PGSINK}	Sink 4mA	--	--	0.4	V
PGOOD Leakage Current	I_{PGLEAK}	V_{PGOOD} = 5V	--	--	100	nA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	T_J rising	135	150	--	°C
Thermal Shutdown Hysteresis			--	25	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

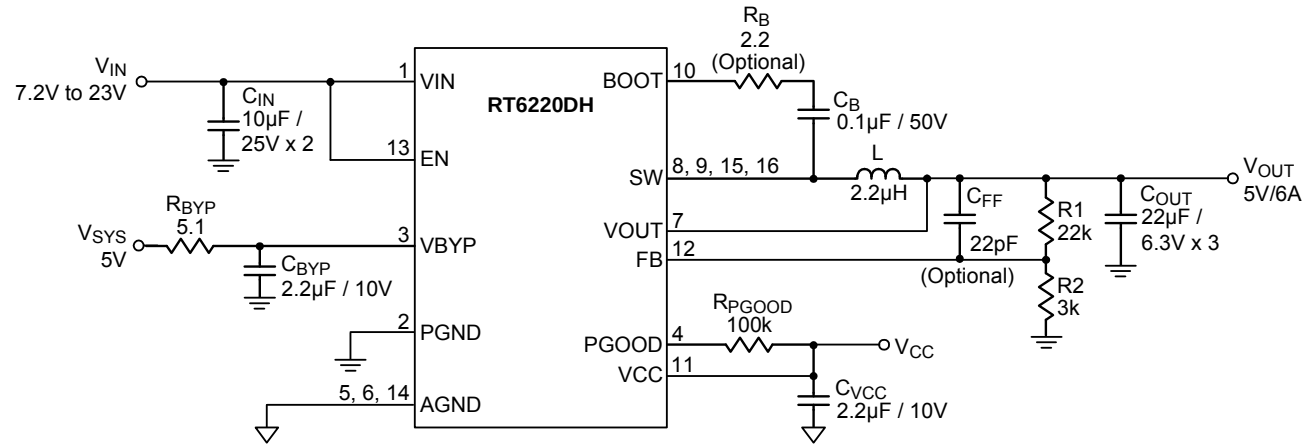


Figure 1. Typical Application Circuit for V_{OUT} = 5V

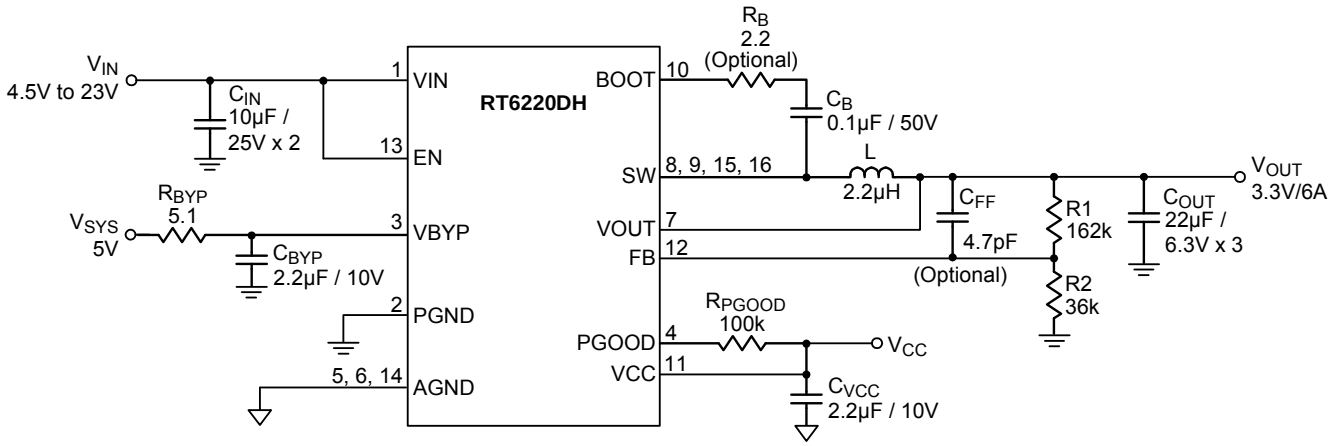


Figure 2. Typical Application Circuit for V_{OUT} = 3.3V

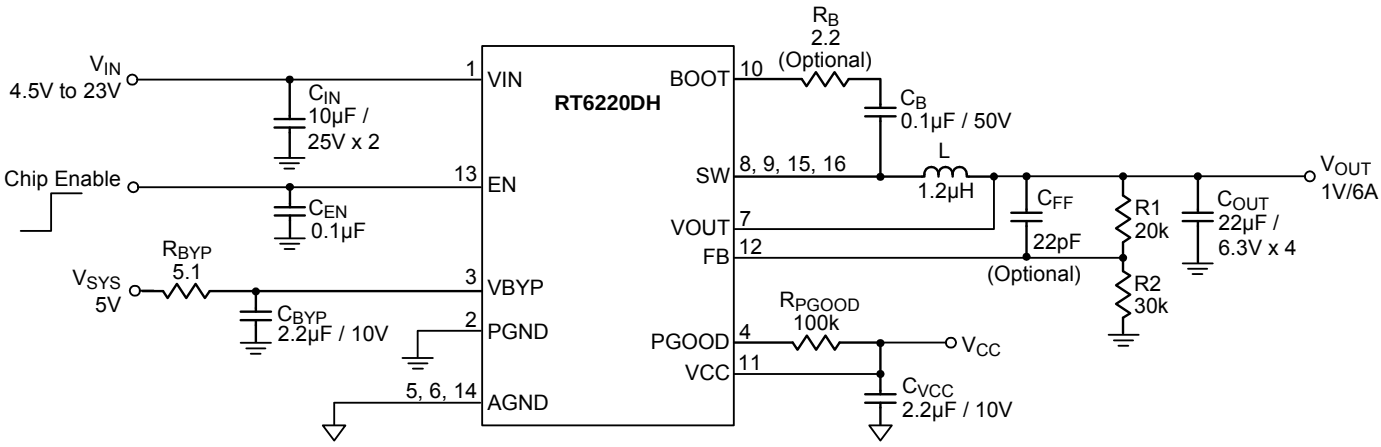
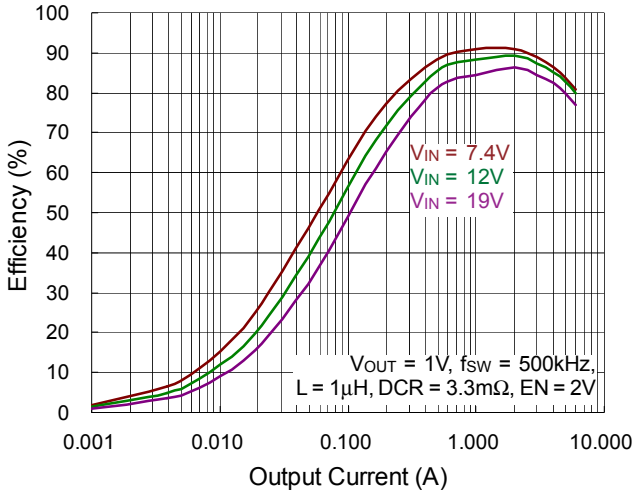


Figure 3. Typical Application Circuit for V_{OUT} = 1V

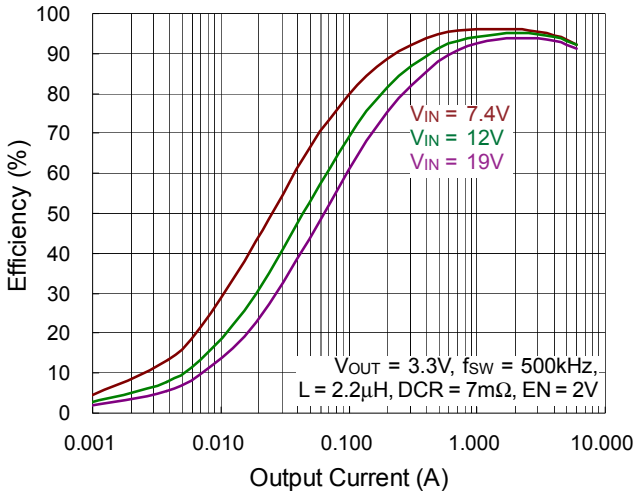
Typical Operating Characteristics

Performance waveforms are tested on the evaluation board of the Typical Application Circuit, V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_J = 25°C, unless otherwise noted.

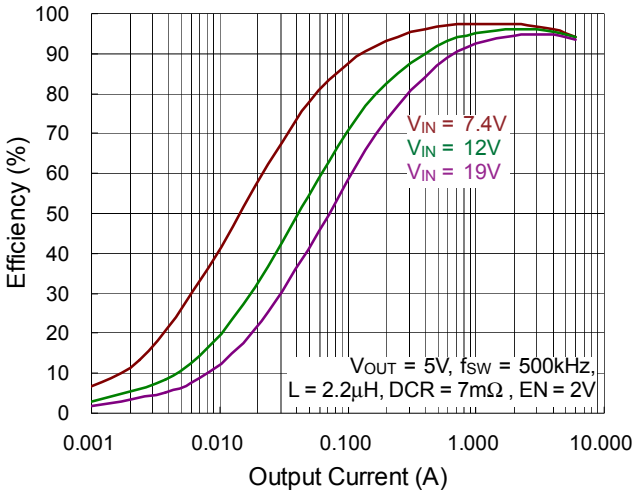
Efficiency vs. Output Current



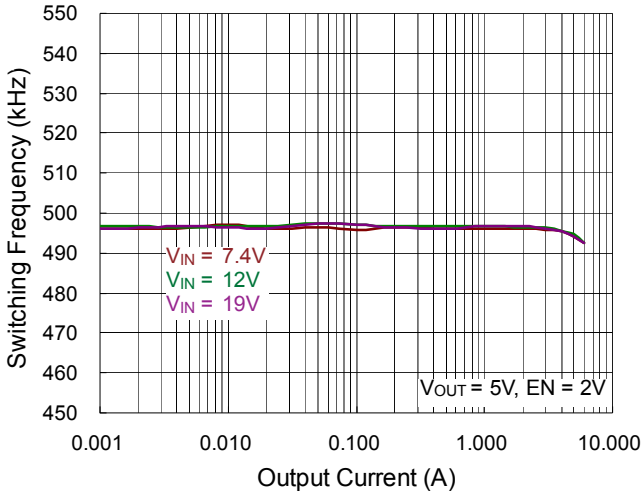
Efficiency vs. Output Current



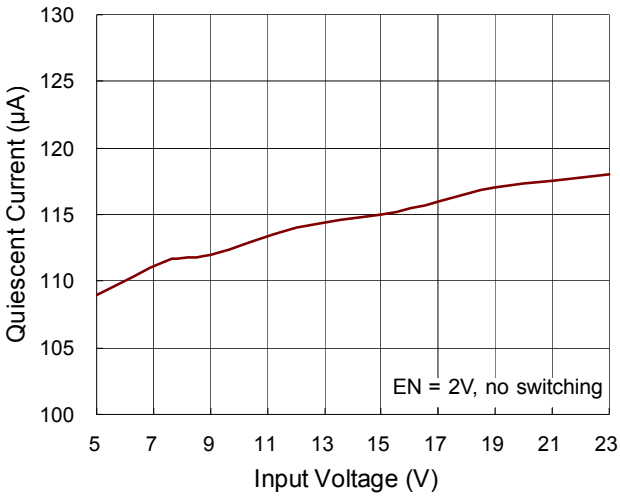
Efficiency vs. Output Current



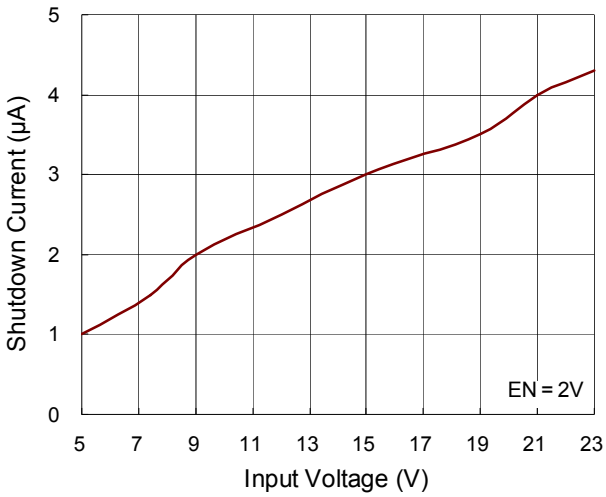
Switching Frequency vs. Output Current



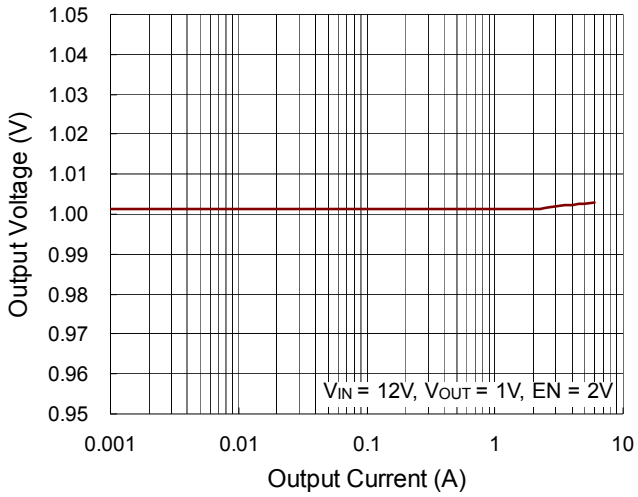
Quiescent Current vs. Input Voltage



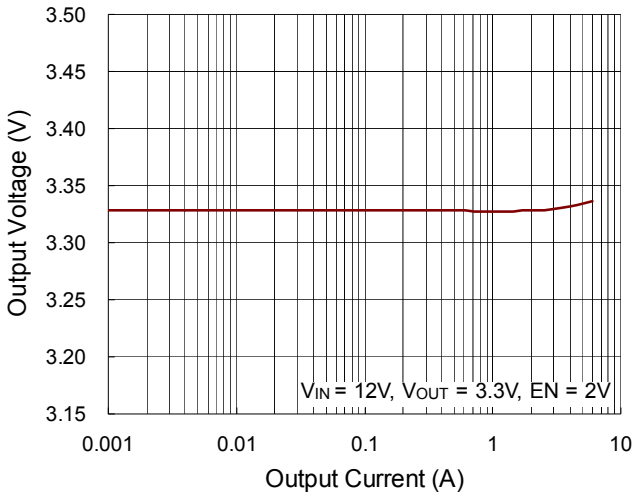
Shutdown Current vs. Input Voltage



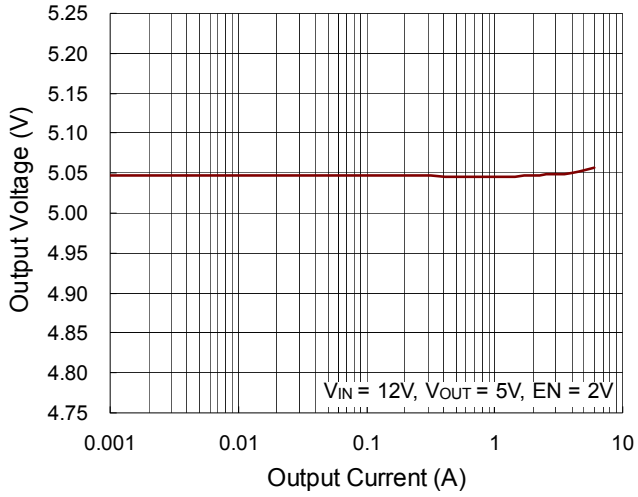
Output Voltage vs. Output Current



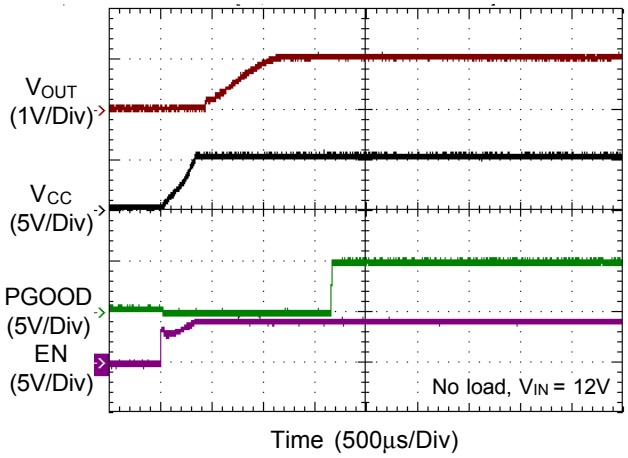
Output Voltage vs. Output Current



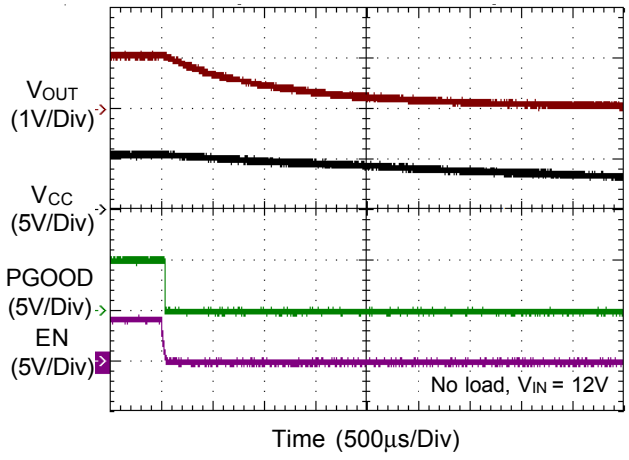
Output Voltage vs. Output Current



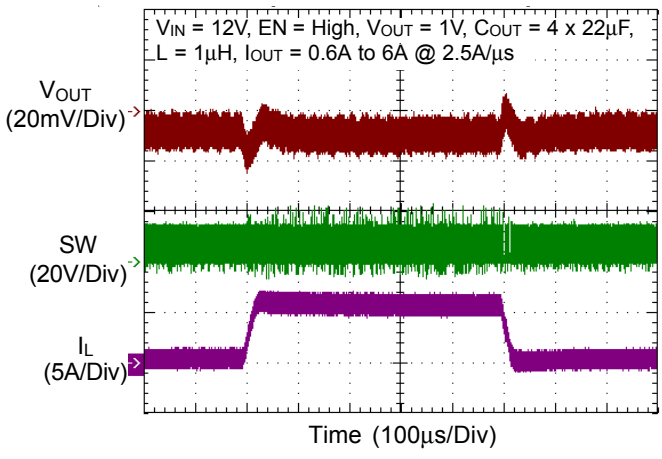
Power On Through EN



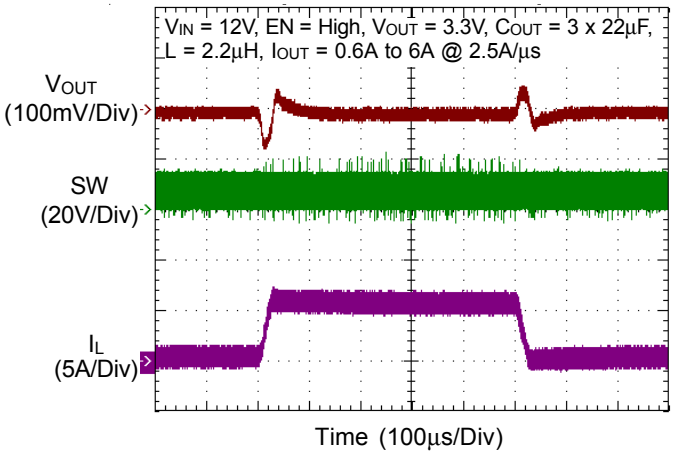
Power Off Through EN



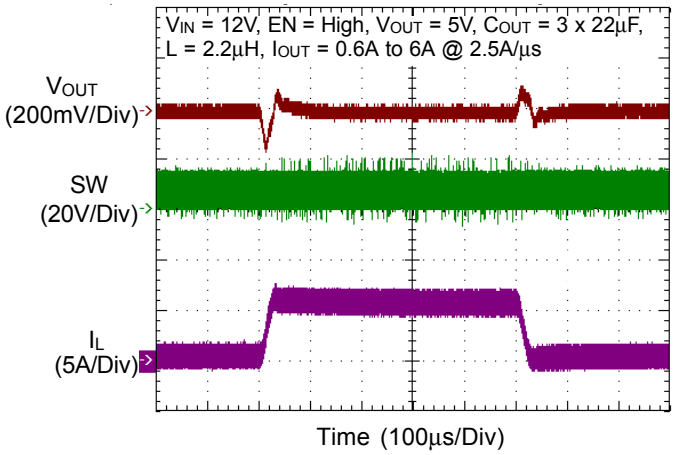
Load Transient Response



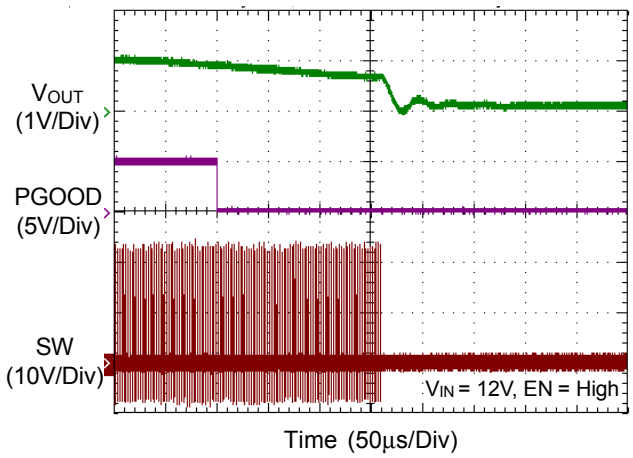
Load Transient Response



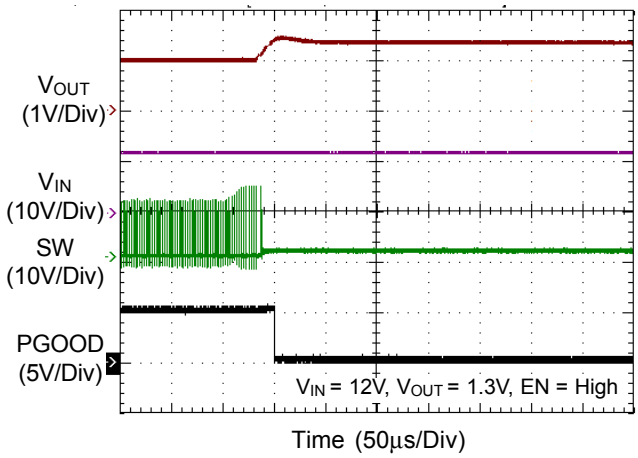
Load Transient Response



UVP



OVP



Application Information

The RT6220DH is high-performance 500kHz 6A step-down regulators with internal power switches and synchronous rectifiers. It features an Advanced Constant On-Time (ACOT™) control architecture that provides stable operation for ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 23V, and the output voltage is adjustable from 0.6V to 5V.

The proprietary ACOT™ control scheme improves conventional constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

ACOT™ Control Architecture

In order to achieve good stability with low-ESR ceramic capacitors, ACOT™ uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

Making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage as sensing input and output voltage. When the load changes, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on-time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. The ACOT™ uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

ACOT™ One-Shot Operation

The RT6220DH control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (200ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Linear Regulators (VCC)

The RT6220DH includes a 5V linear regulator (VCC). The VCC regulator steps down input voltage to supply both internal circuitry and gate drivers. Do not connect the VCC pin to external loads. When PGOOD is pulled high and BYP pin voltage is above 4.6V, an internal 3Ω P-MOSFET switch connects VCC to the BYP pin while the VCC linear regulator is simultaneously turned off.

Current Limit

The RT6220DH current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between Source and Drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the current limit, the on-time one-shot is inhibited until the inductor

current ramps down below the current limit. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level (see next section), the IC will stop switching to avoid excessive heat.

Output Over-Voltage Protection and Under-Voltage Protection

The RT6220DH features an output Over-Voltage Protection (OVP). If the output voltage rises above the regulation level, the IC will stop switching and restart automatically after a short period which is the so-called Hiccup mode. The RT6220DH also features an output Under-Voltage Protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 5μs (typical), the UVP is triggered, and the IC will stop switching and enter the Hiccup mode.

Input Under-Voltage Lockout

In addition to the enable function, the RT6220DH features an Under-Voltage Lockout (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Over-Temperature Protection

The RT6220DH features an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP shuts down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 25°C the IC resumes normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C. Note that the VCC regulator remains on as the OTP is triggered.

Enable and Disable

The enable input (EN) has a logic-low level of 1.15V. When V_{EN} is below this level, the IC enters shutdown mode and supply current drops to less than 5μA (typical). When V_{EN} exceeds its logic-high level (1.35V typical), the IC is fully operational.

Soft-Start

The RT6220DH provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramp of internal reference voltage which is compared with FB signal. And it will correct the output voltage more accurately after soft-start. The typical soft-start duration is 1.5ms.

Power Off

When V_{EN} is pulled to GND or lower than the logic-low level of 1.15V, there is an internal discharging resistor to discharge the residual charge inside the output capacitors. Besides, the value of discharging resistor is about twenty ohms.

Power Good Output (PGOOD)

The power good output is an open-drain output that requires a pull-up resistor. When the output voltage is 20% (typical) below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to 90% of its set voltage once more. During soft-start, PGOOD is actively held low and only allowed to be pulled high after soft-start is over and the output reaches 90% of its set voltage and the PGOOD low to high delay(500μs typical) has passed. There is a 2μs PGOOD high to low delay built into PGOOD circuitry to prevent false triggering.

External Bootstrap Capacitor (C_{BOOT})

Connect a 0.22μF low ESR ceramic capacitor between the BOOT and SW pins. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-MOSFET switch.

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, and slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{SW} rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead-time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense

of some additional power dissipation. The switch turn-on can be slowed by placing a small (<10Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and V_{SW}'s rise.

Setting the Output Voltage

The output voltage of the RT6220DH is adjustable and with valley control. There is an easy way to determine the output voltage only by two resistors, R1 and R2. As the feedback circuit shown in Figure 4. the relation of V_{OUT} and V_{REF} can be derived as V_{OUT} = (1+R1/R2) x V_{REF} readily. Generally, the stability is a serious issue for converter. In order to achieve better performance on stability and transient, a feed-forward capacitor, C_{FF}, is added to increase the noise margin and transient response of loop control. However, there is a tradeoff of adding a feed-forward capacitor. An additional dc offset will be generated on output voltage due to the amplified feedback ripple by feed-forward compensator. This is not always the case that every C_{FF} makes the same value of dc offset, it is based on different pole and zero placement generated by R1, R2 and C_{FF}. For simplicity, a symbol named $V_{dc,offset}$ is supposed to be the value of dc offset. This value may influence the performance (e.g. regulation or peak value of V_{OUT}) of converter slightly, the suggested $C_{FF}$is to select a pair of pole and zero to provide the maximum phase lead at switching frequency.

$$V_{OUT,valley} = \left(1+\frac{R1}{R2}\right)\times V_{REF} + V_{dc,offset}$$

$V_{OUT,valley}$ is the valley of output voltage, and $V_{dc,offset}$ is used for describing the additional dc offset on V_{OUT}, the value is related to the output voltage ripple and C_{FF}.

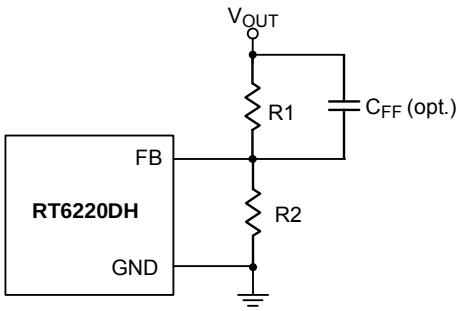


Figure 4. The Equivalent Circuit of Feedback Loop

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response. However, they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times f_{SW}\times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times f_{SW}\times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability. Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. The input capacitor is used to supply the input RMS current, which can be calculated using the following equation :

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1 - \frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{IN}}{C_{IN} \times f_{SW} \times V_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The typical operating circuit is recommended to use two 10μF low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT6220DH is optimized for ceramic output capacitors and best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 500kHz switching frequency. However, some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increases compensations for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Most applications never experience instantaneous full load steps and the RT6220DH's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that over-voltage protection and under-voltage protection will not be triggered.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-16L 3x3 (FC) package, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.4W for a UQFN-16L 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

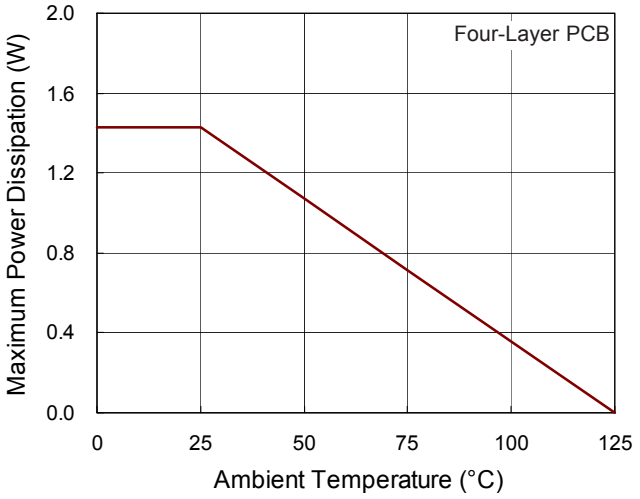


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT6220DH.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and PGND).
- The SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent noise coupling.
- The PGND pin should be connected to a strong ground plane for heat sinking and noise protection.
- Avoid using vias in the power path connections that have switched currents (from C_{IN} to PGND and C_{IN} to V_{IN}) and the switching node (SW).

- The ground of VCC is recommended to connect to GND layer through via.

An example of PCB layout guide is shown in Figure 6 for reference.

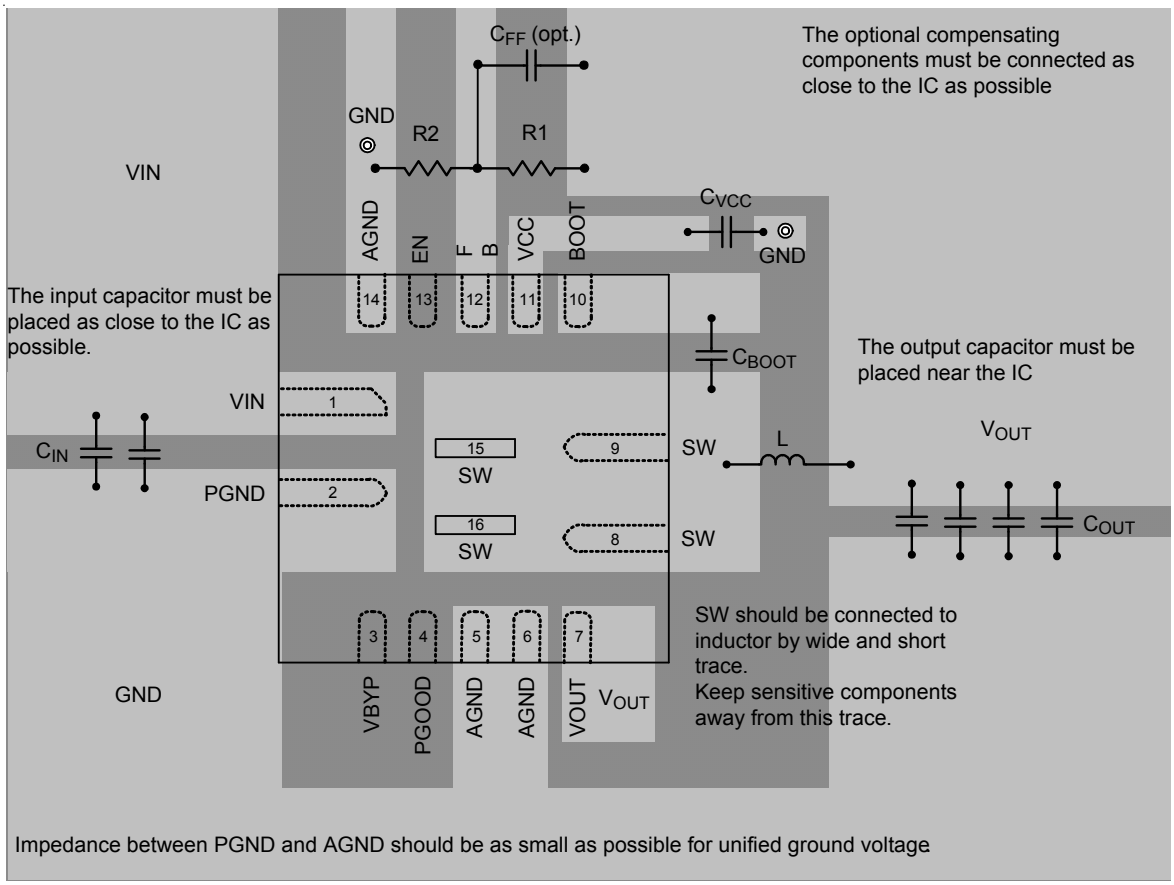
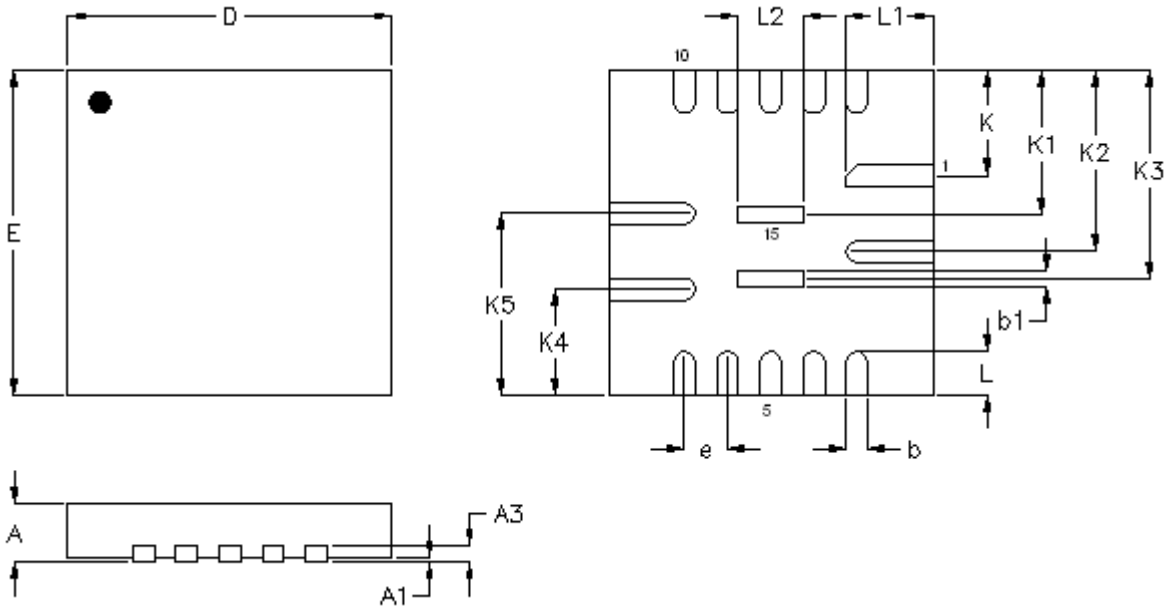


Figure 6. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.175	0.004	0.007
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
b	0.150	0.250	0.006	0.010
b1	0.100	0.200	0.004	0.008
L	0.350	0.450	0.014	0.018
L1	0.750	0.850	0.030	0.033
L2	0.550	0.650	0.022	0.026
e	0.400		0.016	
K	0.975		0.038	
K1	1.335		0.053	
K2	1.675		0.066	
K3	1.935		0.076	
K4	0.975		0.038	
K5	1.675		0.066	

U-Type 16L QFN 3x3 (FC) Package

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