Description

The 5P49V6968 is a programmable clock generator that is intended for high-performance consumer, networking, industrial, computing, and data communications applications. This is Renesas' sixth generation of programmable clock technology (VersaClock 6E).

The 5P49V6968 generates the frequencies from a single reference clock, which can originate from one of the two redundant clock inputs. A glitchless manual switchover function allows one of the redundant clocks to be selected during normal operation.

Two select pins allow up to four different configurations to be programmed, and can be used for different operating modes.

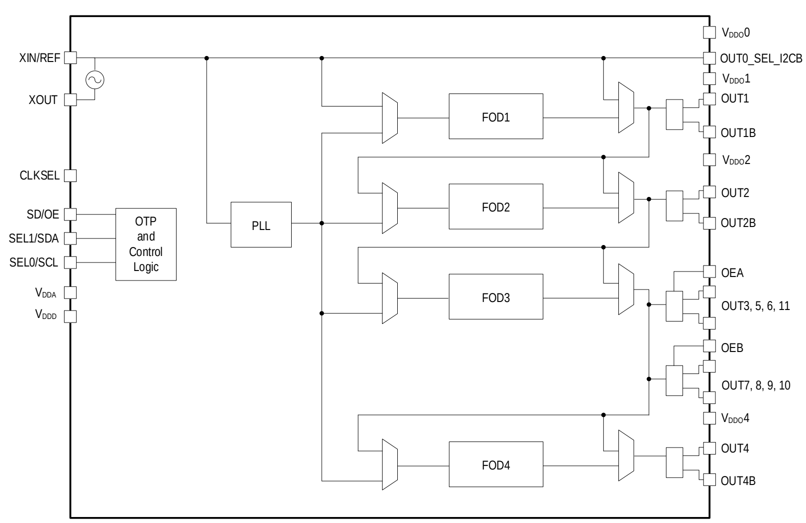
Typical Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0/4.0 spread spectrum on
- PCI Express 1.0/2.0/3.0/4.0/5.0 spread spectrum off
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- Datacenter

Features

- Flexible 1.8V, 2.5V, and 3.3V power rails
- High-performance, low phase noise PLL, < 0.5ps RMS typical phase jitter on outputs
- Four banks of internal OTP memory
  - In-system or factory programmable
- I^2C serial programming interface
  - 0xD0 or 0xD4 I^2C address options allow multiple devices to be configured in a same system
- Reference LVCMOS output clock
- Three universal configurable outputs (OUT1, 2, 4):
  - Differential (LVPECL, LVDS, or HCSL) 1kHz to 350MHz
  - Two single-ended (in-phase or 180 degrees out of phase) 1kHz to 200MHz
  - I/O VDDs can be mixed and matched, supporting 1.8V (LVDS and LVCMOS), 2.5V, or 3.3V
  - Independent spread spectrum on each output pair
- Eight additional LPHCSL outputs (OUT 3, 5–11)
  - 1.8V low power supply
  - 1kHz to 200MHz
- Programmable output enable or power-down mode
- Redundant clock inputs with manual switchover
- Available in 6 × 6 mm 48-VFQFPN package
- -40° to +85°C industrial temperature operation

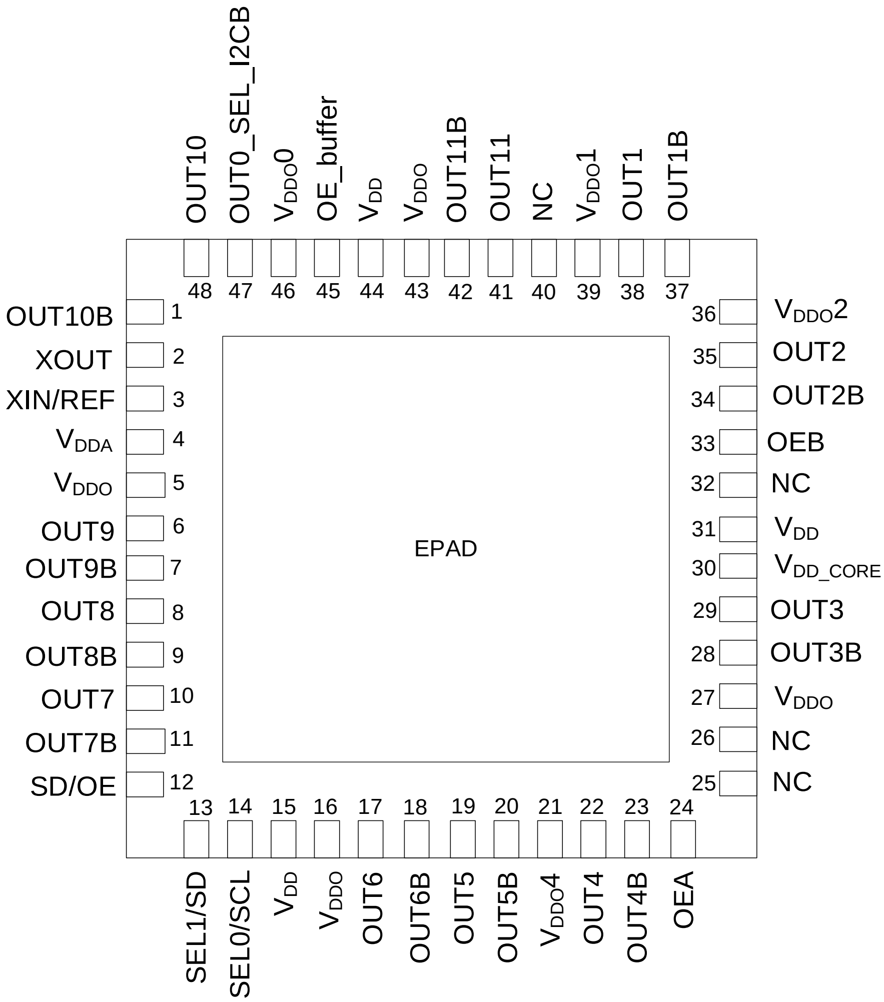
Block Diagram



Contents

1. Pin Assignments

Figure 1. Pin Assignments for 6 × 6 mm 48-VFQFPN Package – Top View



48-pin VFQFPN

2. Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Type		Description
1	OUT10B	Output		Complementary output clock 10. Low-power HCSL (LP-HCSL) output.
2	XOUT	Output		Crystal oscillator interface output.
3	XIN/REF	Input		Crystal oscillator interface input, or single-ended LVCMOS clock input. Input voltage needs to be below 1.2V. Refer to the *Output Drivers* section for more details.
4	VDDA	Power		Analog functions power supply pin. Connect to 1.8V.
5	VDDO	Power		Connect to 1.8V. Power pin for outputs 3, and 5–11.

Pin	Name	Type		Description
6	OUT9	Output		Output clock 9. Low-power HCSL (LP-HCSL) output.
7	OUT9B	Output		Complementary output clock 9. Low-power HCSL (LP-HCSL) output.
8	OUT8	Output		Output clock 8. Low-power HCSL (LP-HCSL) output.
9	OUT8B	Output		Complementary output clock 8. Low-power HCSL (LP-HCSL) output.
10	OUT7	Output		Output clock 7. Low-power HCSL (LP-HCSL) output.
11	OUT7B	Output		Complementary output clock 7. Low-power HCSL (LP-HCSL) output.
12	SD/OE	Input	Internal Pull- down	Enables/disables the outputs (OE) or powers down the chip (SD). The SH bit controls the configuration of the SD/OE pin. The SH bit needs to be high for SD/OE pin to be configured as SD. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW only when the pin is configured as OE (Default is active LOW.) It has a weak internal pull-down resistor. When configured as SD, the device is shut down, differential outputs are driven high/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs can be selected to be tri-stated or driven high/low depending on the programming bits as discussed in “SD/OE Pin Function”.
13	SEL1/SDA	Input	Internal Pull-down	Configuration select pin, or I^{2}C SDA input as selected by OUT0_SEL_I2CB. It has a weak internal pull-down resistor.
14	SEL0/SCL	Input	Internal Pull-down	Configuration select pin, or I^{2}C SCL input as selected by OUT0_SEL_I2CB. It has a weak internal pull-down resistor.
15	VDD	Power		Connect to 1.8V.
16	VDDO	Power		Connect to 1.8V. Power pin for outputs 3, and 5–11.
17	OUT6	Output		Output clock 6. Low-power HCSL (LP-HCSL) output.
18	OUT6B	Output		Complementary output clock 6. Low-power HCSL (LP-HCSL) output.
19	OUT5	Output		Output clock 5. Low-power HCSL (LP-HCSL) output.
20	OUT5B	Output		Complementary output clock 5. Low-power HCSL (LP-HCSL) output.
21	VDDO4	Power		Connect to 1.8V to 3.3V. VDD supply for OUT4.
22	OUT4	Output		Output clock 4. Refer to the *Output Drivers* section for more details.
23	OUT4B	Output		Complementary output clock 4. Refer to the *Output Drivers* section for more details.
24	OEA	Input	Internal Pull-down	Active low output enable pin for outputs 3, 5, 6, and 11. 0 = Enable outputs, 1 = Disable outputs. This pin has an internal pull-down.
25	NC	—		Do not connect.
26	NC	—		Do not connect.
27	VDDO	Power		Connect to 1.8V. This is a power pin for outputs 3, and 5–11.
28	OUT3B	Output		Complementary output clock 3. Refer to the *Output Drivers* section for more details.
29	OUT3	Output		Output clock 3. Refer to the *Output Drivers* section for more details.
30	VDD_Core	Power		Connect to 1.8V.
31	VDD	Power		Connect to 1.8V.

Pin	Name	Type		Description
32	NC	Input		Do not connect.
33	OEB7_10	Input	Internal Pull-down	Active low output enable pin for outputs 7–10. 0 = Enable outputs; 1 = Disable outputs. This pin has an internal pull-down.
34	OUT2B	Output		Complementary output clock 2. Refer to the *Output Drivers* section for more details.
35	OUT2	Output		Output clock 2. Refer to the *Output Drivers* section for more details.
36	VDDO2	Power		Connect to 1.8V to 3.3V. VDD supply for OUT2
37	OUT1B	Output		Complementary output clock 1. Refer to the *Output Drivers* section for more details.
38	OUT1	Output		Output clock 1. Refer to the *Output Drivers* section for more details.
39	VDDO1	Power		Connect to 1.8V to 3.3V. VDD supply for OUT1.
40	NC	—		Do not connect.
41	OUT11	Output		Output clock 11. Low-power HCSL (LP-HCSL) output.
42	OUT11B	Output		Complementary output clock 11. Low-power HCSL (LP-HCSL) output.
43	VDDO	Power		Connect to 1.8V. Power pin for outputs 3, and 5–11.
44	VDD	Power		Connect to 1.8V.
45	OE_buffer	Input	Internal Pull- up	Active High Output enable for outputs 3, and 5–11. 0 = Disable outputs; 1 = Enable outputs. This pin has an internal pull-up.
46	VDDO0	Power		Power supply pin for OUT0_SEL_I2CB and crystal oscillation. Connect to 1.8 to 3.3V. It sets the output voltage levels for OUT0.
47	OUT0_SEL_I2CB	Output	Internal Pull- down	Latched input/LVCMOS Output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 13 and 14. If a weak pull-up (10Kohms) is placed on OUT0_SEL_I2CB, pins 13 and 14 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull-down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 13 and 14 will act as the SDA and SCL pins of an I²C interface. After power up, the pin acts as a LVCMOS reference output.
48	OUT10	Output		Output clock 10. Low-power HCSL (LP-HCSL) output.
ePAD	GND	GND		Connect to ground pad.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.6V
XIN/REF Input	1.2V
I^2C Loading Current (SDA)	10mA
Storage Temperature, TSTG	-65°C to 150°C
Junction Temperature	125°C
ESD Human Body Model	2000V

4. Thermal Characteristics

Table 3. Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Theta JA. Junction to air thermal impedance (0mps)	41.05	°C/W
θ_{JB}	Theta JB. Junction to board thermal impedance (0mps)	13.6	°C/W
θ_{JC}	Theta JC. Junction to case thermal impedance (0mps)	36.41	°C/W

5. Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DDOx}	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions.	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply.	1.71		3.465	V
T_{PU}	Power ramp time for all VDDs to reach 90% of VDD.	0.05		50	ms
T_A	Operating temperature, ambient.	-40		85	°C
C_L	Maximum load capacitance (3.3V LVCMOS only).			15	pF

6. Electrical Characteristics

Table 5. Current Consumption Characteristics

V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{DDCORE}[a]	Core Supply Current	100MHz on all outputs		30		mA
I_{DDOX}	Output Buffer Supply Current	LVPECL, 350MHz, 3.3V V_{DDOx}		42		mA
		LVPECL, 350MHz, 2.5V V_{DDOx}		37		mA
		LVDS, 350MHz, 3.3V V_{DDOx}		18		mA
		LVDS, 350MHz, 2.5V V_{DDOx}		17		mA
		LVDS, 350MHz, 1.8V V_{DDOx}		16		mA
		HCSL, 250MHz, 3.3V V_{DDOx} [b]		29		mA
		HCSL, 250MHz, 2.5V V_{DDOx} [b]		28		mA
		LVCMOS, 50MHz, 3.3V, V_{DDOx} [b],[c]		16		mA
		LVCMOS, 50MHz, 2.5V, V_{DDOx} [b],[c]		14		mA
		LVCMOS, 50MHz, 1.8V, V_{DDOx} [b],[c]		12		mA
		LVCMOS, 200MHz, 3.3V V_{DDOx} [b],[c]		36		mA
		LVCMOS, 200MHz, 2.5V V_{DDOx} [b],[c]		27		mA
		LVCMOS, 200MHz, 1.8V V_{DDOx} [b],[c]		16		mA
I_{DDPD}	Power Down Current	SD asserted, I^2C programming.		10		mA

[a] I_{DDCORE} = I_{DDA} + I_{DDD}, no loads.

[b] Measured into a 5” 50Ω trace with a 2pF load.

[c] Single CMOS driver active.

Table 6. AC Timing Characteristics

V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
F_{IN} [a]	Input Frequency	Input frequency limit (Crystal)	8		40	MHz
		Input frequency limit (Single-ended over XIN)	1		200	
F_{OUT} [b]	Output Frequency	Single-ended clock output limit (LVCMOS), individual FOD mode.	1		200	MHz
		Differential clock output (LVPECL/LVDS/HCSL), individual FOD mode.	0.001		350	
		Single-ended clock output limit (LVCMOS), cascaded FOD mode, output 2, 4.	0.001		200	
		Differential clock output limit (LVPECL/LVDS/HCSL), cascaded FOD mode, output 2, 4.	0.001		350	
		Differential clock output (LP-HCSL output 3, 5–11)	0.001		200	
f_{VCO}	VCO Operating Frequency Range		2500		2900	MHz
T_{DC} [c]	Output Duty Cycle	Measured at V_{DD}/2, all outputs except reference output, V_{DDOX} = 2.5V or 3.3V.	45	50	55	%
		Measured at V_{DD}/2, all outputs except reference output, V_{DDOX} = 1.8V	40	50	60	%
		Measured at V_{DD}/2, reference output OUT0 (5–150.1MHz) with 50% duty cycle input.	40	50	60	%
		Measured at V_{DD}/2, reference output OUT0 (150.1–200MHz) with 50% duty cycle input.	30	50	70	%
T_{SKEW}	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0ns.		75		ps
$T_{STARTUP}$ [d] [e]	Startup Time	Measured after all V_{DD}s have raised above 90% of their target value. [f]			30	ms
		PLL lock time from shutdown mode.		3	4	ms

[a] Practical lower frequency is determined by loop filter settings.
[b] A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
[c] Duty cycle is only guaranteed at maximum slew rate settings.
[d] Actual PLL lock time depends on the loop configuration.
[e] Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.
[f] Power-up with temperature calibration enabled, please contact Renesas if shorter lock-time is required in system.

Table 7. General Input Characteristics

V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Pins	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	SD/OE,SEL1/SDA, SEL0/SCL		3	7	pF
R_{PD}	Pull-down Resistor	SD/OE, SEL1/SDA, SEL0/SCL, OUT0_SEL_I2CB	100		300	kΩ
V_{IH}	Input High Voltage	SD/OE	0.7 x V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input Low Voltage	SD/OE	GND - 0.3		0.3 x V_{DDD}	V
V_{IH}	Input High Voltage	OUT0_SEL_I2CB	0.65 x V_{DDO0}		V_{DDO0} + 0.3	V
V_{IL}	Input Low Voltage	OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input High Voltage	XIN/REF	0.8		1.2	V
V_{IL}	Input Low Voltage	XIN/REF	GND - 0.3		0.4	V
T_R/T_F	Input Rise/Fall Time	SD/OE, SEL1/SDA, SEL0/SCL			300	ns

Table 8. Electrical Characteristics – CMOS Outputs

V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	IOH = -15mA (3.3V), -12mA (2.5V).	0.7 x V_{DDO}		V_{DDO}	V
V_{OH}	Output High Voltage	IOH = -8mA (1.8V)	0.5 x V_{DDO}		V_{DDO}	V
V_{OL}	Output Low Voltage	IOH = 15mA (3.3V), 12mA (2.5V), 8mA (1.8V)			0.45	V
R_{OUT}	Output Driver Impedance	CMOS Output Driver		17		Ω
T_{SR}	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (output load = 5pF) V_{DDOX} = 3.3V	1.0	2.2		V/ns
	Slew Rate, SLEW[1:0] = 01		1.2	2.3		
	Slew Rate, SLEW[1:0] = 10		1.3	2.4		
	Slew Rate, SLEW[1:0] = 11		1.7	2.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 2.5V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (output load = 5pF) V_{DDOX} = 2.5V	0.6	1.3		
	Slew Rate, SLEW[1:0] = 01		0.7	1.4		
	Slew Rate, SLEW[1:0] = 10		0.6	1.4		
	Slew Rate, SLEW[1:0] = 11		1.0	1.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 1.8V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (output load = 5pF) VDD = 1.8V.	0.3	0.7		
	Slew Rate, SLEW[1:0] = 01		0.4	0.8		
	Slew Rate, SLEW[1:0] = 10		0.4	0.9		
	Slew Rate, SLEW[1:0] = 11		0.7	1.2		
I_{OZDD}	Output Leakage Current (OUT1–4)	Tri-state outputs			5	μA
	Output Leakage Current (OUT0)	Tri-state outputs			30	μA

Table 9. Electrical Characteristics – LVDS Outputs

V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{OT} (+)	Differential Output Voltage for the TRUE Binary State	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE Binary State	-454		-247	mV
ΔV_{OT}	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage) at 3.3V±5%, 2.5V±5%	1.125	1.25	1.375	V
	Output Common Mode Voltage (Offset Voltage) at 1.8V±5%	0.8	0.875	0.96	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT}-		6	12	mA
T_R	LVDS rise time 20%-80%		300		ps
T_F	LVDS fall time 80%-20%		300		ps

Table 10. Electrical Characteristics – LVPECL Outputs

V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{OH}	Output Voltage High, terminated through 50Ω tied to V_{DD} - 2V	V_{DDO} - 1.19		V_{DDO} - 0.69	V
V_{OL}	Output Voltage Low, terminated through 50Ω tied to V_{DD} - 2V	V_{DDO} - 1.94		V_{DDO} - 1.4	V
V_{SWING}	Peak-to-Peak Differential Output Voltage Swing	1.1		2	V
T_R	LVPECL rise time 20%-80%		400		ns
T_F	LVPECL fall time 80%-20%		400		ns

Table 11. Electrical Characteristics – HCSL Outputs[a]

V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
dV/dt	Slew Rate	Scope averaging on [b] [c]	1		4	V/ns
ΔdV/dt	Slew Rate Matching	Scope averaging on [b] [c]			20	%
V_{MAX}	Maximum Voltage	Measurement on single-ended signal using absolute value (scope averaging off)			1150	mV
V_{MIN}	Minimum Voltage		-300			mV
V_{SWING}	Voltage Swing	Scope averaging off [b] [f]	300			mV
V_{CROSS}	Crossing Voltage Value	Scope averaging off [d] [f]	250		550	mV
ΔV_{CROSS}	Crossing Voltage Variation	Scope averaging off [e]			140	mV

[a] Guaranteed by design and characterization. Not 100% tested in production.

[b] Measured from differential waveform.

[c] Slew rate is measured through the VSWING voltage range centered on differential 0V. This results in a ±150mV window around differential 0V.

[d] VCROSS is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e., Clock rising and Clock# falling).

[e] The total variation of all VCROSS measurements in any particular system. Note that this is a subset of VCROSS min/max (VCROSS absolute) allowed. The intent is to limit VCROSS induced modulation by setting ΔVCROSS to be smaller than VCROSS absolute.

[f] Measured from single-ended waveform.

Table 12. Spread-Spectrum Generation Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{SSOUT}	Spread Frequency	Output frequency range for spread spectrum	5		300	MHz
f_{MOD}	Mod Frequency	Modulation frequency.		30 to 63		kHz
f_{SPREAD}	Spread Value	Amount of spread value (programmable)–center spread.		±0.1% to ±2.5%		$\%f_{OUT}$
		Amount of spread value (programmable)–down spread.		-0.2% to -5%		

Table 13. I²C Bus (SCL/SDA) DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Level	For SEL1/SDA pin and SEL0/SCL pin.	0.7 x V_{DDD}			V
V_{IL}	Input Low Level	For SEL1/SDA pin and SEL0/SCL pin.			0.3 x V_{DDD}	V
V_{HYS}	Hysteresis of Inputs		0.05 x V_{DDD}			V
I_{IN}	Input Leakage Current		-1		36	μA
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V

Table 14. I²C Bus (SCL/SDA) AC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
F_{SCLK}	Serial Clock Frequency (SCL)	10		400	kHz
t_{BUF}	Bus Free Time between Stop and Start	1.3			μs
$t_{SU:START}$	Setup Time, Start	0.6			μs
$t_{HD:START}$	Hold Time, Start	0.6			μs
$t_{SU:DATA}$	Setup Time, Data Input (SDA)	0.1			μs
$t_{HD:DATA}$	Hold Time, Data Input (SDA) [a]	0			μs
t_{OVD}	Output Data Valid from Clock			0.9	μs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, Data and Clock (SDA, SCL)	20 + 0.1 x C_B		300	ns
t_F	Fall Time, Data and Clock (SDA, SCL)	20 + 0.1 x C_B		300	ns
t_{HIGH}	High Time, Clock (SCL)	0.6			μs
t_{LOW}	Low Time, Clock (SCL)	1.3			μs
$t_{SU:STOP}$	Setup Time, Stop	0.6			μs

[a] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[b] I²C inputs are 3.3V tolerant.

7. Test Loads

Figure 2. LVCMOS Test Load

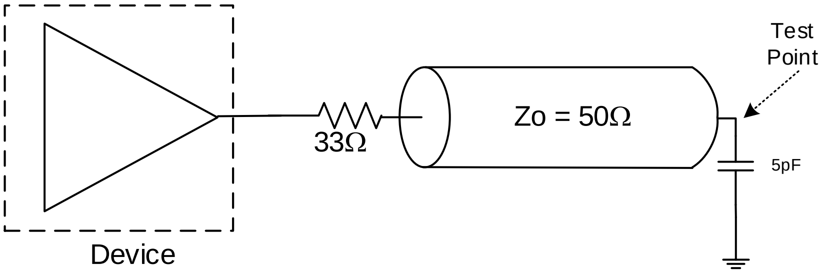


Figure 3. HCSL/LPHCSL Test Load

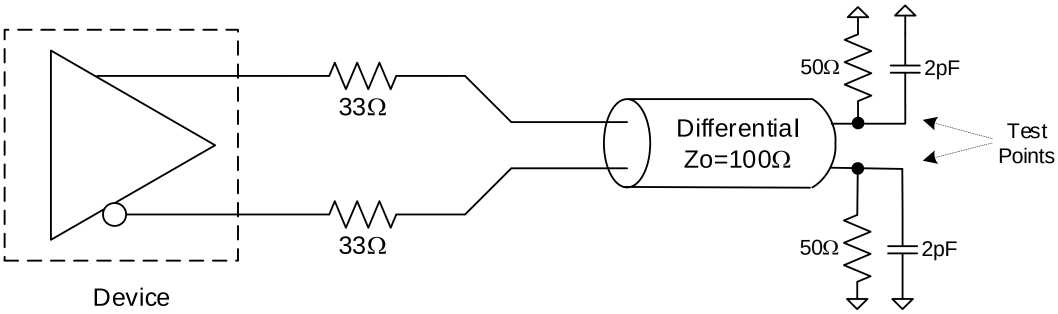


Figure 4. LVDS Test Load

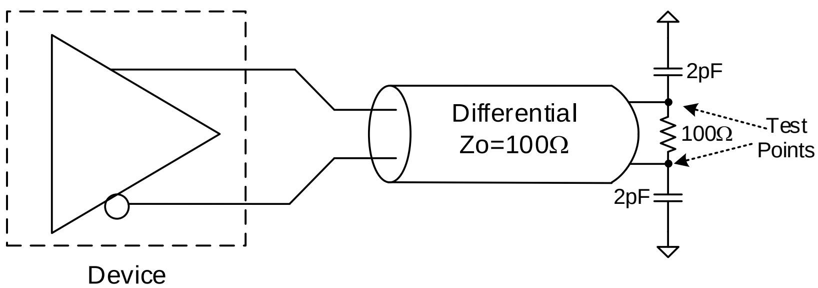
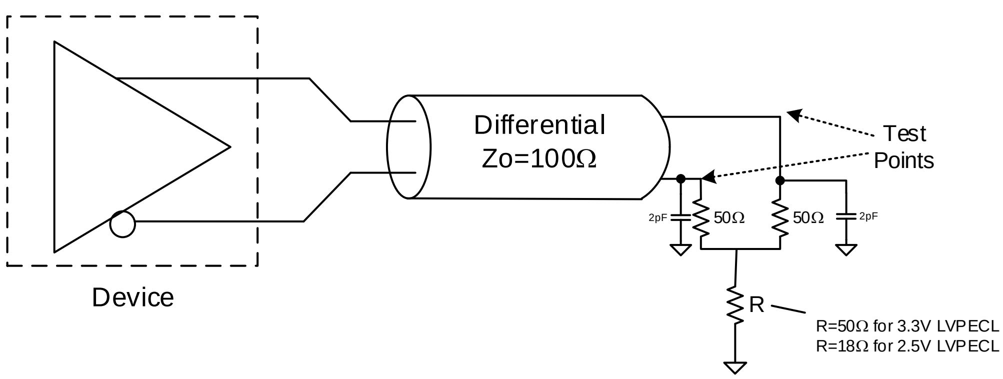
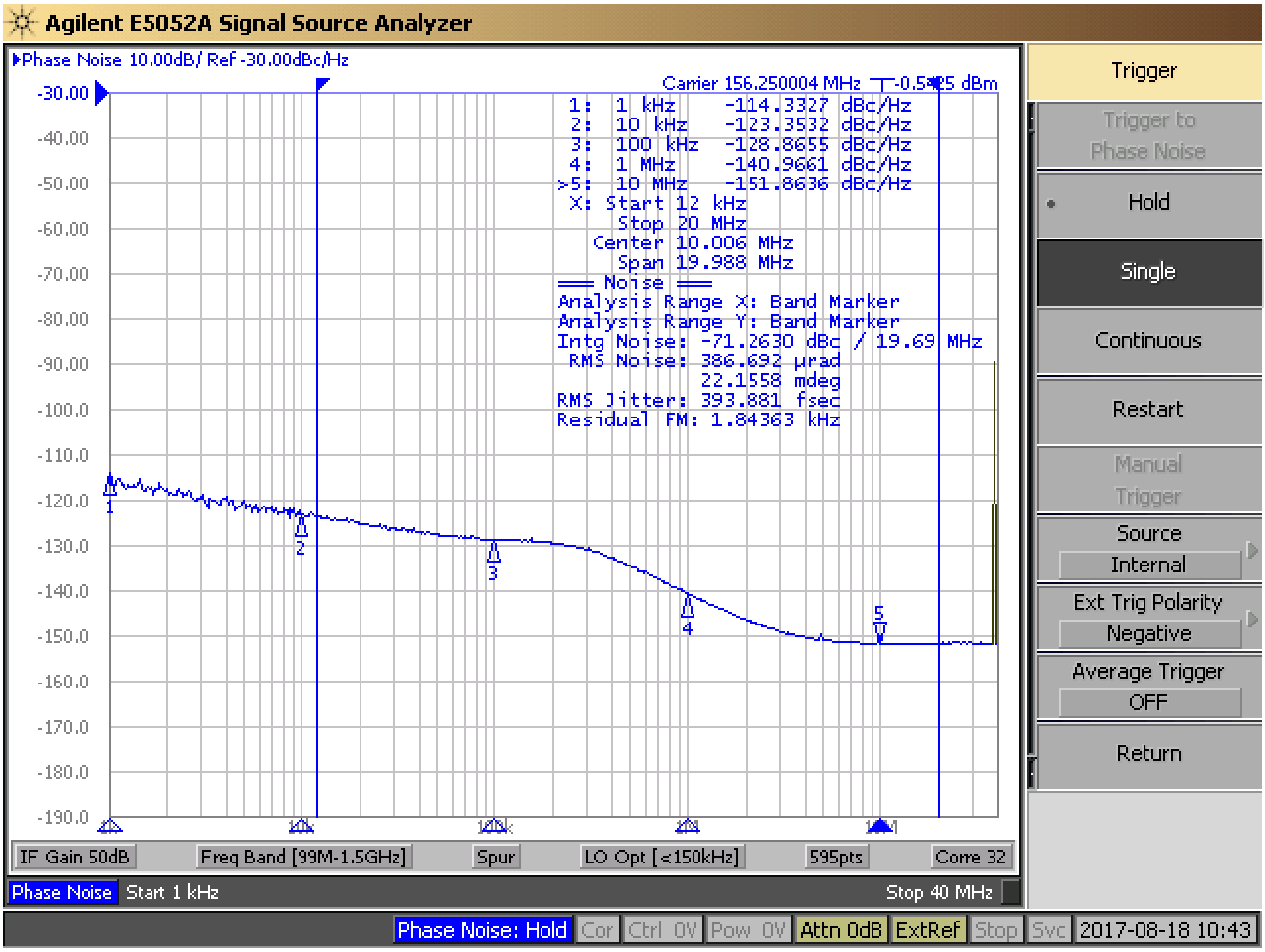


Figure 5. LVPECL Test Load



8. Jitter Performance Characteristics

Figure 6. Typical Phase Jitter Plot at 156.25MHz



Note: Measured with OUT2=156.25MHz on, 39.625MHz input.

Table 15. Jitter Performance

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
J_{CY-CY}	Cycle to Cycle Jitter	LVCMOS 3.3V ±5%,-40°C to 90°C		5	30	ps
		All differential outputs 3.3V ±5%,-40°C to 90°C		25	35	ps
J_{pk-pk}	Period Jitter	LVCMOS 3.3V ±5%,-40°C–90°C		28	40	ps
		All differential outputs 3.3V ±5%,-40°C to 90°C		4	30	ps
J_{RMS}	RMS Phase Jitter (12kHz-20MHz)	LVCMOS 3.3V ±5%,-40°C to 90°C		0.3		ps
		All differential outputs 3.3V ±5%,-40°C to 90°C		0.5		ps

[a] Measured with 25MHz crystal input.

[b] Configured with OUT0 = 25MHz–LVCMOS OUT1 = 100MHz HCSL OUT2 = 125MHz LVDS OUT3 = 156.25MHz–LVPECL.

9. PCI Express Jitter Performance and Specification

Table 16. PCI Express Jitter Performance (Spread Spectrum = OFF)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
PCIe Phase Jitter (Common Clocked Architectures)	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen1 (2.5 GT/s) SSC = OFF		4		86	ps (p-p)	1, 2
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen2 Lo Band (5.0 GT/s) SSC = OFF		0.05		3	ps (RMS)	1, 2
		PCIe Gen2 Hi Band (5.0 GT/s) SSC = OFF		0.22		3.1	ps (RMS)	1, 2
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen3 (8.0 GT/s) SSC = OFF		0.12		1	ps (RMS)	1, 2
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen4 (16.0 GT/s) SSC = OFF		0.12		0.5	ps (RMS)	1, 2, 3, 4
	$t_{jphPCIeG5\text{-}CC}$	PCIe Gen5 (32.0 GT/s) SSC = OFF		0.05		0.15	ps (RMS)	1, 2, 3, 5
PCIe Phase Jitter (SRNS Architectures)	$t_{jphPCIeG1\text{-}SRNS}$	PCIe Gen1 (2.5 GT/s) SSC = OFF		0.3		n/a	ps (p-p)	1, 2, 6
	$t_{jphPCIeG2\text{-}SRNS}$	PCIe Gen2 (5.0 GT/s) SSC = OFF		0.26		n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG3\text{-}SRNS}$	PCIe Gen3 (8.0 GT/s) SSC = OFF		0.07		n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG4\text{-}SRNS}$	PCIe Gen4 (16.0 GT/s) SSC = OFF		0.07		n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG5\text{-}SRNS}$	PCIe Gen5 (32.0 GT/s) SSC = OFF		0.07		n/a	ps (RMS)	1, 2, 6

1 The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table.

2 Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

3 SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

4 Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

5 Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

6 While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by Ö2.

Table 17. PCI Express Jitter Performance (Spread Spectrum = ON)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
PCIe Phase Jitter (Common Clocked Architectures)	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen1 (2.5 GT/s) SSC = ≤ -0.5%		16		86	ps (p-p)	1, 2
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen2 Lo Band (5.0 GT/s) SSC = ≤ -0.5%		0.02		3	ps (RMS)	1, 2
		PCIe Gen2 Hi Band (5.0 GT/s) SSC = ≤ -0.5%		0.92		3.1	ps (RMS)	1, 2
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen3 (8.0 GT/s) SSC = ≤ -0.5%		0.37		1	ps (RMS)	1, 2
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen4 (16.0 GT/s) SSC = ≤ -0.5%		0.37		0.5	ps (RMS)	1, 2, 3, 4
	$t_{jphPCIeG5\text{-}CC}$	PCIe Gen5 (32.0 GT/s) SSC = ≤ -0.5%		N/A		0.15	ps (RMS)	1, 2, 3, 5
PCIe Phase Jitter (SRIS Architectures)	$t_{jphPCIeG1\text{-}SRIS}$	PCIe Gen1 (2.5 GT/s) SSC = ≤ -0.3%		14		n/a	ps (p-p)	1, 2, 6
	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen2 (5.0 GT/s) SSC = ≤ -0.3%		1.4		n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen3 (8.0 GT/s) SSC = ≤ -0.3%		0.42		n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG4\text{-}SRIS}$	PCIe Gen4 (16.0 GT/s) SSC = ≤ -0.3%		0.36		n/a	ps (RMS)	1, 2, 6
	$t_{jphPCIeG5\text{-}SRIS}$	PCIe Gen5 (32.0 GT/s) SSC = ≤ -0.3%		N/A		n/a	ps (RMS)	1, 2, 6

[1] The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by Ö2.

10. Features and Functional Blocks

10.1 Device Startup and Power-on-Reset

The 5P49V6968 has an internal power-up reset (POR) circuit. All VDDs must be connected to the desired supply voltage to trigger a POR.

The user can define specific default configurations through internal One-Time-Programmable (OTP) memory -- either the user or factory can program the default configuration. Contact Renesas if a specific factory-programmed default configuration is required, or refer to the *VersaClock 6E Programming Guide*.

The device will identity which of the two modes to operate in by the state of the OUT0_SEL_I2CB pin at POR. Both modes' default configurations can be programmed as follows:

1. **Software Mode (I^2C):** OUT0_SEL_I2CB is low at POR.

   The I^2C interface will be open to users for in-system programming, overriding device default configurations at any time.

2. **Hardware Select Mode:** OUT0_SEL_I2CB is high at POR.

   The device has been programmed to load OTP at power-up (REG0[7] = 1). The device will load internal registers according to *Table 18. Power-Up Behavior* .

   Internal OTP memory can support up to four configurations, which selectable by the SEL0/SEL1 pins.

   At POR, logic levels at SEL0 and SEL1 pins must be settled, which results in the selected configuration to be loaded at power up.

   After the first 10ms of operation, the levels of the SELx pins can be changed, either to low or to the same level as VDDD/VDDA. The SELx pins must be driven with a digital signal of < 300ns rise/fall time and only a single pin can be changed at a time. After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

Table 18. Power-Up Behavior

OUT0_SEL_I2CB at POR	SEL1	SEL0	I^2C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	X	X	Yes	1	I^2C defaults
0	X	X	Yes	0	0

10.2 Internal Crystal Oscillator (XIN/REF)

10.2.1 Choosing Crystals

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa. Therefore, for an accurate oscillation frequency you must match the oscillator load capacitance with the crystal load capacitance.

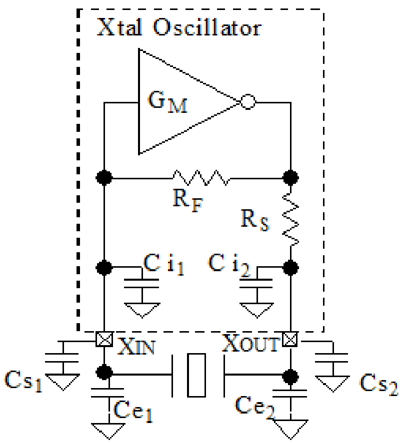
10.2.2 Tuning the Crystal Load Capacitor

Cs1 and Cs2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF (see Figure 7).

Ce1 and Ce2 are additional external capacitors. Increasing the load capacitance reduces the oscillator gain, so it is recommended to consult the manufacturer when adding Ce1 and/or Ce2 to avoid crystal startup issues.

Ci1 and Ci2 are integrated programmable load capacitors, one at XIN and one at XOUT.

Figure 7. Tuning the Crystal Load Capacitor



The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register. Ci1 and Ci2 are commonly programmed to be the same value. Adjustment of the crystal tuning capacitors allows maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table. Ci1/Ci2 starts at 9pF with the setting 000000b, and can be increased up to 25pF with the setting 111111b. The step per bit is 0.5pF.

Table 19. XTAL[5:0] Tuning Capacitor

Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	6	0.5	9	25

You can write the following equation for this capacitance:

$$Ci = 9pF + 0.5pF \times XTAL[5:0]$$

$$C_{XIN} = Ci1 + Cs1 + Ce1$$

$$C_{XOUT} = Ci2 + Cs2 + Ce2$$

The final load capacitance of the crystal:

$$C_L = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$$

It is recommended to set the same value at each crystal pin meaning:

$C_{XIN} = C_{XOUT}$

Example 1: The crystal load capacitance is specified as 8pF and the stray capacitance at each crystal pin is Cs = 1.5pF. Assuming an equal capacitance value at XIN and XOUT, the equation is as follows:

8pF = (9pF + 0.5pF × XTAL[5:0] + 1.5pF) / 2

So, XTAL[5:0] = 11 (decimal)

Example 2: The crystal load capacitance is specified as 12pF and the stray capacitance Cs is unknown. Footprints for external capacitors Ce are added and a worst case Cs of 5pF is used. This example uses Cs + Ce = 5pF; the correct value for Ce can be determined later to make 5pF together with Cs.

12pF = (9pF + 0.5pF × XTAL[5:0] + 5pF) / 2

So, XTAL[5:0] = 20 (decimal)

Table 20. Recommended Crystal Characteristics

Parameter	Minimum	Typical	Maximum	Units
Mode of Oscillation	Fundamental			
Frequency	8	25	40	MHz
Equivalent Series Resistance (ESR)		10	100	Ω
Shunt Capacitance			7	pF
Load Capacitance (C_L) at < = 25MHz	6	8	12	pF
Load Capacitance (C_L) > 25MHz to 40MHz	6		8	pF
Maximum Crystal Drive Level			100	µW

10.3 Programmable Loop Filter

The device PLL loop bandwidth operating range depends on the input reference frequency (Fref).

Table 21. Loop Filter Settings

Input Reference Frequency (MHz)	Loop Bandwidth Minimum (kHz)	Loop Bandwidth Maximum (kHz)
1	40	126
350	300	1000

10.4 Fractional Output Dividers (FOD)

The 5P49V6968 has four fractional output dividers (FOD). Each FOD is comprised of a 12-bit integer counter and a 24-bit fractional counter. The output divider can operate in integer divide only mode for improved performance, or use the fractional counters to generate a clock frequency accurate to 50ppb.

FODs support the following features.

10.4.1 Individual Spread Spectrum Modulation

The output clock frequencies can be modulated to spread energy across a broader range of frequencies, thereby lowering system EMI. Each divider has individual spread ability. Spread modulation independent of output frequency, a triangle wave modulation between 30 and 63kHz.

Spread spectrum can be applied to any output clock, clock frequency, or spread amount from ±0.25% to ±2.5% center-spread and -0.5% to -5% down-spread.

10.4.2 Bypass Mode

Bypass mode (divide by 1) allows the output to behave as a buffered copy from the input or another FOD.

10.4.3 Cascaded Mode

As shown in the block diagram on page 1, FODs can be cascaded for lower output frequency.

For example, if OUT1 is configured to run at 12.288MHz and needs another 48kHz output, the user can cascade FOD2 by taking input from OUT1, with a divide ratio of 256. As a result, OUT 2 runs at 48kHz while in alignment with 12.288MHz on OUT1.

10.4.4 Dividers Alignment

Each output divider block has a synchronizing pulse to provide startup alignment between outputs dividers. This allows alignment of outputs for low skew performance.

When the 5P49V6968 is in hardware select mode, outputs are automatically aligned at POR. The same synchronization reset is also triggered when switching between configurations with the SEL0/1 pins. This ensures that the outputs remain aligned in every configuration.

When the 5P49V6968 is using software mode, I^{2}C is used to reprogram an output divider during operation, and therefore, alignment can be lost. Alignment can be restored by manually triggering a reset through I^{2}C.

The outputs are aligned on the falling edges of each output by default. Rising edge alignment can also be achieved by using the programmable skew feature to delay the faster clock by 180 degrees. The programmable skew feature also allows for fine tuning of the alignment.

10.4.5 Programmable Skew

The 5P49V6968 can skew outputs by quadrature values. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. As a result, for 100MHz output and a 2800MHz VCO, the user can select how many 11.161ps units to be added to the skew (resulting in units of 0.402 degrees). For example, 0, 0.402, 0.804, 1.206, 1.408, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

10.5 Output Drivers

Device output drivers can individually support the following features:

- 2.5V or 3.3V voltage level for HCSL/LVPECL operation
- 1.8V, 2.5V, or 3.3V voltage levels for CMOS/LVDS operation
- CMOS supports four operating modes:
  - CMOSD: OUTx and OUTxB 180 degrees out of phase
  - CMOSX2: OUTx and OUTxB phase-aligned
  - CMOS1: only OUTx pin is on
  - CMOS2: only OUTxB pin is on

  When a given output is configured to CMOSD or CMOSX2, then all previously described configuration and control apply equally to both pins.
- Independent output enable/disabled by register bits. When disabled, an output can be either in a logic 1 state or Hi-Z.

The following options are used to disable outputs:

- Output turned off by I^2C
- Output turned off by SD/OE pin
- Output unused, which means it is turned off regardless of OE pin status

10.6 SD/OE Pin Function

The SD/OE pin can be programmed as follows:

- OE output enable (low active)
- OE output enable (high active)
- Global shutdown (low active)
- Global shutdown (high active)

Output behavior when disabled is also programmable. The user can select the output driver behavior when it is off as follows:

- OUTx pin high, OUTxB pin low (controlled by SD/OE pin)
- OUTx/OUTxB Hi-Z (controlled by SD/OE pin)
- OUTx pin high, OUTxB pin low (configured through I^2C)
- OUTx/OUTxB Hi-Z (configured by I^2C)

The user can disable the output with either I^2C or SD/OE pin. For more information, see the *VersaClock 6E Programming Guide*.

10.7 I²C Operation

The 5P49V6968 acts as a slave device on the I²C bus using one of the two I²C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations.

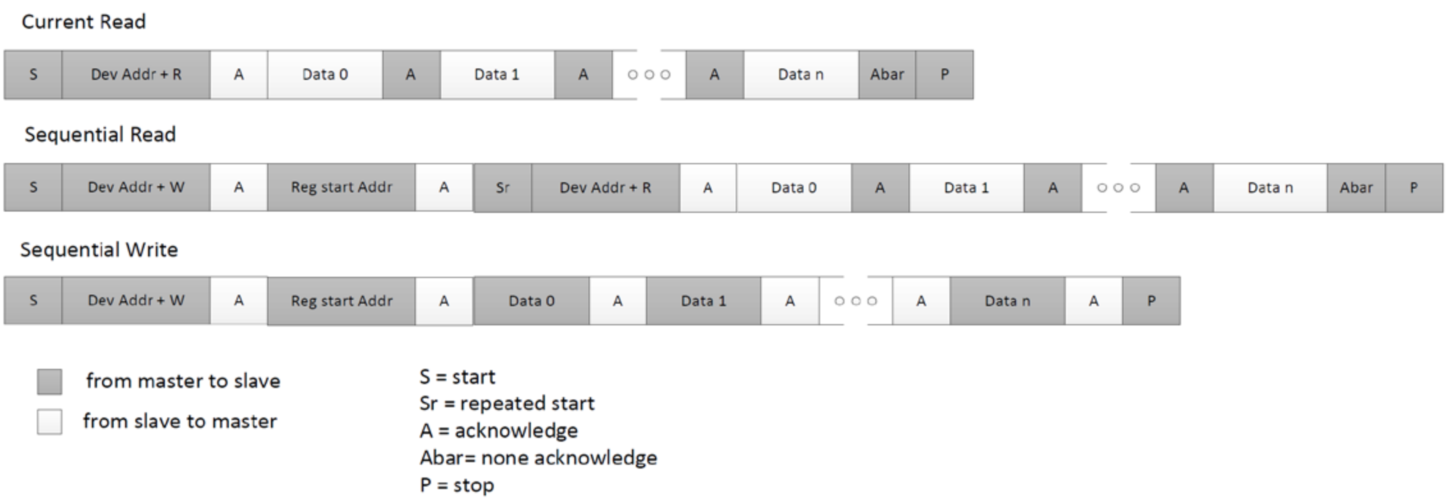
Address bytes (2 bytes) specify the register address of the byte position of the first register to write or read.

Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first).

Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

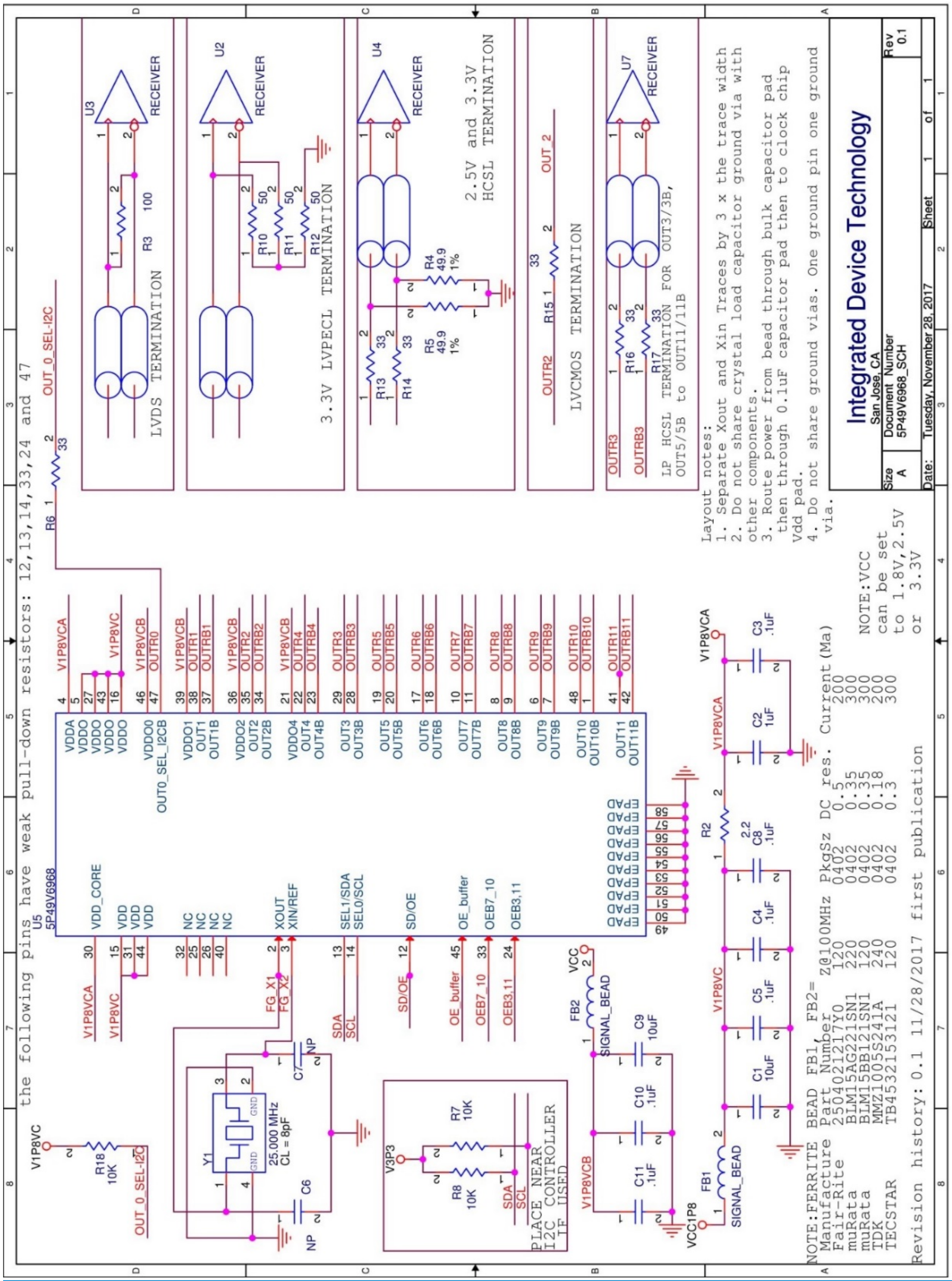
For full electrical I²C compliance, use external pull-up resistors for SDATA and SCLK.

Figure 8. I²C R/W Sequence



11. Typical Application Circuit

Figure 9. Typical Application Circuit



11.1 Input – Driving the XIN/REF

11.1.1 Driving XIN/REF with a CMOS Driver

In some instances, it is preferable to have XIN/REF driven by a clock input -- for reasons such as better SNR, multiple input select with device CLKIN, etc. The XIN/REF pin can take an input when its amplitude is between 500mV and 1.2V, and the slew rate more than 0.2V/ns. The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating.

Figure 10. Overdriving XIN with a CMOS Driver

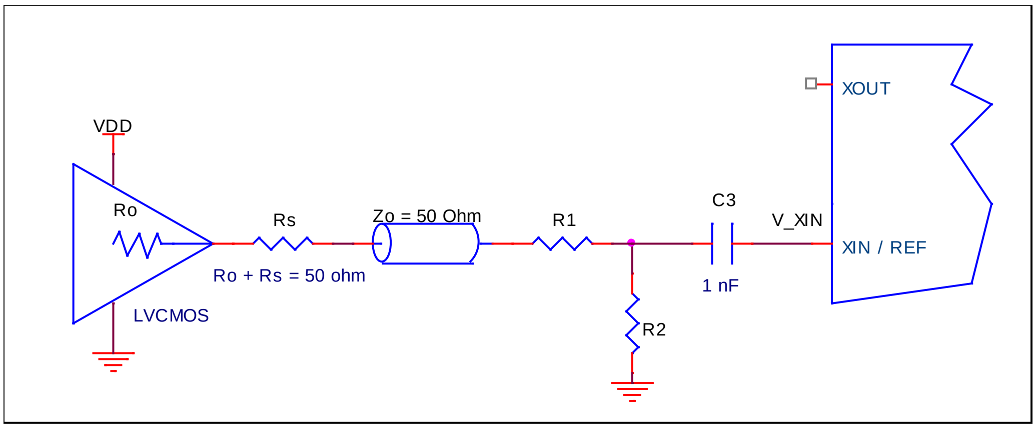


Table 22. Nominal Voltage Divider Values for Overdriving CLKIN with Single-ended Driver

LVCMOS Diver V_{DD}	Ro + Rs	R1	R2	V_XIN (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

11.1.2 Driving XIN with a LVPECL Driver

Figure 11 shows an example of the interface diagram for a 3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematic be placed in the layout; though some components may not be used, they can be used for debugging purposes. The datasheet specifications are characterized and guaranteed using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only required change is to use the appropriate R3 value.

Figure 11. Overdriving XIN with a LVPECL Driver

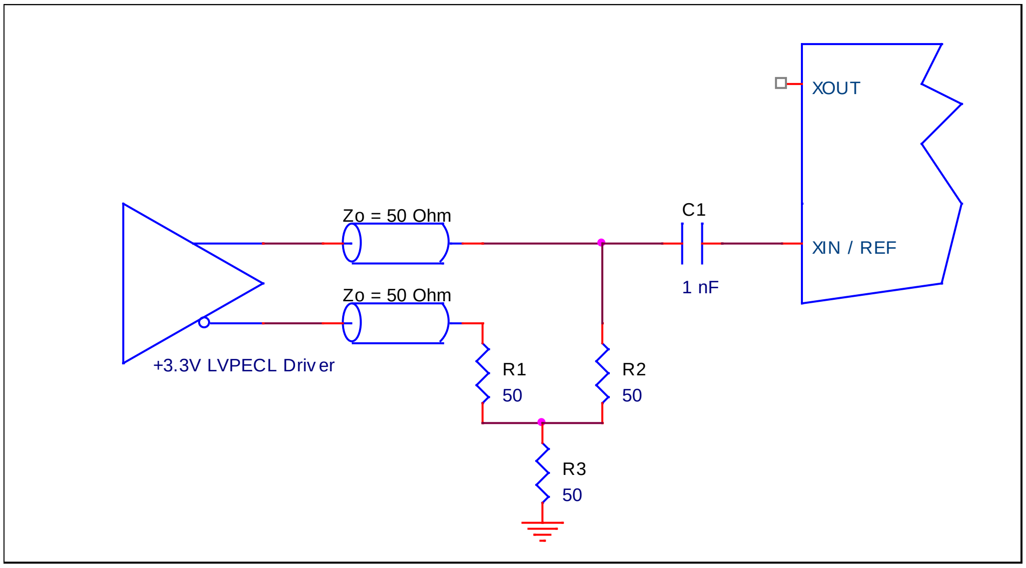


Table 23 shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver V_{DD}, V_{DDO0}, and 5% resistor tolerances. The resistor values can be adjusted to reduce the loading for a slower and weaker LVCMOS driver by increasing the impedance of the R1–R2 divider. To better assist with this assessment, the total load (Ro+Rs+R1+R2) on the driver is included in the table.

Table 23. Nominal Voltage Divider Values for Overdriving CLKIN with Single-ended Driver

LVCMOS Diver V_{DD}	Ro + Rs	R1	R2	Vrx (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

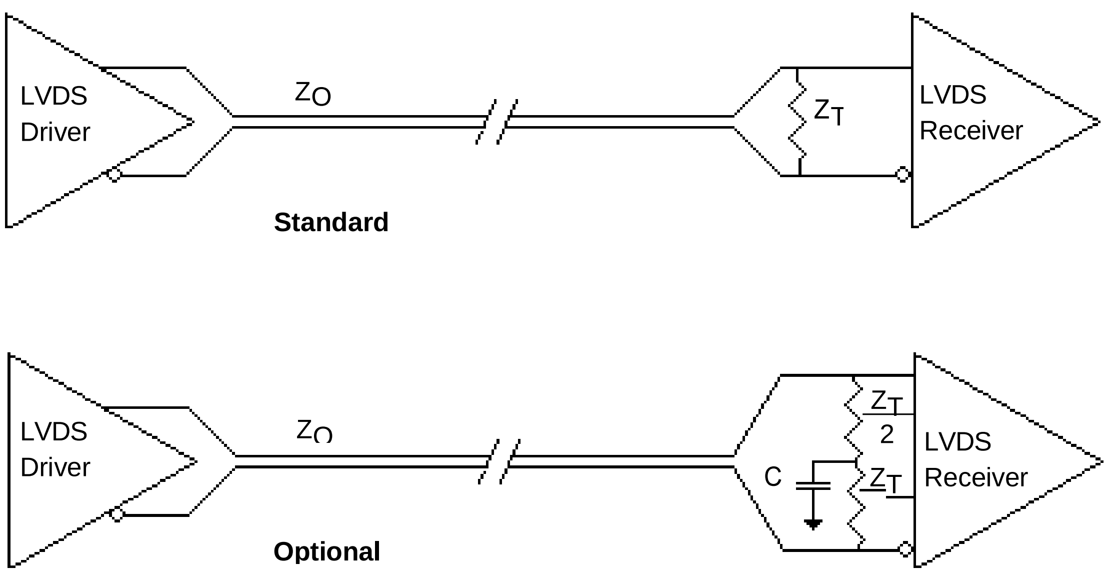
11.2 Output – Single-ended or Differential Clock Terminations

11.2.1 LVDS Termination

For a general LVDS interface, the recommended value for the termination impedance (ZT) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Zo) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω. Differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure *Standard Termination* or the termination of figure *Optional Termination* can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the Renesas LVDS output.

For example, the LVDS outputs can be AC coupled by placing capacitors between the LVDS outputs and the 100Ω shunt load. This is a common practice with receiver with internal self-bias circuitry. If using a non-standard termination, it is recommended to contact Renesas and confirm that the termination will function as intended.

Figure 12. Standard and Optional Terminations



11.2.2 LVPECL Termination

The clock layout topology shown below are typical terminations for LVPECL outputs. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. For VDDO = 2.5V, the VDDO – 2V is very close to ground level. The R3 in 2.5V LVPECL Output Termination can be eliminated and the termination is shown in 2.5V LVPECL Output Termination (2).

Figure 13. 3.3V LVPECL Output Termination (1)

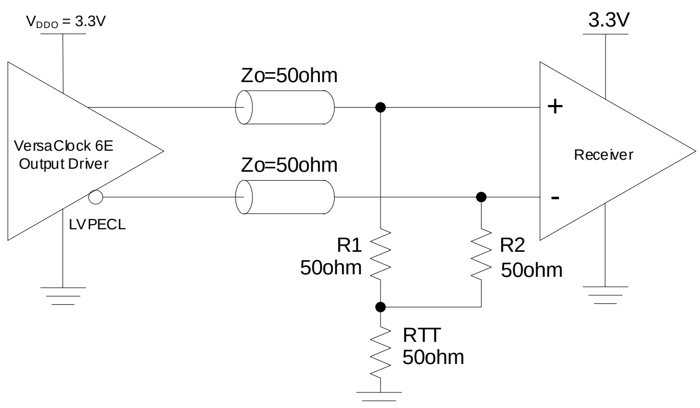


Figure 15. 2.5V LVPECL Output Termination (1)

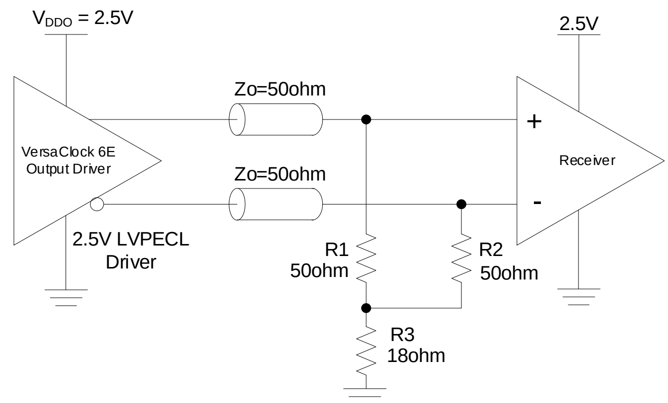


Figure 14. 3.3V LVPECL Output Termination (2)

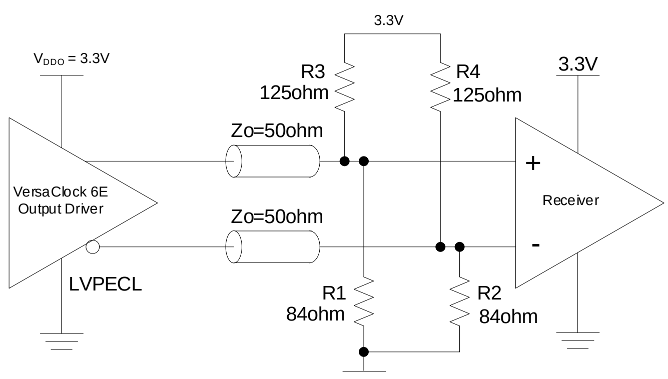


Figure 16. 2.5V LVPECL Output Termination (2)

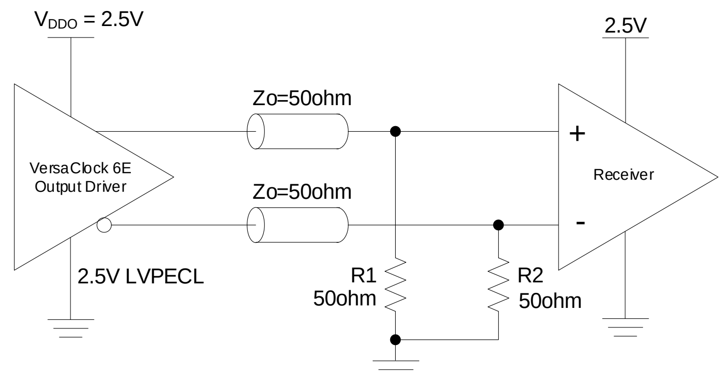
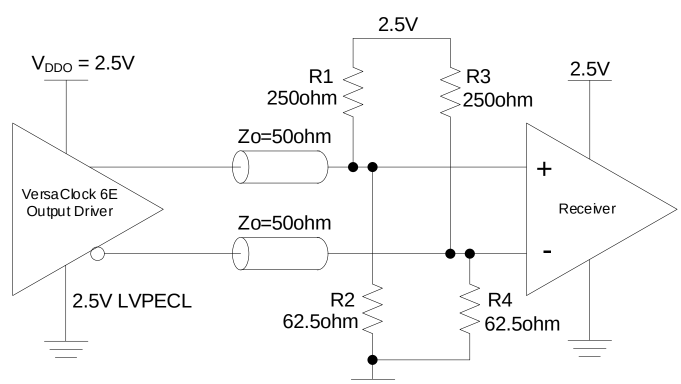


Figure 17. 2.5V LVPECL Output Termination (3)



11.2.3 HCSL Termination

HCSL termination scheme applies to both 3.3V and 2.5V VDDO.

Figure 18. HCSL Receiver Terminated

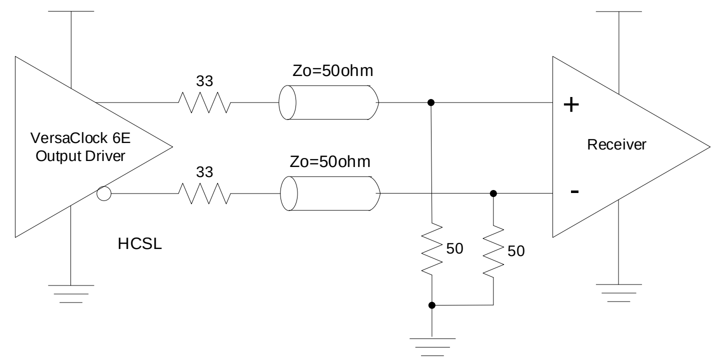
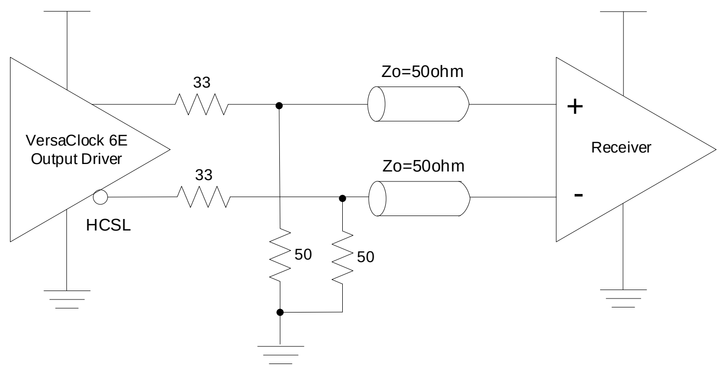


Figure 19. HCSL Source Terminated

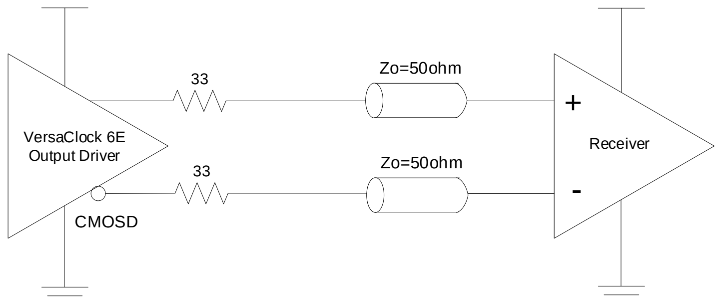


11.2.4 LVCMOS Termination

Each output pair can be configured as a standalone CMOS or dual-CMOS output driver. An example of CMOSD driver termination is shown in the following figure:

- CMOS1 – Single CMOS active on OUTx pin
- CMOS2 – Single CMOS active on OUTxB pin
- CMOSD – Dual CMOS outputs active on both OUTx and OUTxB pins, 180 degrees out of phase
- CMOSX2 – Dual CMOS outputs active on both OUTx and OUTxB pins, in-phase

Figure 20. LVCMOS Termination



12. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/48-vfqfpn-package-outline-drawing60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitchndg48p2

13. Marking Diagram

- Lines 1 and 2 indicate the part number.
- Line 3:
  - "YYWW" is the last digit of the year and week that the part was assembled.
  - # denotes the sequential lot number.
  - "$" denotes the mark code.

14. Ordering Information

Orderable Part Number [a][b]	Package	Carrier Type	Temperature
5P49V6968AdddNDGI	6 × 6 mm 48-VFQFPN	Tray	-40° to +85°C
5P49V6968AdddNDGI8	6 × 6 mm 48-VFQFPN	Tape and Reel	-40° to +85°C
5P49V6968A000NDGI	6 × 6 mm 48-VFQFPN	Tray	-40° to +85°C
5P49V6968A000NDGI8	6 × 6 mm 48-VFQFPN	Tape and Reel	-40° to +85°C

[a] "ddd" denotes factory programmed configurations based on required settings. Please contact factory for factory programming.

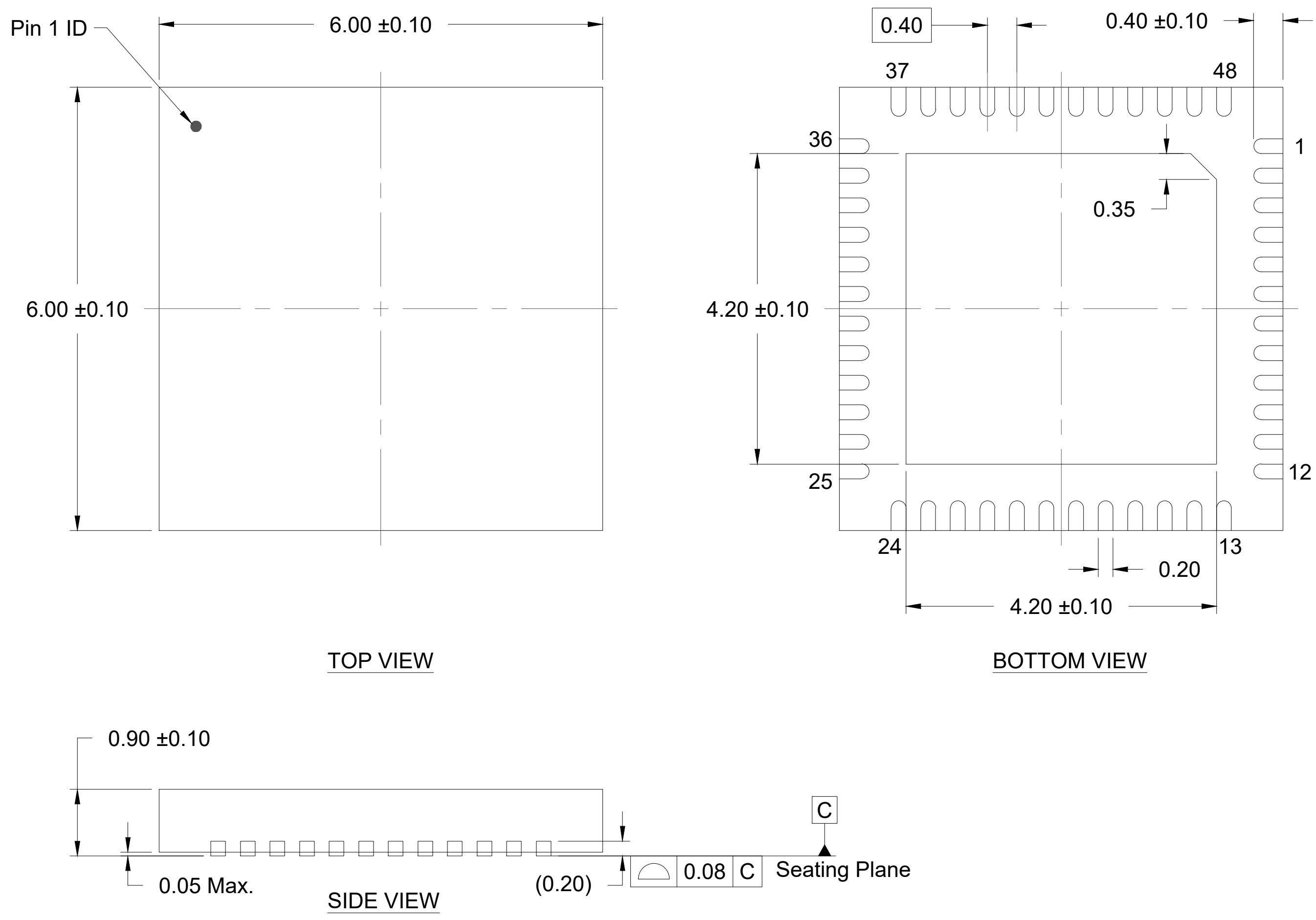
[b] "000" denotes un-programmed parts for user customization.

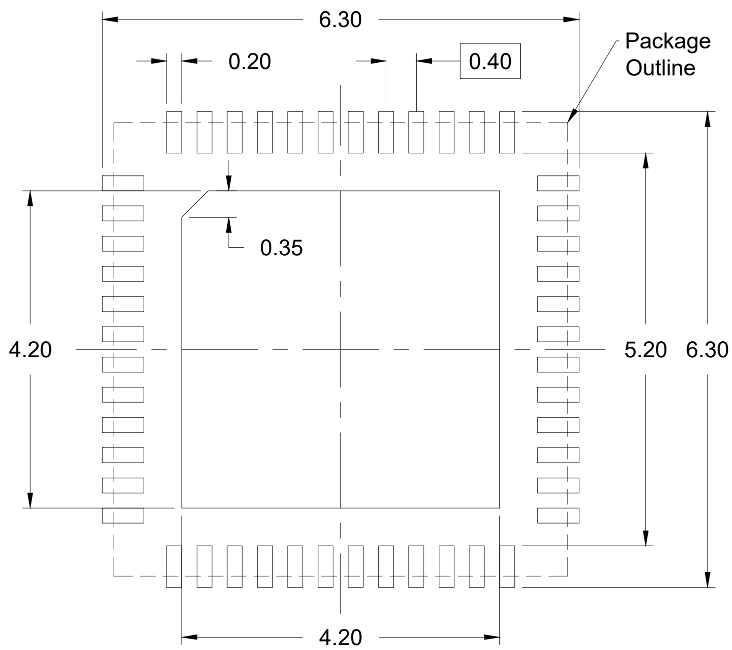
15. Revision History

Revision Date	Description of Change
August 20, 2020	Updated slew rate terminology in section Driving XIN/REF with a CMOS Driver.
October 4, 2019	▪ Updated Absolute Maximum Ratings table. ▪ Updated PCI Express Jitter Performance tables (Table 16 and Table 17). ▪ Updated Electrical Characteristics tables (Table 8, Table 10 and Table 13).
June 19, 2019	▪ PCIe specification updated. ▪ Added recommended power ramp time. ▪ Expanded spread spectrum value range. ▪ I2C tolerant voltage footnote changed to 3.3V. ▪ LVDS Termination section allows AC-coupling for LVDS signals.
August 30, 2018	Updated schematics for Driving XIN/REF with a CMOS Driver and Driving XIN with an LVPECL Driver sections.
July 5, 2018	Removed all references to CLKIN and updated values in electrical tables.
March 16, 2018	Updated Current Consumption, AC Timing, LVDS, and CMOS electrical tables.
December 12, 2017	Initial release.

Package Outline Drawing

Package Code:NDG48P2
48-VFQFPN 6.0 x 6.0 x 0.9 mm Body, 0.4mm Pitch
PSC-4212-02, Revision: 04, Date Created: Sep 28, 2022





RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

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