Description

The 8T49N1012 has one fractional-feedback PLL that can be used for frequency synthesis. It is equipped with two integer and eight fractional output dividers, allowing the generation of up to ten different output frequencies, ranging from 8kHz to 1GHz. Eight of these frequencies are completely independent of each other and the inputs. Two more are related frequencies. The twelve outputs may select among LVPECL, LVDS, HSCL or LVCMOS output levels.

This functionality makes it ideal to be used in any frequency synthesis application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates.

The device supports Output Enable inputs and Lock and LOS status outputs.

The device is programmable through an I^2C interface. It also supports I^2C master capability to allow the register configuration to be read from an external EEPROM.

Typical Applications

- OTN or SONET / SDH equipment Line cards (up to OC-192, and supporting FEC ratios)
- Gigabit and Terabit IP switches / routers
- Wireless base station baseband
- Data communications

Features

- <350fs RMS typical jitter (including spurs), @122.88MHz (12kHz to 20MHz)
- Operating modes: locked to input signal and free-run
- Operates from a 10MHz to 40MHz fundamental-mode crystal
- Accepts one LVPECL, LVDS, LVHSTL, HCSL or LVCMOS input clock
  - Accepts frequencies ranging from 10MHz up to 600MHz
  - Clock input monitoring
- Generates 12 LVPECL / LVDS / HSCL or 24 LVCMOS output clocks
  - Output frequencies ranging from 8kHz up to 1.0GHz (Q[8:11], Differential)
  - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
- Two Output Enable control inputs
- Lock and Loss-of-Signal status outputs
- Programmable output de-skew adjustments in steps as small as 16ps
- Register programmable through I^2C or via external I^2C EEPROM
- Bypass clock paths and Reference Output for system tests
- Power supply modes:
  V_{CC} / V_{CCA} / V_{CCO}
  3.3V / 3.3V / 3.3V
  3.3V / 3.3V / 2.5V
  3.3V / 3.3V / 1.8V (LVCMOS)
  2.5V / 2.5V / 3.3V
  2.5V / 2.5V / 2.5V
  2.5V / 2.5V / 1.8V (LVCMOS)
- -40°C to 85°C ambient operating temperature
- Package: 72QFN, lead-free RoHs (6)

8T49N1012 Block Diagram

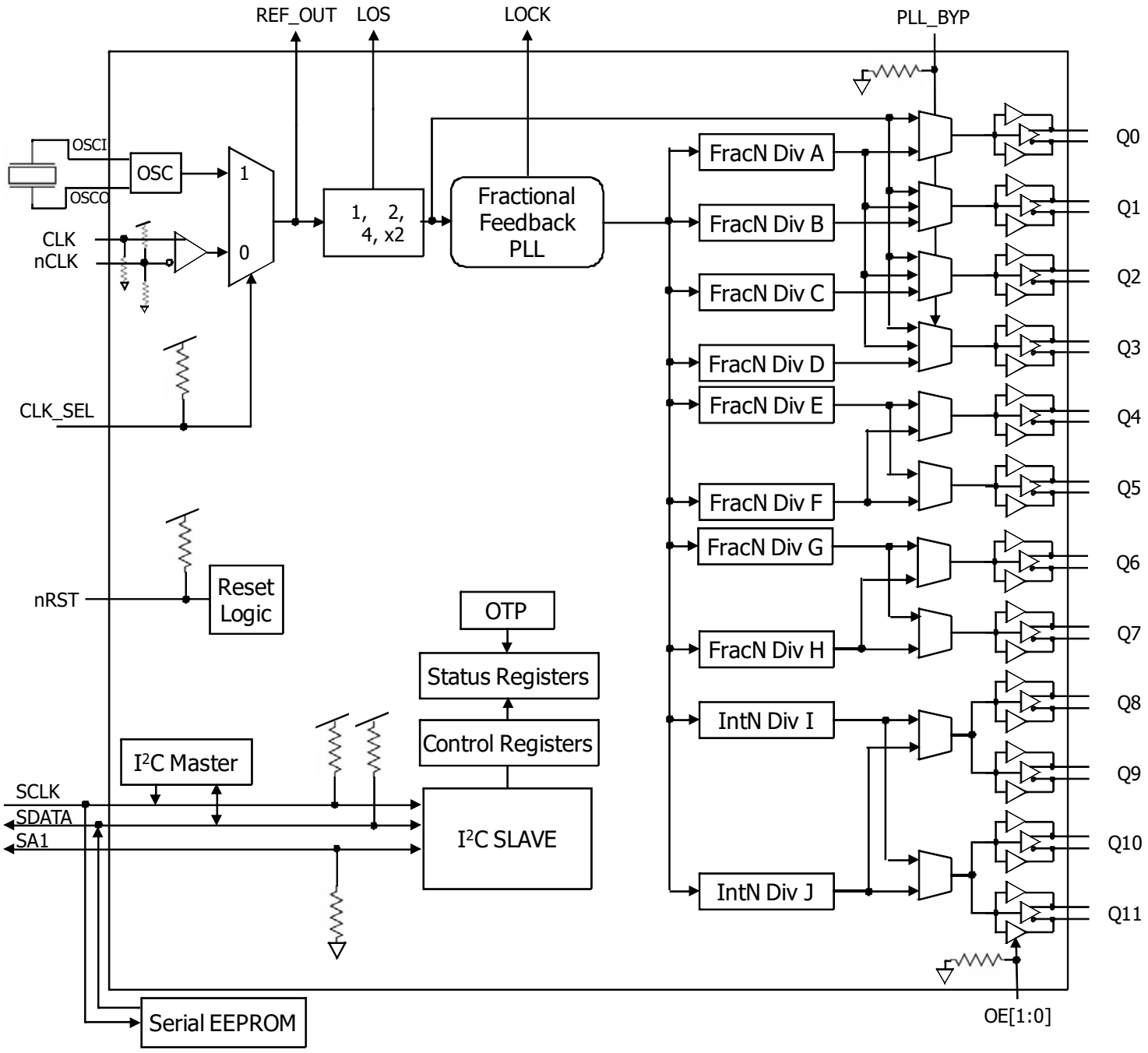


Figure 1. 8T49N1012 Functional Block Diagram

Pin Assignment for 72-pin, 10mm x 10mm VFQFN Package

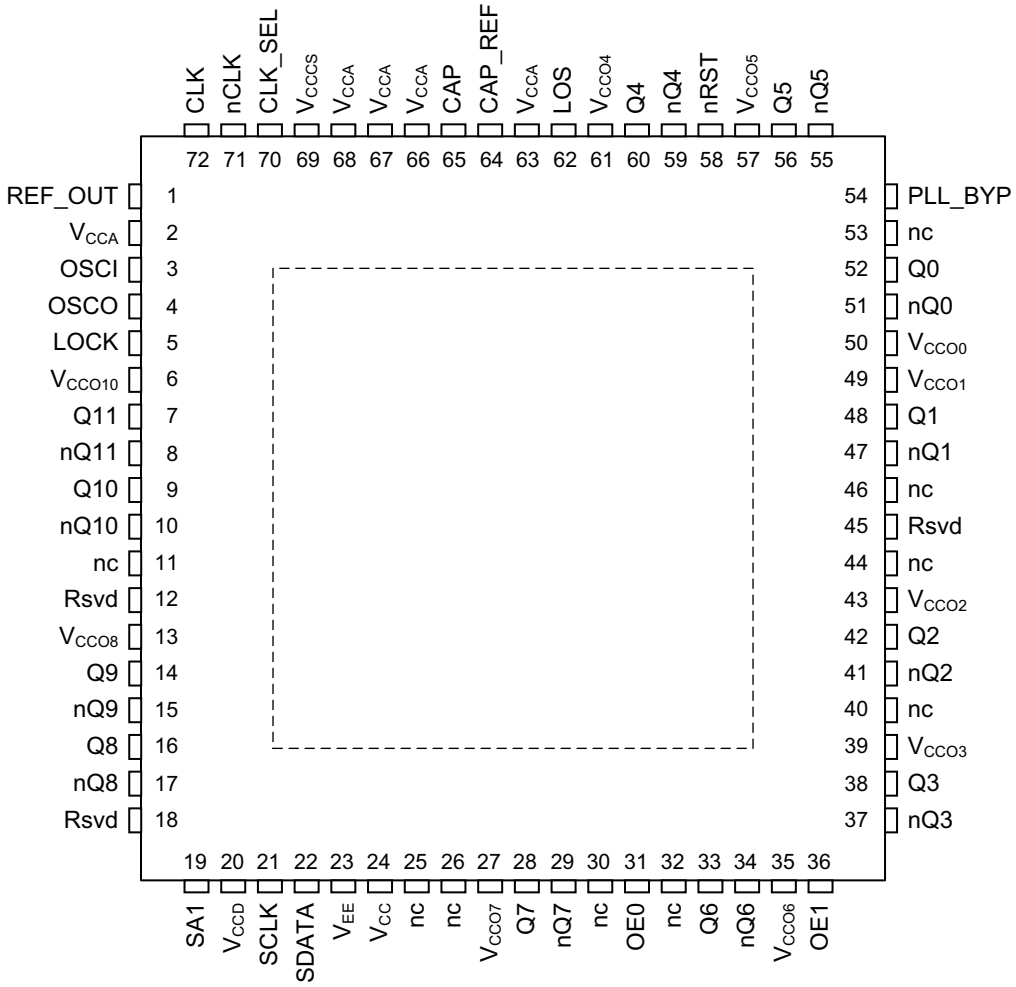


Figure 2. Pinout Drawing

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	REF_OUT	Output		Single-ended REF output. 1.8V LVCMOS/LVTTL interface levels.
2	V_{CCA}	Power		Core analog functions supply pin.
3	OSCI	Input		Crystal Input. Accepts a 10MHz-40MHz reference from a clock oscillator or a 12pF fundamental mode, parallel-resonant crystal.
4	OSCO	Output		Crystal Output. This pin should be connected to a crystal. If an oscillator is connected to OSCI, then this pin must be left unconnected.
5	LOCK	Output		PLL lock indicator. LVCMOS/LVTTL interface levels.
6	V_{CCO10}	Power		Output supply for Q10 and Q11 output clock pairs.
7	Q11	Output		Output Clock 11. Refer to the Output Drivers section for more details.
8	nQ11	Output		Output Clock 11. Refer to the Output Drivers section for more details.
9	Q10	Output		Output Clock 10. Refer to the Output Drivers section for more details.
10	nQ10	Output		Output Clock 10. Refer to the Output Drivers section for more details.
11	nc	Unused		No internal connection.
12	Rsvd	Reserved		Reserved - leave unconnected.
13	V_{CCO8}	Power		Output supply for Q8 and Q9 output clock pairs.
14	Q9	Output		Output Clock 9. Refer to the Output Drivers section for more details.
15	nQ9	Output		Output Clock 9. Refer to the Output Drivers section for more details.
16	Q8	Output		Output Clock 8. Refer to the Output Drivers section for more details.
17	nQ8	Output		Output Clock 8. Refer to the Output Drivers section for more details.
18	Rsvd	Reserved		Reserved - leave unconnected.
19	SA1	Input	Pulldown	I^2C lower address bit A1.
20	V_{CCD}	Power		Core Digital functions supply voltage.
21	SCLK	I/O	Pullup	I^2C interface bi-directional Clock.
22	SDATA	I/O	Pullup	I^2C interface bi-directional Data.
23	V_{EE}	Power		Negative supply voltage.
24	V_{CC}	Power		Core functions supply voltage.
25	nc	Unused		No internal connection.
26	nc	Unused		No internal connection.
27	V_{CCO7}	Power		Output supply for Q7 output clock pair.
28	Q7	Output		Output Clock 7. Refer to the Output Drivers section for more details.
29	nQ7	Output		Output Clock 7. Refer to the Output Drivers section for more details.
30	nc	Unused		No internal connect.
31	OE0	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels.
32	nc	Unused		No internal connection.
33	Q6	Output		Output Clock 6. Refer to the Output Drivers section for more details.
34	nQ6	Output		Output Clock 6. Refer to the Output Drivers section for more details.
35	V_{CCO6}	Power		Output supply for Q6 output clock pair.
36	OE1	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels.
37	nQ3	Output		Output Clock 3. Refer to the Output Drivers section for more details.
38	Q3	Output		Output Clock 3. Refer to the Output Drivers section for more details.

Table 1. Pin Descriptions[1] (Continued)

Number	Name	Type		Description
39	V_{CCO3}	Power		Output supply for Q3 output clock pair.
40	nc	Unused		No internal connection.
41	nQ2	Output		Output Clock 2. Refer to the Output Drivers section for more details.
42	Q2	Output		Output Clock 2. Refer to the Output Drivers section for more details.
43	V_{CCO2}	Power		Output supply for Q2 output clock pair.
44	nc	Unused		No internal connection.
45	Rsvd	Reserved	Pulldown	Reserved - leave unconnected.
46	nc	Unused		No internal connection.
47	nQ1	Output		Output Clock 1. Refer to the Output Drivers section for more details.
48	Q1	Output		Output Clock 1. Refer to the Output Drivers section for more details.
49	V_{CCO1}	Power		Output supply for Q1 output clock pair.
50	V_{CCO0}	Power		Output supply for Q0 output clock pair.
51	nQ0	Output		Output Clock 0. Refer to the Output Drivers section for more details.
52	Q0	Output		Output Clock 0. Refer to the Output Drivers section for more details.
53	nc	Unused		No internal connection.
54	PLL_BYP	Input	Pulldown	Bypass Selection. Allow PLL references to bypass PLL and appear at Q[0:3]. LVTTL / LVCMOS interface levels.
55	nQ5	Output		Output Clock 5. Refer to the Output Drivers section for more details.
56	Q5	Output		Output Clock 5. Refer to the Output Drivers section for more details.
57	V_{CCO5}	Power		Output supply for Q5 output clock pair.
58	nRST	Input	Pullup	Master Reset input. LVTTL / LVCMOS interface levels. 0 = All registers and state machines are reset to their default values 1 = Device runs normally
59	nQ4	Output		Output Clock 4. Refer to the Output Drivers section for more details.
60	Q4	Output		Output Clock 4. Refer to the Output Drivers section for more details.
61	V_{CCO4}	Power		Output supply for Q4 output clock pair.
62	LOS	Output		Loss of reference to PLL indicator. LVCMOS/LVTTL interface levels.
63	V_{CCA}	Power		Core analog function supply voltage.
64	CAP_REF	Analog		PLL External Capacitance reference.
65	CAP	Analog		PLL External Capacitance. A 0.1µF capacitance value across CAP and CAP_REF pins is recommended.
66	V_{CCA}	Power		Core analog function supply voltage.
67	V_{CCA}	Power		Core analog function supply voltage.
68	V_{CCA}	Power		Core analog function supply voltage.
69	V_{CCCS}	Power		Supply voltage for status and control signals: nRST, LOCK, LOS, PLL_BYP, OE[1:0].
70	CLK_SEL	Input	Pullup	Clock select pin: 0: CLK, nCLK 1: XTAL (default)

Table 1. Pin Descriptions[1] (Continued)

Number	Name	Type		Description
71	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{CC}/2$.
72	CLK	Input	Pulldown	Non-inverting differential clock input.
ePAD	V_{EE_EP}	Power		Exposed pad of package. All ground pins and EPAD must be connected before any positive supply voltage is applied.

NOTE 1. *Pullup* and *Pulldown* refer to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics [1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance[2]				3.5		pF
R_{PULLUP}	Internal Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Internal Pulldown Resistor				51		kΩ
C_{PD}	Power Dissipation Capacitance (per output pair)	LVCMOS; Q[0:7]	V_{CCOx} = 3.465V		17		pF
		LVCMOS; Q[8:11]	V_{CCOx} = 3.465V		14		pF
		LVCMOS; Q[0:7]	V_{CCOx} = 2.625V		15		pF
		LVCMOS; Q[8:11]	V_{CCOx} = 2.625V		13		pF
		LVCMOS; [0:7]	V_{CCOx} = 1.89V		15		pF
		LVCMOS; Q[8:11]	V_{CCOx} = 1.89V		11.5		pF
		LVDS, HSCL, LVPECL or Hi-Z; Q[0:7]	V_{CCOx} = 3.465V or 2.625V		4.5		pF
		LVDS, HSCL, LVPECL or Hi-Z; Q[8:11]	V_{CCOx} = 3.465V or 2.625V		2.5		pF
R_{OUT}	Output Impedance	LOCK, LOS	V_{CCCS} = 3.3V		43		Ω
			V_{CCCS} = 2.5V		52		Ω
		Q[0:11], nQ[0:11]	LVCMOS Operation Selected		22		Ω
		REF_OUT			30		Ω

NOTE 1. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.
NOTE 2. This specification does not apply to OSCI and OSCO pins.

Principles of Operation

The 8T49N1012 accepts either a crystal input or a differential input clock. It generates up to twelve output clocks ranging from 8kHz up to 1.0GHz.

The 8T49N1012 has one fractional-feedback PLL that tracks either a crystal or input reference clock. From the output of the PLL a wide range of output frequencies can be simultaneously generated.

The device monitors the input clock and generates an alarm when an input clock or crystal failure is detected.

The PLL provides a frequency reference that is unrelated to the input clock or crystal frequency. The PLL frequency may be used by any of eight fractional output dividers or two Integer output dividers to generate up to 10 different frequencies on the twelve outputs.

The device supports programmable skew adjustment on the eight fractional output dividers.

The device is programmable through an I^2C interface and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory or an external serial I^2C EEPROM.

Bypass Path and Reference Output

For system test purposes, the PLL may be bypassed. When PLL_BYP is asserted the PLL input reference will be presented on the Q0 - Q3 outputs. Note that this frequency represents the selected input frequency after the pre-scaler circuit.

Additionally, the input reference clock or crystal frequency may be enabled on the REF_OUT pin. This is the selected input frequency before the pre-scaler circuit. Note that since REF_OUT is an LVCMOS output, it is limited to ≤ 250MHz. If the selected input frequency is higher than this, REF_OUT must be disabled.

Input Clock Selection and Pre-Scaling

The 8T49N1012 is referenced either to a fundamental mode crystal in the range of 10MHz to 40MHz or to an input reference clock with frequency ranging from 10MHz up to 600MHz. The reference clock input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels. To use LVCMOS inputs, please refer to the Application Note later in this datasheet, *Wiring the Differential Input to Accept Single-Ended Levels* (page 37) for biasing instructions.

The input reference clock does not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ±100ppm or better.

The user selects via the CLK_SEL input pin whether the crystal (CLK_SEL = HIGH) or the CLK/nCLK (CLK_SEL = LOW) is used as the reference frequency. The CLK_SEL input has an internal pull-up so that if it is not connected, the crystal will be selected as the source. The output of this selection logic may be monitored via the REF_OUT pin.

Whichever source is selected is passed to a pre-scaler function which can multiply that frequency by a factor of 2, pass it on directly or divide it by 2 or by 4. For best performance, this pre-scaler should be set to provide the highest frequency less than the 150MHz limit the PLL can accept. This scaled reference may be monitored on the Q[0:3] outputs by use of the PLL_BYP pin or via register control.

Input Clock Monitor

The PLL input (after pre-scaling) is monitored for Loss of Signal (LOS). If no activity has been detected by the PLL on its input within 64 clock periods then the input is considered to have failed and the internal Loss-of-Signal status flag is set and the LOS pin is asserted.

Once a LOS on the selected input reference is detected, the internal LOS alarm will be asserted and it will remain asserted until that PLL input clock returns.

Note that the internal LOS alarm register bit is ‘sticky’. Once asserted it will remain asserted until a ‘1’ has been written to that register bit to clear it. If the LOS condition is still in effect when the ‘sticky’ bit is cleared, then it will immediately re-assert.

The LOS pin is not ‘sticky’ and will directly reflect the current LOS status of the selected input reference.

Loop Bandwidth and Lock Indication

The 8T49N1012 has a fixed loop bandwidth set using internal components of approximately 200kHz.

Once the PLL has locked to the selected input reference, then the internal LOCK status will be set.

The internal lock status will be reflected directly on the LOCK pin and on the internal LOCK status register.

Note that the internal LOCK status register bit is ‘sticky’. Once asserted it will remain asserted until a ‘1’ has been written to that register bit to clear it. If the LOCK condition is still in effect when the ‘sticky’ bit is cleared, then it will immediately re-assert.

Fractional Output Dividers (Div A - Div H)

For the fractional output dividers, the output divide ratio is given by:

Output Divide Ratio = (N.F)x2

N = Integer Part: 4, 5, ...(2^{18}-1)

F = Fractional Part: [0, 1, 2, ...(2^{28}-1)]/(2^{28})

For integer operation (F = 0) of these fractional output dividers, N = 3 is also supported. The max frequency with Integer Divider mode is 667.67MHz, and with Fractional Divider mode is 400MHz.

Integer Output Dividers (Div I & Div J)

Each integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in *Table 3*.

Table 3. Integer Output Divider Ratios

1st-Stage Divide	2nd-Stage Divide	Total Divide	Minimum F_{OUT} MHz	Maximum F_{OUT} MHz
4	1	4	750	1000
5	1	5	600	800
6	1	6	500	666.7
4	2	8	375	500
5	2	10	300	400
6	2	12	250	333.3
4	4	16	187.5	250
5	4	20	150	200
6	4	24	125	166.7
...				
4	131,070	524,280	0.0057	0.0076
5	131,070	655,350	0.0046	0.0061
6	131,070	786,420	0.0038	0.0051

Output Skew Adjustment (Div A - Div H)

For the fractional output dividers Div A through Div H, the user may apply adjustments that are proportional to the period of the clock source driving each output divider. The phase of those divider outputs may be adjusted with a granularity of 1/16th of the VCO period. For example a 4GHz VCO frequency gives a granularity of 16ps. Anywhere from 0 to 15 steps of skew adjustment can be added to the output clock from each fractional output divider.

This is performed by directly writing the required offset (from the nominal rising edge position) in units of 1/16^{th} of the output period into a register. Then the PLL_SYN bit must be toggled to load the new value. The output will then jump directly to that new offset value. For this reason, this adjustment should be made as the output is initially programmed or in high-impedance.

Output Buffers

The Q0 to Q11 clock outputs are provided with register-controlled output buffers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HSCL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V V_{CCO}.

Each output may be enabled or disabled by register bits and/or OE[1:0] pins. When disabled an output will be in a high impedance state.

Each output has the capability of being inverted (180 degree phase shift).

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, skew adjustment, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q and nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Phase-aligned outputs will have increased simultaneous switching currents which can negatively affect phase noise performance and power consumption. It is recommended that use of this selection be kept to a minimum.

Output Enables

Control of output enable for all outputs may be performed either via pin control or via register control as dictated by the OEMODE control bit.

If OEMODE = 0, then the OE[1:0] pins will control the output buffers as indicated in *Table 4*.

If OEMODE = 1, then the OUTEN register bits will control the function of each output buffer individually.

Table 4. Output Enable Pin Functions

OE1	OE0	Description
0	0	All outputs disabled (High-Impedance)
0	1	Q[0:3] enabled; Q[4:11] disabled
1	0	Q[0:3] disabled; Q[4:11] enabled
1	1	All outputs enabled

Power-Saving Modes

To allow the device to consume the least power possible for a given application, the device is divided into several power domains each with its own independent supply pins. Some of the power domains may be powered-down under register control. Note that if the register control is used to disable a power domain, the associated power pin must still have an appropriate voltage applied. Each power domain may be powered with one of the indicated voltages regardless of what voltage is provided to any other domain. Please refer to the Power Calculation section near the end of this document for details on power consumption in a specific configuration.

Table 5. Device Power Domains

Power Pin	Supported Voltages	Power-down Mode	Functions in the Domain
V_{CC}	2.5V, 3.3V	Not Supported	OTP
V_{CCD}	2.5V, 3.3V	Not Supported	Internal Registers
V_{CCA}	2.5V, 3.3V	Not Supported	Input Clock, Crystal and input reference logic, pre-scaler, PLL
V_{CCCS}	1.8V, 2.5V, 3.3V	Not Supported	Output / Input buffers for pins: nRST, CLK_SEL, PLL_BYP, LOCK, LOS, OE[1:0], SA1, SCLK and SDATA
V_{CCO0}	1.8V[1], 2.5V, 3.3V	Supported	Div A, Q0 Output Buffer & Mux
V_{CCO1}	1.8V[1], 2.5V, 3.3V	Supported	Div B, Q1 Output Buffer & Mux
V_{CCO2}	1.8V[1], 2.5V, 3.3V	Supported	Div C, Q2 Output Buffer & Mux
V_{CCO3}	1.8V[1], 2.5V, 3.3V	Supported	Div D, Q3 Output Buffer & Mux
V_{CCO4}	1.8V[1], 2.5V, 3.3V	Supported	Div E, Q4 Output Buffer & Mux
V_{CCO5}	1.8V[1], 2.5V, 3.3V	Supported	Div F, Q5 Output Buffer & Mux
V_{CCO6}	1.8V[1], 2.5V, 3.3V	Supported	Div G, Q6 Output Buffer & Mux
V_{CCO7}	1.8V[1], 2.5V, 3.3V	Supported	Div H, Q7 Output Buffer & Mux
V_{CCO8}	1.8V[1], 2.5V, 3.3V	Supported	Div I, Q8 & Q9 Output Buffers & Muxes
V_{CCO10}	1.8V[1], 2.5V, 3.3V	Supported	Div J, Q10 & Q11 Output Buffers & Muxes

NOTE 1. Operation of 1.8V is only supported when in LVCMOS output mode.

Device Hardware Configuration

The 8T49N1012 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with one complete device configuration. If the device is set to read a configuration from an external, serial EEPROM, then the values read will overwrite the OTP-defined values.

This configuration can be over-written using the serial interface once device initialization is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The 8T49N1012 has an internal power-up reset (POR) circuit and a Master Reset input pin nRST. If either is asserted, the device will be in the Reset State.

For highly programmable devices, it is common practice to reset the device immediately after the initial power-on sequence. IDT recommends connecting the nRST input pin to a programmable logic source for optimal functionality. It is recommended that a minimum pulse width of 10ns be used to drive the nRST input pin.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- All clock outputs will be disabled.
- All alarm status bits will be cleared.

Upon the latter of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load an initial block of its internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory. Once this step is complete, the 8T49N1012 will check the register settings to see if it should load the remainder of its configuration from an external I^2C EEPROM at a defined address or continue loading from OTP. See the section on I^2C Boot Initialization for details on how this is performed.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the selected source and begin operation. Once the PLL is locked, all the output dividers will be synchronized and output skew adjustments can then be applied if desired.

Serial Control Port Description

Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I^{2}C compatible configuration, to allow access to any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details.

The device has the additional capability of becoming a master on the I^{2}C bus only for the purpose of reading its initial register configurations from a serial EEPROM on the I^{2}C bus. Writing of the configuration to the serial EEPROM must be performed by another device on the same I^{2}C bus or pre-programmed into the device prior to assembly.

I^{2}C Mode Operation

The I^{2}C interface is designed to fully support v2.1 of the I^{2}C Specification for Normal and Fast mode operation. The device acts as a slave device on the I^{2}C bus at 100kHz or 400kHz using the address defined in the Serial Interface Control register (0006h), as modified by the SA1 input pin settings. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I^{2}C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

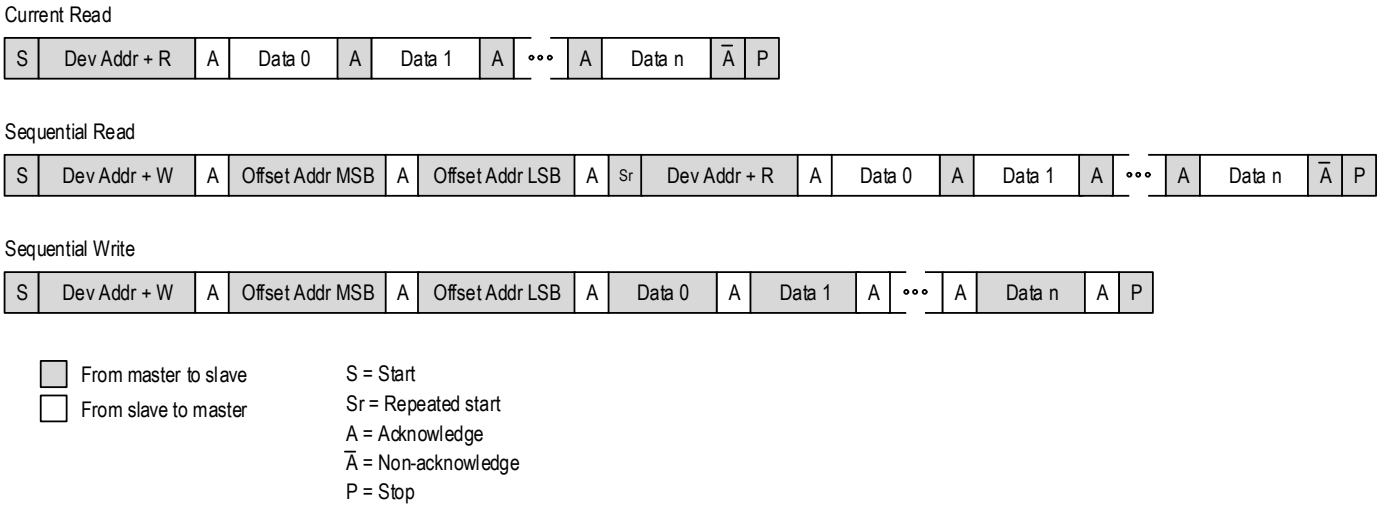


Figure 3. I^{2}C Slave Read and Write Cycle Sequencing

I²C Master Mode

When operating in I²C mode, the 8T49N1012 has the capability to become a bus master on the I²C bus for the purposes of reading its configuration from an external I²C EEPROM. Only a block read cycle will be supported.

As an I²C bus master, the 8T49N1012 will support the following functions:

- 7-bit addressing mode
- Base address register for EEPROM
- Validation of the read block via CCITT-8 CRC check against value stored in last byte (B4h) of EEPROM
- Support for 100kHz and 400kHz operation with speed negotiation. If bit d0 is set at Byte address 05h in the EEPROM, this will shift from 100kHz operation to 400kHz operation.
- Support for 1- or 2-byte addressing mode
- Master arbitration with programmable number of retries
- Fixed-period cycle response timer to prevent permanently hanging the I²C bus.
- Read will abort with an alarm (BOOTFAIL) if any of the following conditions occur: Slave NACK, Arbitration Fail, Collision during Address Phase, CRC failure, Slave Response time-out

The 8T49N1012 will not support the following functions:

- I²C General Call
- Slave clock stretching
- I²C Start Byte protocol
- EEPROM Chaining
- CBUS compatibility
- Responding to its own slave address when acting as a master
- Writing to external I²C devices including the external EEPROM used for booting

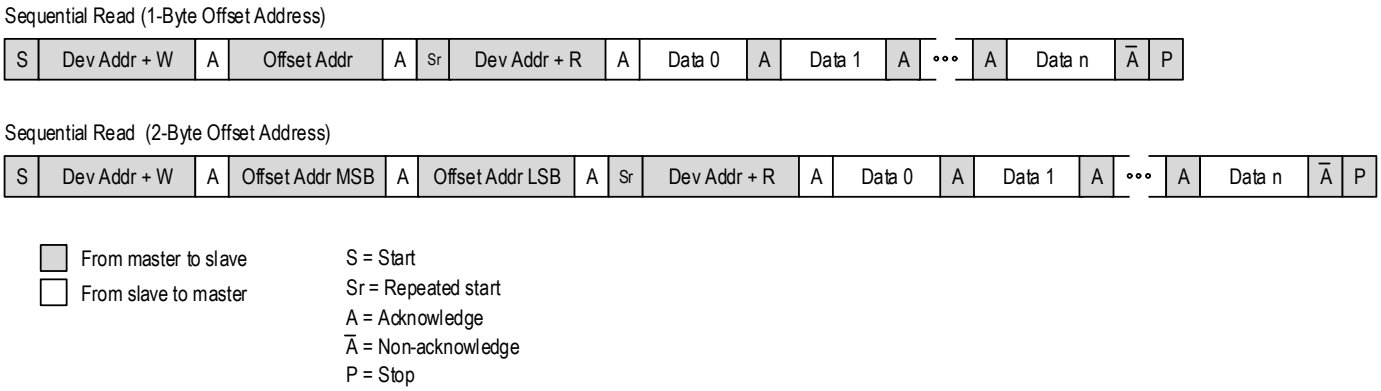


Figure 4. I²C Master Read Cycle Sequencing

I²C Boot-up Initialization Mode

If enabled (via the BOOT_EEP bit in the Startup register), once the nRST input has been deasserted (high) and its internal power-up reset sequence has completed, the device will contend for ownership of the I²C bus to read its initial register settings from a memory location on the I²C bus. The address of that memory location is kept in non-volatile memory in the Startup register. During the boot-up process, the device will not respond to serial control port accesses. Once the initialization process is complete, the contents of any of the device's registers can be altered. It is the responsibility of the user to make any desired adjustments in initial values directly in the serial bus memory.

If a NACK is received to any of the read cycles performed by the device during the initialization process, or if the CRC does not match the one stored in address B4h of the EEPROM the process will be aborted and any uninitialized registers will remain with their default values. The BOOTFAIL bit (0214h) in the Global Status register will also be set in this event.

Contents of the EEPROM should be as shown in *Table 6*.

Table 6. External Serial EEPROM Contents

EEPROM Offset (Hex)	Contents							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00	1	1	1	1	1	1	1	1
01	1	1	1	1	1	1	1	1
02	1	1	1	1	1	1	1	1
03	1	1	1	1	1	1	1	1
04	1	1	1	1	1	1	1	1
05	1	1	1	1	1	1	1	Serial EEPROM Speed Select 0 = 100kHz 1 = 400kHz
06	1	8T49N1012 Device I²C Address [6:2]					1	1
07	0	0	0	0	0	0	0	0
08 - B3	Desired contents of Device Registers 08h - B3							
B4	Serial EEPROM CRC							
B5 - FF	Unused							

Register Descriptions

Table 7A. Register Blocks

Register Ranges Offset (Hex)	Register Block Description
0000 - 0001	Startup Control Registers
0002 - 0005	Device ID Control Registers
0006 - 0007	Serial Interface Control Registers
0008 - 0032	Reserved
0033 - 003E	PLL Divider Control Registers
003F - 0048	Output Buffer Control Registers
0049 - 008C	Output Divider Control Registers
008D - 008F	Output Mux Control Registers
0090- 0091	Divider Power Control Registers
0092 - 0099	Reserved
009A - 009F	PLL Control Registers
00A0- 00A2	Buffer Power Control Registers
00A3 - 01FF	Reserved
0200 - 0203	Interrupt Status Registers
0204- 0212	Reserved
0213 - 0215	Global Status Registers
0216 - 03FF	Reserved

Table 7B. Startup Control Register Bit Field Locations and Descriptions

Startup Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0000	EEP_RTY[4:0]					Rsvd	nBOOT_OTP	nBOOT_EEP
0001	EEP_A15	EEP_ADDR[6:0]						

Startup Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
EEP_RTY[4:0]	R/W	00001b	Select number of times arbitration for the I^2C bus to read the serial EEPROM will be retried before being aborted. Note that this number does not include the original try.
nBOOT_OTP	R/W	Various[1]	Internal One-Time Programmable (OTP) memory usage on power-up: 0 = Load power-up configuration from OTP 1 = Only load 1st eight bytes from OTP
nBOOT_EEP	R/W	Various[1]	External EEPROM usage on power-up: 0 = Load power-up configuration from external serial EEPROM (overwrites OTP values) 1 = Don't use external EEPROM
EEP_A15	R/W	Various[1]	Serial EEPROM supports 15-bit addressing mode (multiple pages).
EEP_ADDR[6:0]	R/W	Various[1]	I^2C base address for serial EEPROM.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1. These values are specific to the device configuration and can be customized when ordering. Refer to the *FemtoClock NG Universal Frequency Translator Ordering Product Information guide* or custom datasheet addendum for more details.

Table 7C. Device ID Control Register Bit Field Locations and Descriptions

Device ID Register Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0002	REV_ID[3:0]				DEV_ID[15:12]			
0003	DEV_ID[11:4]							
0004	DEV_ID[3:0]				DASH_CODE[10:7]			
0005	DASH_CODE[6:0]							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REV_ID[3:0]	R/W	0000b	Device revision.
DEV_ID[15:0]	R/W	060Eh	Device ID code.
DASH_CODE [10:0]	R/W	Various[1]	Device Dash Code. Decimal value assigned by IDT to identify the configuration loaded at the factory. May be over-written by users at any time. Refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* to identify major configuration parameters associated with this Dash Code value.

NOTE 1:These values are specific to the device configuration and can be customized when ordering. Refer to the *FemtoClock NG Universal Frequency Translator Ordering Product Information guide* or custom datasheet addendum for more details.

Table 7D. Serial Interface Control Register Bit Field Locations and Descriptions

Serial Interface Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0006	Rsvd	DEVADD[6:2]					DEVADD[1]	Rsvd
0007	Rsvd							1

Serial Interface Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
DEVDD[6:2]	R/W	Various[1]	Configurable portion of I^2C Base Address (bits 6:2) for this device.
DEVADD[1]	R/O	0b	I^2C Base Address bit 1. This address bit reflects the status of the SA1 external input pin. See *Pin Description and Pin Characteristic Tables* (page 4).
Rsvd	R/O	0b	Reserved.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1. These values are specific to the device configuration and can be customized when ordering. Generic dash codes -900 through -903, -998 and -999 are available and programmed with the default I^2C address of 1111100b.Please refer to the *FemtoClock NG Universal Frequency Translator Ordering Product Information guide* or custom datasheet addendum for more details.

Table 7E. PLL Divider Control Register Bit Field Locations and Descriptions

PLL Divider Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0033	Rsvd							DSM_INT[8]
0034	DSM_INT[7:0]							
0035	DSMFRAC[23:16]							
0036	DSMFRAC[15:8]							
0037	DSMFRAC[7:0]							
0038	Rsvd							
0039	01h							
003A	Rsvd							
003B	Rsvd							
003C	DSM_ORD[1:0]		DCXOGAIN[1:0]		Rsvd	DITHGAIN[2:0]		
003D	Rsvd							
003E	Rsvd							

PLL Divider Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
DSM_INT[8:0]	R/W	02Dh	Integer portion of the Delta-Sigma Modulator value.
DSMFRAC[23:0]	R/W	000000h	Fractional portion of Delta-Sigma Modulator value. Divide this number by 2^{24} to determine the actual fraction.
DSM_ORD[1:0]	R/W	11b	Delta-Sigma Modulator Order for PLL: 00 = Delta-Sigma Modulator disabled 01 = 1st order modulation 10 = 2nd order modulation 11 = 3rd order modulation
DCXOGAIN[1:0]	R/W	01b	Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator: 00 = 0.5 01 = 1 10 = 2 11 = 4
DITHGAIN[2:0]	R/W	000b	Dither Gain setting for Digitally Controlled Oscillator: 000 = No dither 001 = Least Significant Bit (LSB) only 010 = 2 LSBs 011 = 4 LSBs 100 = 8 LSBs 101 = 16 LSBs 110 = 32 LSBs 111 = 64 LSBs
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7F. Output Buffer Control Register Bit Field Locations and Descriptions

Output Buffer Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
003F	Rsvd			OEMODE	OUTEN[11:8]			
0040	OUTEN[7:0]							
0041	Rsvd				POL_Q[11:8]			
0042	POL_Q[7:0]							
0043	OUTMODE11[2:0]			SE_MODE11	OUTMODE10[2:0]			SE_MODE10
0044	OUTMODE9[2:0]			SE_MODE9	OUTMODE8[2:0]			SE_MODE8
0045	OUTMODE7[2:0]			SE_MODE7	OUTMODE6[2:0]			SE_MODE6
0046	OUTMODE5[2:0]			SE_MODE5	OUTMODE4[2:0]			SE_MODE4
0047	OUTMODE3[2:0]			SE_MODE3	OUTMODE2[2:0]			SE_MODE2
0048	OUTMODE1[2:0]			SE_MODE1	OUTMODE0[2:0]			SE_MODE0

Output Buffer Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
OEMODE	R/W	0b	Register or OE[1:0] pins to control Output Enable operation: 0 = OE[1:0] pins will control enabling of the output buffers as shown in *Table 4* 1 = OE[1:0] pins are disabled and Output Enables are controlled by internal registers
OUTEN[11:0]	R/W	fffh	Output Enable control for Clock Outputs Q[0:11], nQ[0:11]: 0 = Qn is in a high-impedance state 1 = Qn is enabled as indicated in appropriate OUTMODEn[2:0] register field
POL_Q[11:0]	R/W	000h	Polarity of Clock Outputs Q[0:11], nQ[0:11]: 0 = Normal polarity 1 = Inverted polarity
OUTMODEm [2:0]	R/W	001b	Output Driver Mode of Operation for Clock Output Pair Qm, nQm: 000 = High-impedance 001 = LVPECL 010 = LVDS 011 = LVCMOS 100 = HCSL 101 - 111 = reserved
SE_MODEm	R/W	0b	Behavior of Output Pair Qm, nQm when LVCMOS operation is selected (Must be 0 if LVDS, HCSL or LVPECL output style is selected): 0 = Qm and nQm are both the same frequency but inverted in phase 1 = Qm and nQm are both the same frequency and phase

Table 7G. Output Divider Control Register Bit Field Locations and Descriptions

Output Divider Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0049	Rsvd						N_DIVA[17]	N_DIVA[16]
004A	N_DIVA[15:8]							
004B	N_DIVA[7:0]							
004C	Rsvd						N_DIVB[17]	N_DIVB[16]
004D	N_DIVB[15:8]							
004E	N_DIVB[7:0]							
004F	Rsvd						N_DIVC[17]	N_DIVC[16]
0050	N_DIVC[15:8]							
0051	N_DIVC[7:0]							
0052	Rsvd						N_DIVD[17]	N_DIVD[16]
0053	N_DIVD[15:8]							
0054	N_DIVD[7:0]							
0055	Rsvd						N_DIVE[17]	N_DIVE[16]
0056	N_DIVE[15:8]							
0057	N_DIVE[7:0]							
0058	Rsvd						N_DIVF[17]	N_DIVF[16]
0059	N_DIVF[15:8]							
005A	N_DIVF[7:0]							
005B	Rsvd						N_DIVG[17]	N_DIVG[16]
005C	N_DIVG[15:8]							
005D	N_DIVG[7:0]							
005E	Rsvd						N_DIVH[17]	N_DIVH[16]
005F	N_DIVH[15:8]							
0060	N_DIVH[7:0]							
0061	Rsvd						N1_DIVI[1:0]	
0062	N2_DIVI[15:8]							
0063	N2_DIVI[7:0]							
0064	Rsvd						N1_DIVJ[1:0]	
0065	N2_DIVJ[15:8]							
0066	N2_DIVJ[7:0]							
0067	Rsvd				F_DIVA[27:24]			
0068	F_DIVA[23:16]							
0069	F_DIVA[15:8]							
006A	F_DIVA[7:0]							
006B	Rsvd				F_DIVB[27:24]			
006C	F_DIVB[23:16]							
006D	F_DIVB[15:8]							
006E	F_DIVB[7:0]							
006F	Rsvd				F_DIVC[27:24]			
0070	F_DIVC[23:16]							
0071	F_DIVC[15:8]							

Output Divider Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0072	F_DIVC[7:0]							
0073	Rsvd				F_DIVD[27:24]			
0074	F_DIVD[23:16]							
0075	F_DIVD[15:8]							
0076	F_DIVD[7:0]							
0077	Rsvd				F_DIVE[27:24]			
0078	F_DIVE[23:16]							
0079	F_DIVE[15:8]							
007A	F_DIVE[7:0]							
007B	Rsvd				F_DIVF[27:24]			
007C	F_DIVF[23:16]							
007D	F_DIVF[15:8]							
007E	F_DIVF[7:0]							
007F	Rsvd				F_DIVG[27:24]			
0080	F_DIVG[23:16]							
0081	F_DIVG[15:8]							
0082	F_DIVG[7:0]							
0083	Rsvd				F_DIVH[27:24]			
0084	F_DIVH[23:16]							
0085	F_DIVH[15:8]							
0086	F_DIVH[7:0]							
0087	FINE_C[3:0]				FINE_A[3:0]			
0088	FINE_D[3:0]				FINE_B[3:0]			
0089	FINE_G[3:0]				FINE_E[3:0]			
008A	FINE_H[3:0]				FINE_F[3:0]			
008B	Rsvd							
008C	Rsvd							

Output Divider Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
N1_DIVm[1:0]	R/W	10b	1st Stage Output Divider Ratio for Integer Output Dividers I and J: 00 = /5 01 = /6 10 = /4 11 = Output Qm, nQm not switching
N2_DIVm[15:0]	R/W	0002h	2nd Stage Output Divider Ratio for Integer Output Dividers I and J: Actual divider ratio is 2x the value written here. A value of 0 in this register will bypass the second stage of the divider.
N_DIVm[17:0]	R/W	00008h	Integer Portion of Output Divider Ratio for Fractional Output Dividers A - H: Values of 0, 1 or 2 cannot be written to this register. Actual integer portion is 2x the value written here.

Output Divider Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
F_DIVm[27:0]	R/W	0000000h	Fractional Portion of Output Divider Ratio for Fractional Output Dividers A - H: Actual fractional portion is 2x the value written here. Fraction = (F_DIVm * 2) * 2^{-28}
FINE_m[3:0]	R/W	0100b	Number of 1/16ths of the VCO clock period to add to the phase of a Fractional Output Divider A-H. The PLL_SYN bit must be toggled to make this value take effect.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7H. Output Mux Control Register Bit Field Locations and Descriptions

Output Mux Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
008D	Rsvd							PLL_SYN
008E	Rsvd						MUX_10_11	MUX_8_9
008F	MUX_7	MUX_6	MUX_5	MUX_4	MUX_3	MUX_2	MUX_1	Rsvd

Output Mux Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PLL_SYN	R/W	0b	Output Synchronization Control. Setting this bit from 0→1 will cause the output divider(s) to be held in reset. Setting this bit from 1→0 will release all the output divider(s) to run from the same point in time with the output skew adjustment reset to 0.
MUX_10_11	R/W	0b	Output Divider selection for Output Q10, nQ10 and Q11, nQ11: 0 = Output of Integer Divider J is used 1 = Output of Integer Divider I is used
MUX_8_9	R/W	0b	Output Divider selection for Output Q8, nQ8 and Q9, nQ9: 0 = Output of Integer Divider I is used 1 = Output of Integer Divider J is used
MUX_7	R/W	0b	Output Divider selection for Output Q7, nQ7: 0 = Output of Fractional Divider H is used 1 = Output of Fractional Divider G is used
MUX_6	R/W	0b	Output Divider selection for Output Q6, nQ6: 0 = Output of Fractional Divider G is used 1 = Output of Fractional Divider H is used
MUX_5	R/W	0b	Output Divider selection for Output Q5, nQ5: 0 = Output of Fractional Divider F is used 1 = Output of Fractional Divider E is used
MUX_4	R/W	0b	Output Divider selection for Output Q4, nQ4: 0 = Output of Fractional Divider E is used 1 = Output of Fractional Divider F is used
MUX_3	R/W	0b	Output Divider selection for Output Q3, nQ3: 0 = Output of Fractional Divider D is used 1 = Output of Fractional Divider A is used
MUX_2	R/W	0b	Output Divider selection for Output Q2, nQ2: 0 = Output of Fractional Divider C is used 1 = Output of Fractional Divider A is used
MUX_1	R/W	0b	Output Divider selection for Output Q1, nQ1: 0 = Output of Fractional Divider B is used 1 = Output of Fractional Divider A is used
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7I. Divider Power Control Register Bit Field Locations and Descriptions

Divider Power Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0090	Rsvd						PWR_DIVJ	PWR_DIVI
0091	PWR_DIVH	PWR_DIVG	PWR_DIVF	PWR_DIVE	PWR_DIVD	PWR_DIVC	PWR_DIVB	PWR_DIVA

Divider Power Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PWR_DIVm	R/W	0b	Power-Down Control for Output Divider m: 0 = Output Divider m operating normally 1 = Output Divider m powered-down
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7J. PLL Control Register Bit Field Locations and Descriptions

Please contact IDT through one of the methods listed on the last page of this datasheet for details on how to set these fields for a particular user configuration.

PLL Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
009A	CPSET[2:0]			RS[1:0]		CP[1:0]		WPOST
009B	Rsvd		Rsvd		Rsvd	Rsvd	DLCNT	DBITM
009C	Rsvd		VCOMAN	DBIT1[4:0]				
009D	Rsvd			DBIT2[4:0]				
009E	Rsvd			PLL_BYP	Rsvd	REF_OE	P_MODE[1:0]	
009F	Rsvd							

PLL Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
CPSET[2:0]	R/W	100b	Charge Pump Current Setting for PLL: 000 = 110µA 001 = 220µA 010 = 330µA 011 = 440µA 100 = 550µA 101 = 660µA 110 = 770µA 111 = 880µA
RS[1:0]	R/W	01b	Internal Loop Filter Series Resistor Setting for PLL: 00 = 330Ω 01 = 640Ω 10 = 1.2kΩ 11 = 1.79kΩ
CP[1:0]	R/W	01b	Internal Loop Filter Parallel Capacitor Setting for PLL: 00 = 40pF 01 = 80pF 10 = 140pF 11 = 200pF
WPOST	R/W	1b	Internal Loop Filter 2nd Pole Setting for PLL: 0 = Rpost = 497Ω, Cpost = 40pF 1 = Rpost = 1.58kΩ, Cpost = 40pF
DLCNT	R/W	1b	Digital Lock Count Setting for PLL. Set to 0 if external capacitor (CAP) for PLL is >95nF, otherwise set to 1: 0 = 1 ppm accuracy 1 = 16 ppm accuracy
DBITM	R/W	0b	Digital Lock Manual Override Setting for PLL: 0 = Automatic Mode 1 = Manual Mode
VCOMAN	R/W	1b	Manual Lock Mode VCO Selection Setting for PLL: 0 = VCO2 1 = VCO1
DBIT1[4:0]	R/W	01011b	Manual Mode Digital Lock Control Setting for VCO1 in PLL.
DBIT2[4:0]	R/W	00000b	Manual Mode Digital Lock Control Setting for VCO2 in PLL.
PLL_BYP	R/W	0b	PLL Bypass mode (same function as PLL_BYP pin): 0 = Q[0:3]outputs operate normally 1 = Q[0:3] outputs driven by PLL input reference clock

PLL Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REF_OE	R/W	0b	Enable Reference Output pin: 0 = REF_OUT pin is high-impedance 1 = REF_OUT pin is driven from the input reference mux with either the direct crystal frequency or the direct CLK input reference frequency (as controlled by the CLK_SEL pin)
P_MODE[1:0]	R/W	11b	Pre-Scaler Mode Selection: 00 = Selected reference input is driven directly to the PLL (divide-by-1) 01 = Selected reference input is divided-by-2 before being driven to the PLL 10 = Selected reference input is divided-by-4 before being driven to the PLL 11 = Selected reference input is multiplied-by-2 before being driven to the PLL
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7K. Buffer Power Control Register Bit Field Locations and Descriptions

The power controls below will disable specific logic blocks by turning-off the regulators associated with those logic blocks. The associated power supply pin must remain powered, but minimal current will be drawn. The user must ensure that appropriate control bits are set elsewhere to ensure the powered-down functions are not selected to drive other, still enabled, output paths.

Buffer Power Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00A0	PATHH_OFF	PATHG_OFF	PATHF_OFF	PATHE_OFF	PATHD_OFF	PATHC_OFF	PATHB_OFF	PATHA_OFF
00A1	Rsvd			REF_OFF	Rsvd		PATHJ_OFF	PATHI_OFF
00A2	Rsvd					Rsvd	DSM_OFF	Rsvd

Buffer Power Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PATHH_OFF	R/W	0b	Power Control for Div H, Q7, nQ7 output buffer and associated output mux (Associated supply pin: V_{CCO7}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHG_OFF	R/W	0b	Power Control for Div G, Q6, nQ6 output buffer and associated output mux (Associated supply pin: V_{CCO6}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHF_OFF	R/W	0b	Power Control for Div F, Q5, nQ5 output buffer and associated output mux (Associated supply pin: V_{CCO5}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHE_OFF	R/W	0b	Power Control for Div E, Q4, nQ4 output buffer and associated output mux (Associated supply pin: V_{CCO4}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHD_OFF	R/W	0b	Power Control for Div D, Q3, nQ3 output buffer and associated output mux (Associated supply pin: V_{CCO3}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHC_OFF	R/W	0b	Power Control for Div C, Q2, nQ2 output buffer and associated output mux (Associated supply pin: V_{CCO2}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHB_OFF	R/W	0b	Power Control for Div B, Q1, nQ1 output buffer and associated output mux (Associated supply pin: V_{CCO1}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHA_OFF	R/W	0b	Power Control for Div A, Q0, nQ0 output buffer and associated output mux (Associated supply pin: V_{CCO0}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHI_OFF	R/W	0b	Power Control for Div I, Q8, nQ8 output buffer, Q9, nQ9 output buffer and associated output mux (Associated supply pin: V_{CCO8}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
PATHJ_OFF	R/W	0b	Power Control for Div J, Q10, nQ10 output buffer, Q11, nQ11 output buffer and associated output mux (Associated supply pin: V_{CCO10}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down

Buffer Power Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REF_OFF	R/W	0b	Power Control for REF_OUT output buffer (Associated supply pin: V_{CCCS}): 0 = Regulator enabled & logic operates normally 1 = Regulator disabled and logic powered down
DSM_OFF	R/W	0b	Power Control for PLL Fractional Feedback Divider (Associated supply pin: V_{CCD}): 0 = Feedback Divider in Fractional Mode 1 = Feedback Divider in Integer Mode; some power savings will be realized
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7L. Interrupt Status Register Bit Field Locations and Descriptions

This register contains' sticky' bits for tracking the status of the various alarms. Whenever an alarm occurs, the appropriate Interrupt Status bit will be set. The Interrupt Status bit will remain asserted even after the original alarm goes away. The Interrupt Status bits remain asserted until explicitly cleared by a write of a '1' to the bit over the serial port. This type of functionality is referred to as Read / Write-1-to-Clear (R/W1C). Note that the alarm pin is not 'sticky' but reflects the real-time status of the appropriate alarm.

Interrupt Status Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0200	Rsvd							
0201	Rsvd						LOL_INT	LOS_INT
0202	Rsvd							Rsvd
0203	Rsvd							

Interrupt Status Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
LOL_INT	R/W1C	0b	Interrupt Status Bit for Loss-of-Lock on PLL: 0 = No Loss-of-Lock alarm flag on PLL has occurred since the last time this register bit was cleared. 1 = At least one Loss-of-Lock alarm flag on PLL has occurred since the last time this register bit was cleared.
LOS_INT	R/W1C	0b	Interrupt Status Bit for PLL Input Reference Clock: 0 = No Loss-of Signal (LOS) alarm has occurred since the last time this register bit was cleared. 1 = At least one LOS alarm flag has occurred since the last time this register bit was cleared.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7M. Global Status Register Bit Field Locations and Descriptions

Global Status Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0213	Rsvd		Rsvd					
0214	Rsvd					Rsvd	Rsvd	BOOTFAIL
0215	Rsvd	Rsvd	Rsvd	Rsvd	nEEP_CRC	Rsvd	Rsvd	EEPDONE

Global Interrupt Status Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
BOOTFAIL	R/O	-	Reading of Serial EEPROM failed. Once set this bit is only cleared by reset.
nEEP_CRC	R/O	-	EEPROM CRC Error (Active Low): 0 = EEPROM was detected and read, but CRC check failed - please reset the device via the nRST pin to retry (serial port is locked) 1 = No EEPROM CRC Error
EEPDONE	R/O	-	Serial EEPROM Read cycle has completed. Once set this bit is only cleared by reset.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CCX}	3.63V
Inputs, V_I OSCI Other Input	 0V to 2V -0.5V to V_{CCX}+ 0.5V
Outputs, V_O (Q[0:11], nQ[0:11])	-0.5V to V_{CCOx} + 0.5V
Outputs, V_O (LOS, LOCK, REF_OUT)	-0.5V to V_{CCCS} + 0.5V
Outputs, V_O (SCLK, SDATA)	-0.5V to V_{CCD} + 0.5V
Outputs, I_O (Q[0:11], nQ[0:11]) Continuous Current Surge Current	 40mA 65mA
Outputs, I_O (REF_OUT, LOS, LOCK, SDATA, SCLK) Continuous Current Surge Current	 8mA 13mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE: V_{CCOx} denotes: V_{CCO0} through V_{CCO8} and V_{CCO10}.

Supply Voltage Characteristics

Table 8A. Power Supply Characteristics, V_{CCX}[1] = 3.3V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CCX}[1]	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{CCX}[2]	Core Supply Current			18	28	mA
I_{CCA}	Analog Supply Current	All Functions Enabled[3]		140	170	mA

NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE 2. I_{CCX} denotes the sum of: I_{CCD}, I_{CC}, I_{CCCS}.
NOTE 3. REF_OUT is disabled to high-impedance.

Table 8B. Power Supply Characteristics, V_{CCX}[1] = 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CCX}[1]	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{CCX}[2]	Core Supply Current			17	26	mA
I_{CCA}	Analog Supply Current	All Functions Enabled[3]		137	160	mA

NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE 2. I_{CCX} denotes the sum of: I_{CCD}, I_{CC}, I_{CCCS}.
NOTE 3. REF_OUT is disabled to high-impedance.

Table 8C. Maximum Output Supply Current, V_{EE} = 0V, T_A = -40°C to 85°C[1, 2]

Symbol	Parameter	Test Conditions	V_{CCOx}[3] = 3.3V ±5%				V_{CCOx}[3] = 2.5V ±5%				V_{CCOx} = 1.8V ±5%[3]	Units
			LVPECL	LVDS	HCSL	LVCMOS	LVPECL	LVDS	HCSL	LVCMOS	LVCMOS	
I_{CCO0}	Q0, nQ0 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO1}	Q1, nQ1 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO2}	Q2, nQ2 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO3}	Q3, nQ3 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO4}	Q4, nQ4 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO5}	Q5, nQ5 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO6}	Q6, nQ6 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO7}	Q7, nQ7 Output Supply Current	Outputs Unloaded	71	81	71	72	58	66	58	56	48	mA
I_{CCO8}[4]	Q[8:9], nQ[8:9] Outputs Supply Current	Outputs Unloaded	67	86	67	72	50	66	50	53	42	mA
I_{CCO10}[4]	Q[10:11], nQ[10:11] Outputs Supply Current	Outputs Unloaded	67	86	67	72	50	66	50	53	42	mA

NOTE 1. Internal dynamic switching current at maximum f_{OUT} is included.
NOTE 2. Currents per I_{CCO}.
NOTE 3. V_{CCOx} denotes: V_{CCO0} through V_{CCO8} and V_{CCO10}.
NOTE 4. Supply current specifications refer to two output pairs (Q[8:9] or Q[10:11]) being driven by one divider (Divider I or J).

DC Electrical Characteristics

Table 9A. LVCMOS/LVTTL Control/Status Signals DC Characteristics, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CCCS} = 3.3V	2		V_{CCX} +0.3	V
			V_{CCCS} = 2.5V	1.7		V_{CCX} +0.3	V
			V_{CCCS} = 1.8V	1.2		V_{CCX} +0.3	V
V_{IL}	Input Low Voltage		V_{CCCS} = 3.3V	-0.3		0.8	V
			V_{CCCS} = 2.5V	-0.3		0.7	V
			V_{CCCS} = 1.8V	-0.3		0.3	V
I_{IH}	Input High Current	PLL_BYP, SA1, OE1, OE0	V_{CCCS} = V_{IN} = 3.465V or 2.625V or 1.9V			150	µA
		nRST, SDATA, CLK_SEL, SCLK	V_{CCCS} = V_{IN} = 3.465V or 2.625V or 1.9V			5	µA
I_{IL}	Input Low Current	PLL_BYP, SA1, OE1, OE0	V_{CCCS} = 3.465V or 2.625V or 1.9V, V_{IN} = 0V	-5			µA
		nRST, SDATA, CLK_SEL, SCLK	V_{CCCS} = 3.465V or 2.625V or 1.9V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	LOS, LOCK, SDATA,[1] SCLK	V_{CCCS} = 3.3V ±5%, I_{OH} = -2mA	2.6			V
		LOS, LOCK, SDATA,[1] SCLK	V_{CCCS} = 2.5V ±5%, I_{OH} = -2mA	1.8			V
		REF_OUT[2]	I_{OH} = -2mA	1.45			V
V_{OL}	Output Low Voltage	LOS, LOCK, SDATA[1], SCLK	V_{CCCS} = 3.3V ±5% or 2.5V ±5%, I_{OL} = 2mA			0.4	V
		REF_OUT[2]	I_{OL} = 2mA			0.45	V

NOTE 1. Use of external pull-up resistor is recommended.

NOTE 2. REF_OUT is internally regulated 1.8V output.

Table 9B. Differential Input DC Characteristics, V_{CCA} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{CCA} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK	V_{CCA} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nCLK	V_{CCA} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage[1]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[1, 2]			V_{EE}		V_{CCA} – 1.2	V

NOTE 1. V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CCA}.

NOTE 2. Common mode voltage is defined as the cross-point.

Table 9C. LVPECL DC Characteristics, V_{CCOx}[1] = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[1] = 3.3V±5%			V_{CCOx}[1] = 2.5V±5%			Units
			Minimum	Typical	Maximum	Minimum	Typical	Maximum	
V_{OH}	Output High Voltage[2]		V_{CCOx} - 1.3		V_{CCOx} - 0.8	V_{CCOx} - 1.4		V_{CCOx} - 0.9	V
V_{OL}	Output Low Voltage[2]		V_{CCOx} - 1.95		V_{CCOx} - 1.75	V_{CCOx} - 1.95		V_{CCOx} - 1.75	V

NOTE 1. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.
NOTE 2. Outputs terminated with 50Ω to V_{CCOx} – 2V.

Table 9D. LVDS DC Characteristics, V_{CCX}[1] = 3.3V ±5% or 2.5V ±5%, V_{CCOx}[2] = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C[3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		195		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE 2. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.
NOTE 3. Terminated 100Ω across Qx and nQx.

Table 9E. LVCMOS Clock Output DC Characteristics, V_{CCX}[1] = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C [2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	Qx, nQx	V_{CCOx} = 3.3V±5%, I_{OH} = -8mA	2.6			V
V_{OL}	Output Low Voltage	Qx, nQx	V_{CCOx} = 3.3V±5%, I_{OL} = 8mA			0.4	V
V_{OH}	Output High Voltage	Qx, nQx	V_{CCOx} = 2.5V±5%, I_{OH} = -8mA	1.8			V
V_{OL}	Output Low Voltage	Qx, nQx	V_{CCOx} = 2.5V±5%, I_{OL} = 8mA			0.4	V
V_{OH}	Output High Voltage	Qx, nQx	V_{CCOx} = 1.8V±5%, I_{OH} = -2mA	V_{CCOx} – 0.45			V
V_{OL}	Output Low Voltage	Qx, nQx	V_{CCOx} = 1.8V±5%, I_{OL} = 2mA			0.45	V

NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE 2. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.

Table 10. Input Frequency Characteristics, V_{CCX} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency[1]	OSCI, OSCO	Using a crystal (See *Table 11, Crystal Characteristics*)	10		40	MHz
			Overdriving Crystal Input, Doubler Logic Enabled[2]	10		62.5	MHz
			Overdriving Crystal Input, Doubler Logic Disabled[2]	10		125	MHz
		CLK, nCLK		10		600	MHz
f_{SCLK}	Serial Port Clock SCLK (slave mode)	I^2C Operation		100		400	kHz

NOTE 1. For the input reference frequency, the divider values must be set for the VCO to operate within its supported range.

NOTE 2. For optimal noise performance, the use of a quartz crystal is recommended. Refer to Overdriving the XTAL Interface in the Applications Information section.

Table 11. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)			15		Ω
Load Capacitance (C_L)			12		pF
Frequency Stability (total)		-100		100	ppm

AC Electrical Characteristics

Table 12A. AC Characteristics, V_{CCX}[1] = 3.3V ±5% or 2.5V ±5%, V_{CCOx}[2] = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[3]

Symbol	Parameter			Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Operating Frequency				3000		4000	MHz
f_{REF}	PLL Input Reference Frequency				10		150	MHz
f_{OUT}	Output Frequency	LVPECL, LVDS, HCSL	Q[8:11], nQ[8:11]	Integer Divider	0.008		1000	MHz
			Q[0:7], nQ[0:7]	Integer Output Dividers with No Skew Adjustment	0.008		666.67	MHz
			Q[0:7], nQ[0:7]	Outputs Fractional Divide and/or Added Skew Delay	0.008		400	MHz
		LVCMOS	Q[0:11], nQ[0:11]		0.008		250	MHz
			REF_OUT		10		250	MHz
t_R / t_F	Output Rise and Fall Times	LVPECL		20% to 80%, F_{OUT} < 666MHz	250		650	ps
				20% to 80%, $F_{OUT} \geq$ 666MHz	180		450	ps
		LVDS		20% to 80%	100		460	ps
		HCSL		20% to 80%	130		600	ps
		LVCMOS[4, 5]	Q[0:11], nQ[0:11]	20% to 80%, V_{CCOx} = 3.3V	160		630	ps
			Q[0:11], nQ[0:11]	20% to 80%, V_{CCOx} = 2.5V	160		620	ps
			Q[0:11], nQ[0:11]	20% to 80%, V_{CCOx} = 1.8V	190		700	ps
			REF_OUT	20% to 80%	210		740	ps
SR	Output Slew Rate[6]	LVPECL		Measured on Differential Waveform, ±150mV from Center	1		4	V/ns
		LVDS		Measured on Differential Waveform, ±150mV from Center	0.5		4	V/ns
		HCSL		Measured on Differential Waveform, ±150mV from Center, V_{CCOx} = 2.5V, $f_{OUT} \leq$ 125MHz	1.5		4	V/ns
				Measured on Differential Waveform, ±150mV from Center, V_{CCOx} = 3.3V, $f_{OUT} \leq$ 125MHz	2.5		5.5	V/ns
*t*sk(b)	Bank Skew[7]	LVPECL	Q8, nQ8; Q9, nQ9[8, 9, 10]				75	ps
			Q10, nQ10; Q11, nQ11[8, 9, 10]				75	ps
		LVDS	Q8, nQ8; Q9, nQ9[8, 9, 10]				75	ps
			Q10, nQ10; Q11, nQ11[8, 9, 10]				75	ps
		HCSL	Q8, nQ8; Q9, nQ9[8, 9, 10]				75	ps
			Q10, nQ10; Q11, nQ11[8, 9, 10]				75	ps
		LVCMOS	Q8, nQ8; Q9, nQ9[4, 8, 9, 11]				115	ps
			Q10, nQ10; Q11, nQ11[4, 8, 9, 11]				115	ps

Table 12A. AC Characteristics, V_{CCX}[1] = 3.3V ±5% or 2.5V ±5%, V_{CCOx}[2] = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[3] (Continued)

Symbol	Parameter			Test Conditions	Minimum	Typical	Maximum	Units
odc	Output Duty Cycle[12]	LVPECL, LVDS, HCSL		$f_{OUT} \leq 666.667MHz$	45	50	55	%
				$f_{OUT} > 666.667MHz$	40	50	60	%
		LVCMOS	Q[0:11], nQ[0:11]		40	50	60	%
			REF_OUT	$f_{OUT} \leq 62.5MHz$[13]	40		60	%
Φ_{SSB}(1k)	Single Sideband Phase Noise[14]		1kHz	122.88MHz Output		-113		dBc/Hz
Φ_{SSB}(10k)			10kHz	122.88MHz Output		-130		dBc/Hz
Φ_{SSB}(100k)			100kHz	122.88MHz Output		-137		dBc/Hz
Φ_{SSB}(1M)			1MHz	122.88MHz Output		-149		dBc/Hz
Φ_{SSB}(10M)			10MHz	122.88MHz Output		-155		dBc/Hz
Φ_{SSB}(30M)			≥30MHz	122.88MHz Output		-156		dBc/Hz
	Spurious Limit at Offset		≥800kHz	122.88MHz Output[15]		-85		dBc
*t*startup	Startup Time		Internal OTP Startup[16]	from V_{CCX} >80% to First Output Clock Edge		110	150	ms
			External EEPROM Startup[16, 17]	I^2C Frequency = 100kHz; from V_{CCX} >80% to First Output Clock Edge (0 retries)		150	200	ms
				I^2C Frequency = 400kHz; from V_{CCX} >80% to First Output Clock Edge (0 retries)		130	150	ms
				I^2C Frequency = 100kHz; from V_{CCX} >80% to First Output Clock Edge (31 retries)		925	1200	ms
				I^2C Frequency = 400kHz; from V_{CCX} >80% to First Output Clock Edge (31 retries)		360	500	ms

NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.

NOTE 2. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.

NOTE 3. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 4. Appropriate SE_MODE bit must be configured to select phase-aligned or phase-inverted operation.

NOTE 5. All Q and nQ outputs in phase-inverted operation.

NOTE 6. Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crosspoint.

NOTE 7. Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 8. This parameter is guaranteed by characterization. Not tested in production.

NOTE 9. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 10. Measured at the output differential crosspoints.

NOTE 11. Measured at V_{CCOx}/2 of the rising edge. All Qx and nQx outputs phase-aligned.

NOTE 12. Duty Cycle of bypassed signals (input reference clocks or crystal input) is not adjusted by the device.

NOTE 13. REF_OUT output duty cycle characterized with CLK input duty cycle between 48% and 52%.
NOTE 14. Both PLL and output dividers are in Integer Mode. Characterized with 8T49N1012-900.
NOTE 15. Tested with all outputs operating at 122.88MHz.
NOTE 16. This parameter is guaranteed by design.
NOTE 17. Assuming a clear I^2C bus.

Table 12B. HCSL AC Characteristics, V_{CCX}[1] = 3.3V ±5% or 2.5V ±5%, V_{CCOx}[2] = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to 85°C[3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{RB}	Ring-back Voltage Margin[4, 5]		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed[4, 5]		500			ps
V_{MAX}	Absolute Max. Output Voltage[6, 7]				1150	mV
V_{MIN}	Absolute Min. Output Voltage[6, 8]		-300			mV
V_{CROSS}	Absolute Crossing Voltage[9, 10]		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges[9, 11]				140	mV

NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE 2. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.
NOTE 3. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 4. Measurement taken from differential waveform.
NOTE 5. T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 6. Measurement taken from single-ended waveform.
NOTE 7. Defined as the maximum instantaneous voltage including overshoot.
NOTE 8. Defined as the minimum instantaneous voltage including undershoot.
NOTE 9. Measured at crossing point where the instantaneous voltage value of the rising edge of Qn equals the falling edge of nQn.
NOTE 10. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 11. Defined as the total variation of all crossing voltages of rising Qn and falling nQn. This is the maximum allowed variance in V_{CROSS} for any particular system.

Table 13. Typical RMS Phase Jitter, V_{CCX}[1] = 3.3V ±5% or 2.5V ±5%, V_{CCOx}[2] = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[3]

Symbol	Parameter		Test Conditions	LVPECL	LVDS	HCSL	LVCMOS[4]	Units
tjit(ϕ)	RMS Phase Jitter[5] (Random) Integration Range: 12kHz - 20MHz	Q[0:7] Integer	f_{OUT} = 122.88MHz[6]	219	218	216	238	fs
			f_{OUT} = 156.25MHz[7]	223	220	223	220	fs
			f_{OUT} = 622.08MHz[8]	183	190	199	N/A[9]	fs
		Q[8:11]	f_{OUT} = 122.88MHz[6]	251	251	240	263	fs
		Q[0:7] Fractional	f_{OUT} = 122.88MHz[10]	295	296	294	307	fs

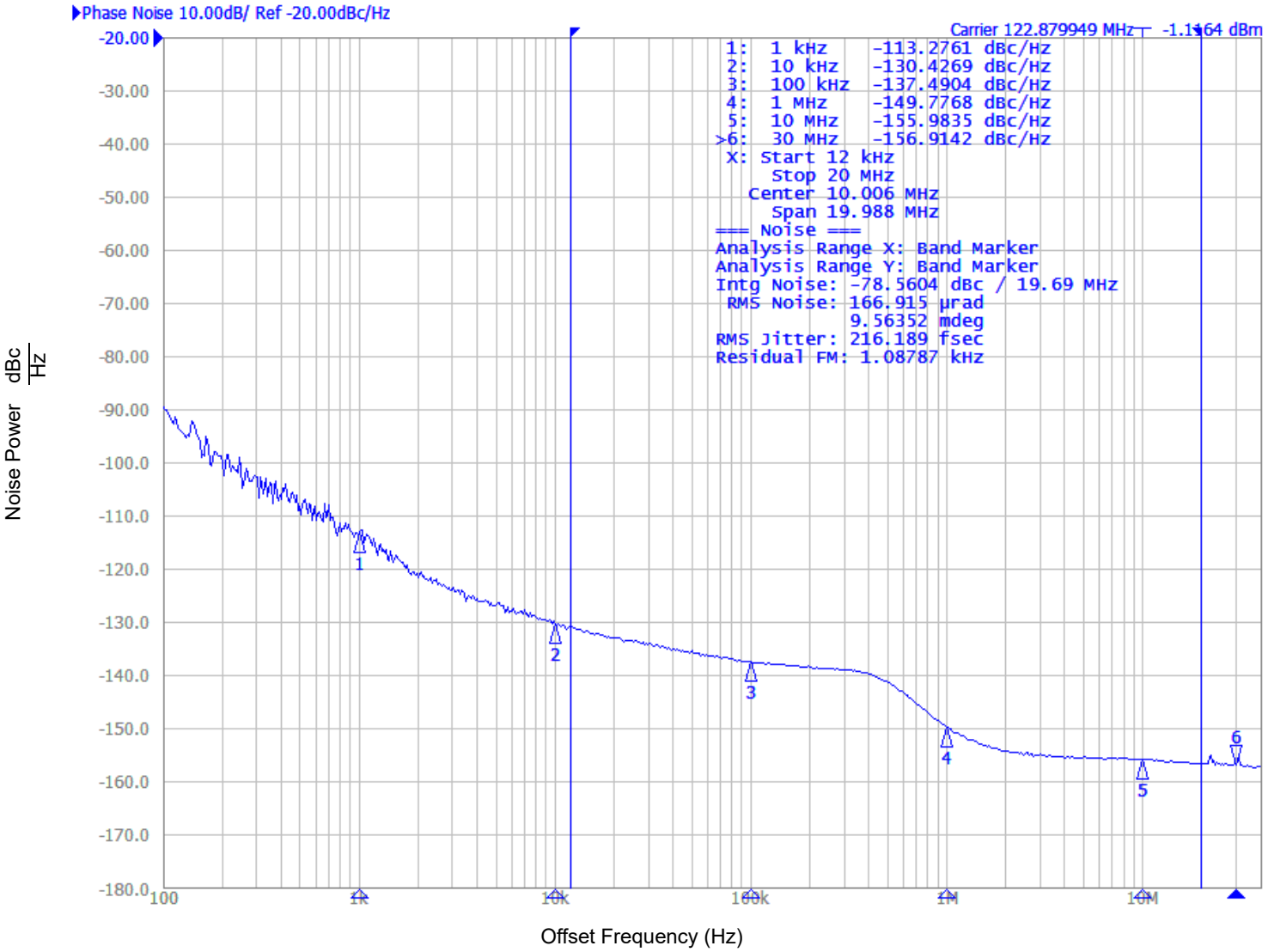
NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE 2. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.
NOTE 3. All outputs configured for the specific output type, as shown in the table.
NOTE 4. Qx and nQx are 180° out of phase.
NOTE 5. It is recommended to use IDT's *Timing Commander software* to program the device for optimal jitter performance.
NOTE 6. Characterized with 8T49N1012-900.
NOTE 7. Characterized with 8T49N1012-901.
NOTE 8. Characterized with 8T49N1012-902.
NOTE 9. This frequency is not supported for LVCMOS operation.
NOTE 10. Characterized with 8T49N1012-903.

Table 14. PCI Express Jitter Specifications, V_{CCX}[1] = 3.3V ±5% or 2.5V ±5%, V_{CCOx}[2] = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to 85°C[3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
tj (PCIe Gen 1)	Phase Jitter Peak-to-Peak[4, 5, 6]	ƒ = 100MHz, 40MHz Crystal Input, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		6	18	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS[5, 6, 7]	ƒ = 100MHz, 40MHz Crystal Input, High Band: 1.5MHz - Nyquist (clock frequency/2)		0.5	1.8	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS[5, 6, 7]	ƒ = 100MHz, 40MHz Crystal Input, Low Band: 10kHz - 1.5MHz		0.1	0.5	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS[5, 6, 8]	ƒ = 100MHz, 40MHz Crystal Input, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.1	0.2	0.8	ps

NOTE 1. V_{CCX} denotes: V_{CCD}, V_{CC}, V_{CCCS}.
NOTE 2. V_{CCOx} denotes: V_{CCO0} through V_{CCO8}, V_{CCO10}.
NOTE 3. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 4. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen1.
NOTE 5. This parameter is guaranteed by characterization. Not tested in production.
NOTE 6. Outputs configured for HSCL mode using integer output dividers. Fox 277LF-40-22 (40MHz, 12pF) crystal used with doubler logic enabled.
NOTE 7. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 8. RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification Revision 0.7, October 2009 and is subject to change pending the final release version of the specification.

Typical Phase Noise at 122.88MHz (3.3V)



Applications Information

Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 5A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 5B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSCI input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. If the duty cycle of the input reference is not 50% then increased phase noise may result. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

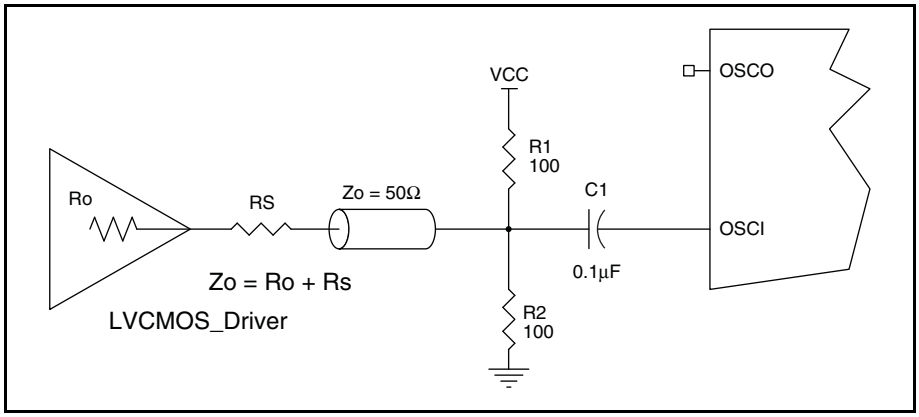


Figure 5A. General Diagram for LVCMOS Driver to XTAL Input Interface

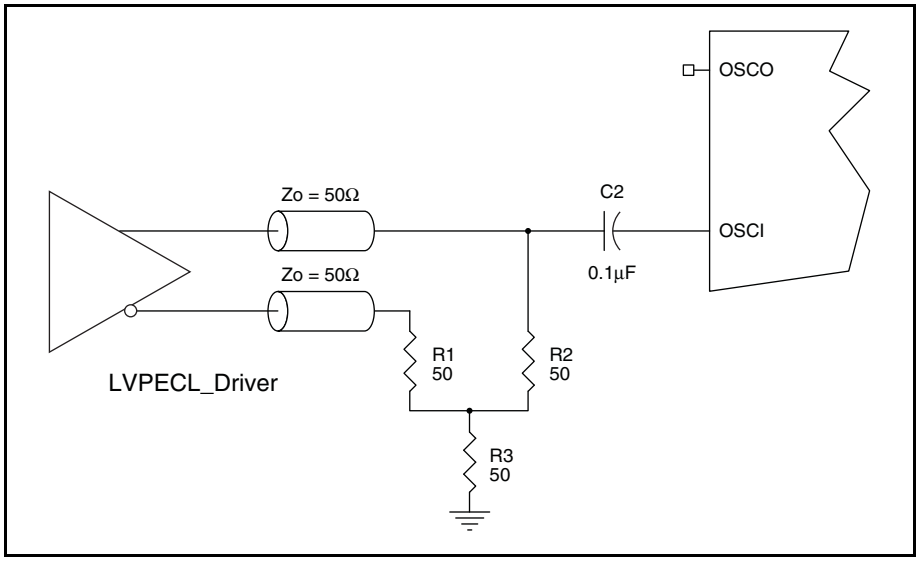


Figure 5B. General Diagram for LVPECL Driver to XTAL Input Interface

Wiring the Differential Input to Accept Single-Ended Levels

Figure 6 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CCD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CCD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. Similarly, if the input clock swing is 1.8V and V_{CCD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 0.9V. It is recommended to always use R1 and R2 to provide a known V_1 voltage. The values below are for when both the single ended swing and V_{CCD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CCD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

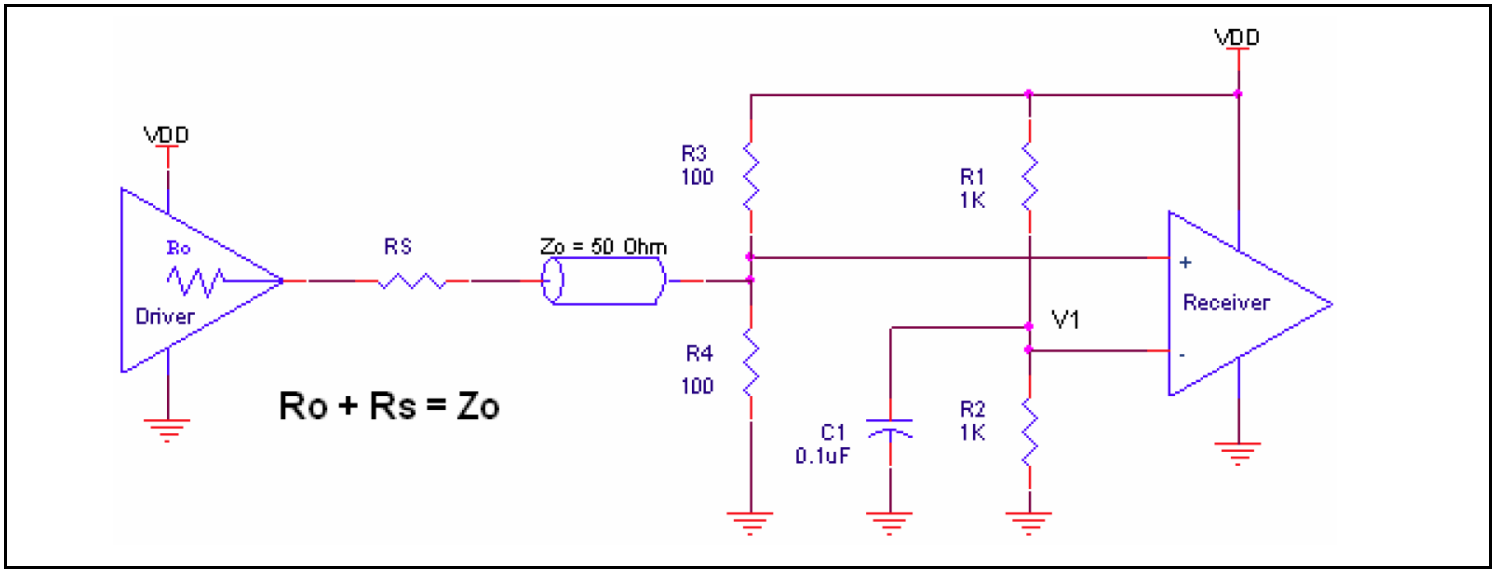


Figure 6. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 7A* to *Figure 7E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 7A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

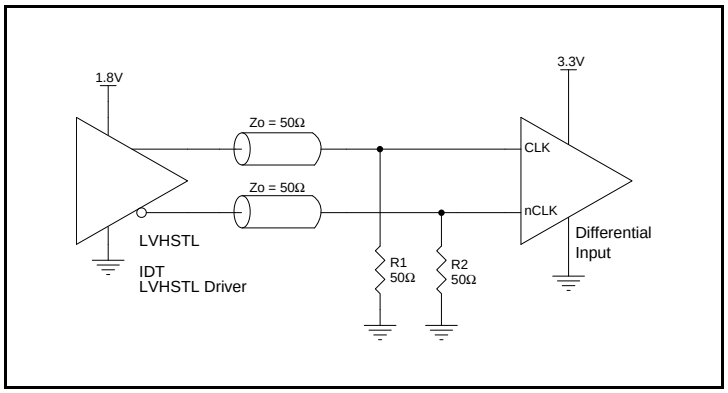


Figure 7A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

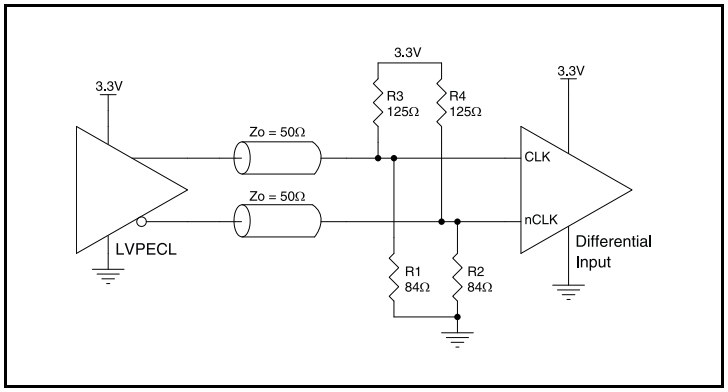


Figure 7B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

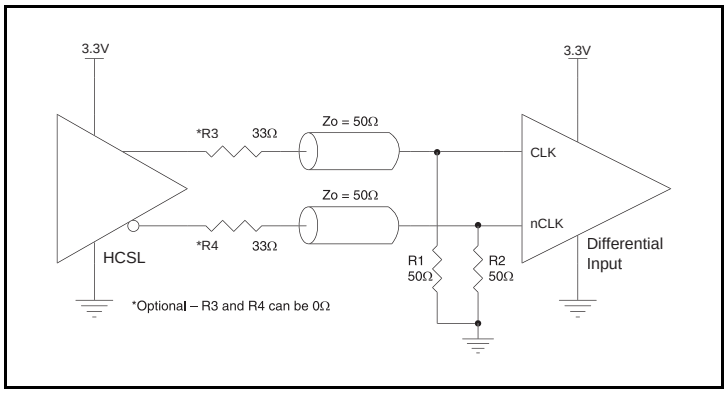


Figure 7C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

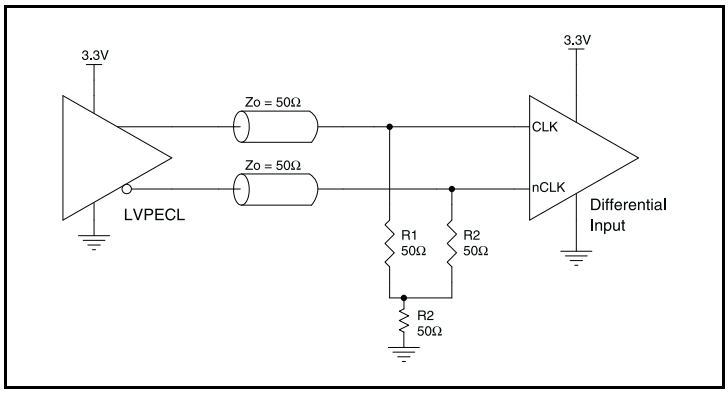


Figure 7D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

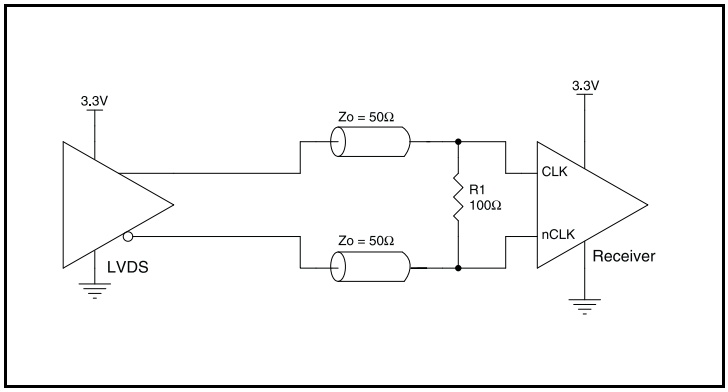


Figure 7E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL, LVHSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 8A* to *Figure 8D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 8A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

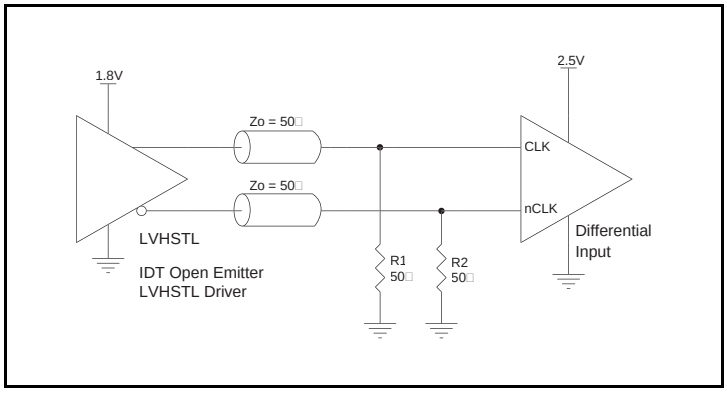


Figure 8A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

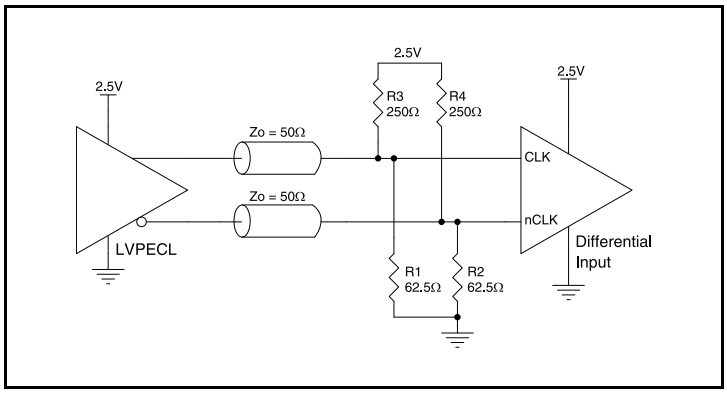


Figure 8C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

Figure 8B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

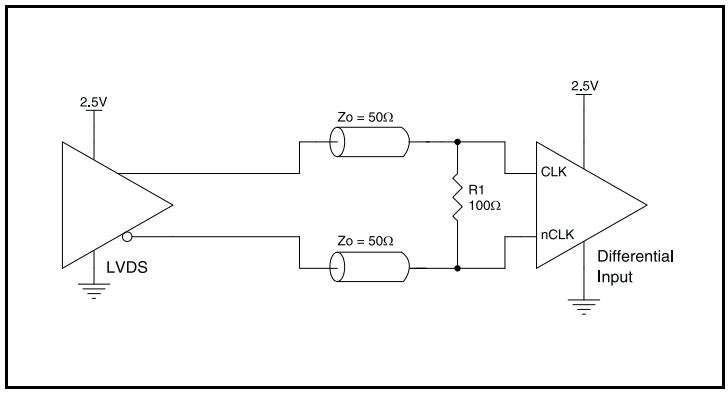


Figure 8D. CLK/nCLK Input Driven by a 2.5V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use the reference clock inputs, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground. It is recommended that CLK, nCLK not be driven with active signals when not enabled for use by the PLL.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both OSCI and OSCO can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from OSCI to ground.

LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

Unused differential outputs should be programmed to high-impedance.

LVCMOS Outputs

If only one output from an output pair (such as Q0 is used and nQ0 remains unused) is intended for use, it is then recommended to program the unused output to inverted mode and terminate both outputs properly. If both outputs (Qx and nQx) are unused, it is recommended to program the output buffers to high-impedance.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 9A* can be used with either type of output structure. *Figure 9B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

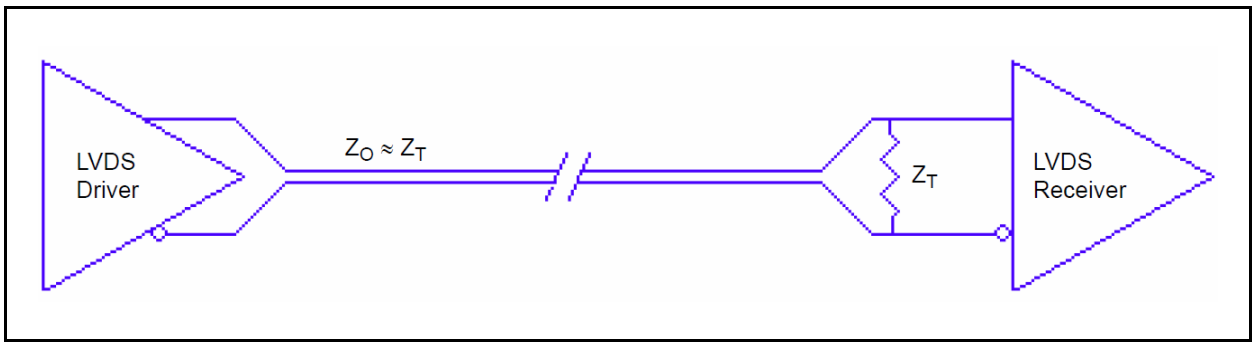


Figure 9A.Standard LVDS Termination

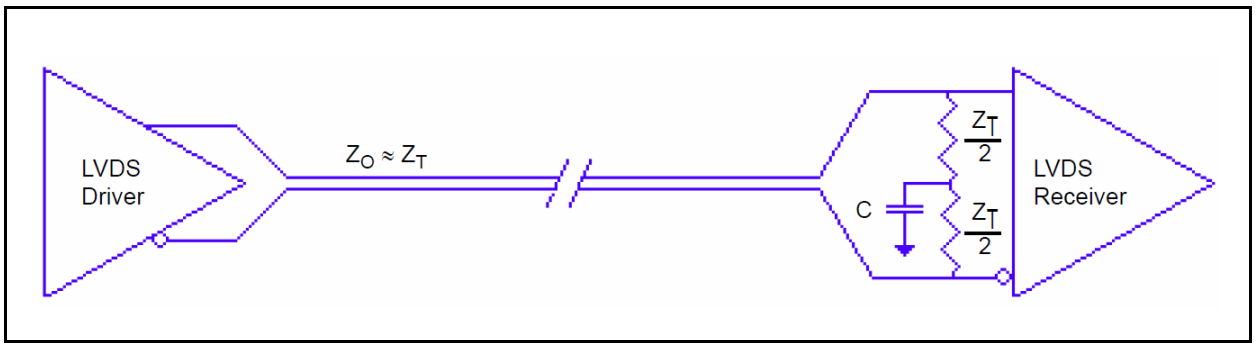


Figure 9B. Optional LVDS Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 10A* and *Figure 10B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

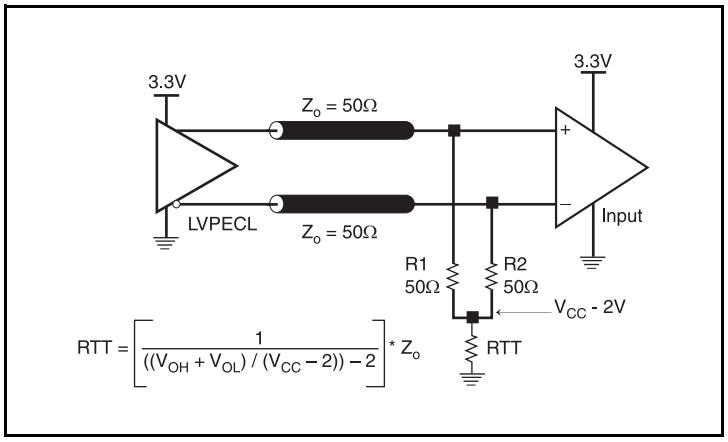


Figure 10A. 3.3V LVPECL Output Termination

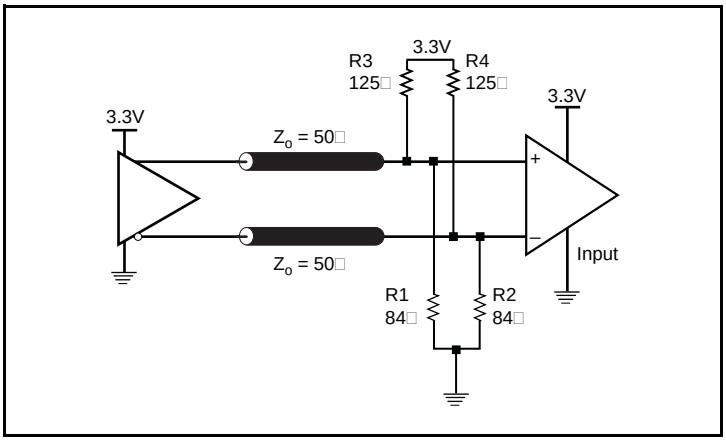


Figure 10B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 11A and *Figure 11C* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in *Figure 11C* can be eliminated and the termination is shown in *Figure 11B.*

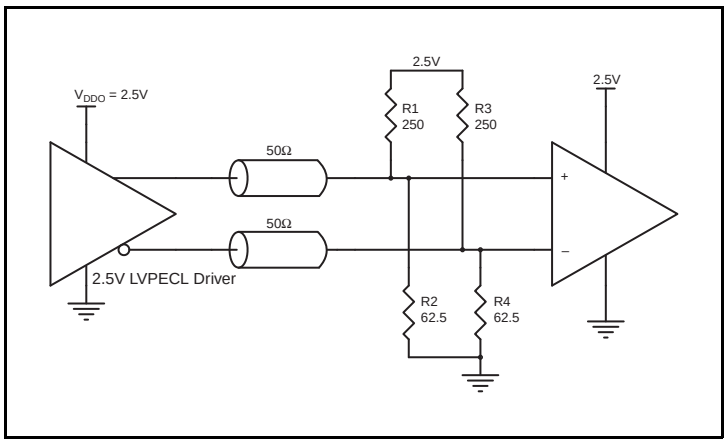


Figure 11A. 2.5V LVPECL Driver Termination Example

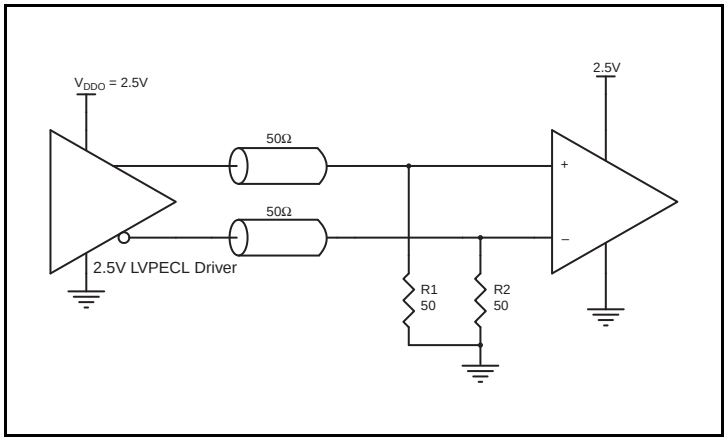


Figure 11C. 2.5V LVPECL Driver Termination Example

Figure 11B. 2.5V LVPECL Driver Termination Example

2.5V and 3.3V HCSL Output Termination

Figure 12A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

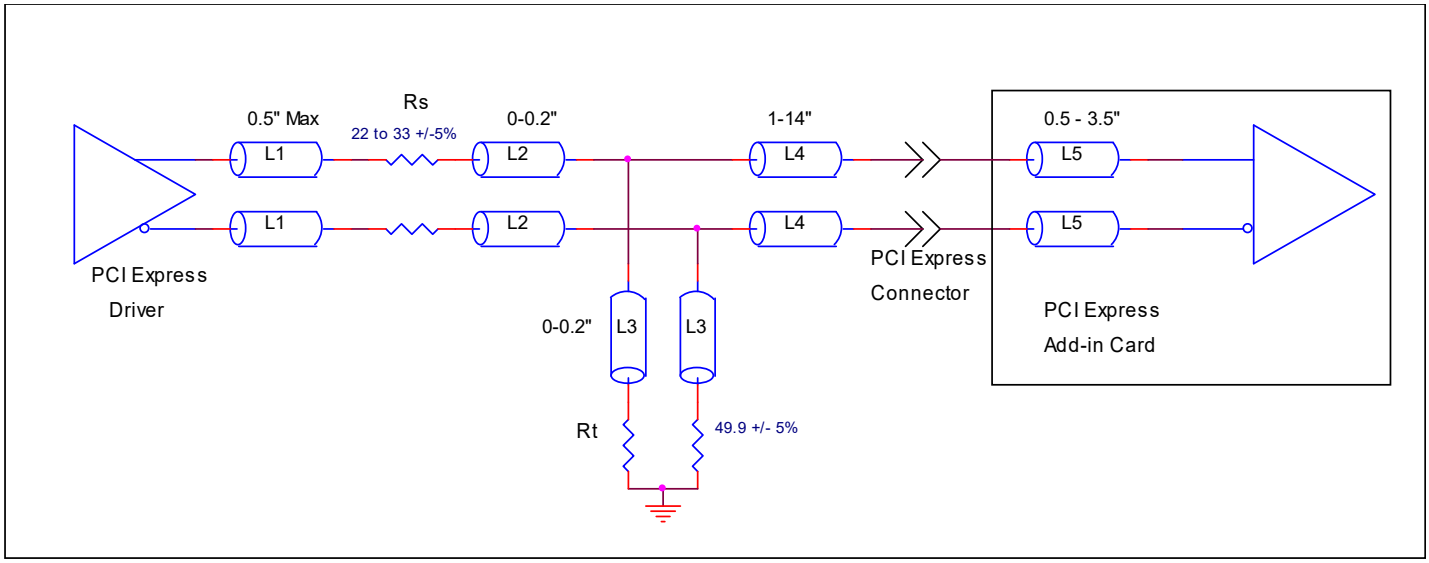


Figure 12A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 12B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

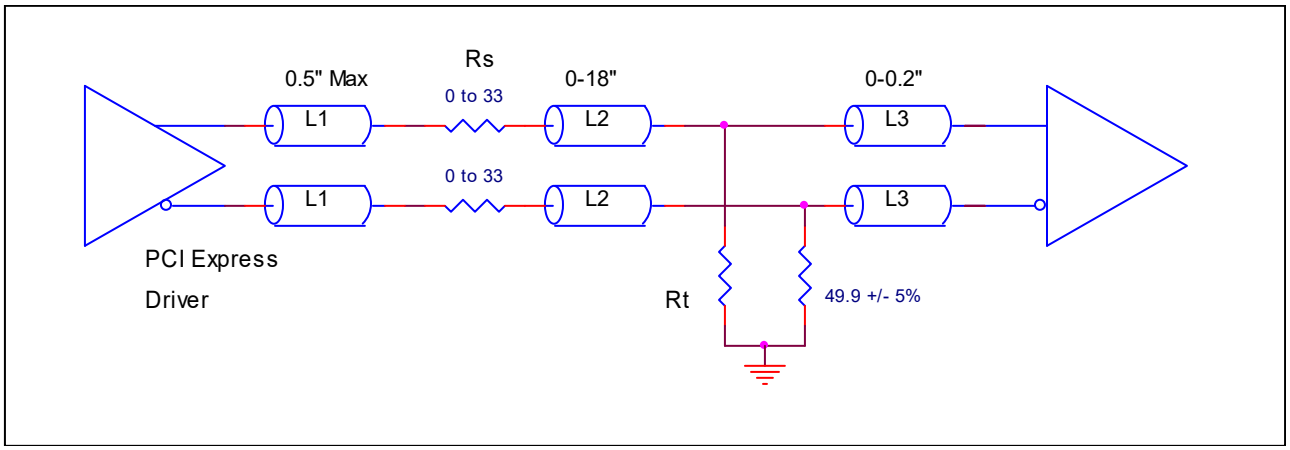


Figure 12B. Recommended Termination (where a point-to-point connection can be used)

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 13.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

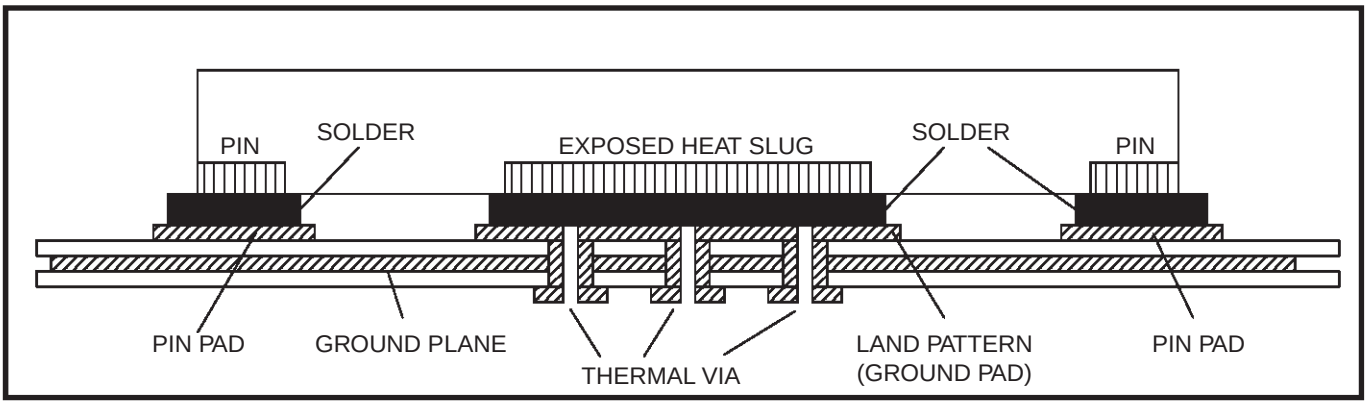


Figure 13. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic and Layout Information

Schematics for 8T49N1012 can be found on IDT.com. Please search for the 8T49N1012 device and click on the link for evaluation board schematics.

Crystal Recommendation

This device was characterized using FOX 277LF series through-hole crystals including part #277LF-40-18 (40MHz) and 277LF-38.88-2 (38.88MHz). If a surface mount crystal is desired, we recommend FOX Part #603-40-48 (40MHz) or FOX Part #603-38.88-7 (38.88MHz).

I^2C Serial EEPROM Recommendation

The 8T49N1012 was designed to operate with most standard I^2C serial EEPROMs of 256 bytes or larger. Atmel AT24C04C was used during device characterization and is recommended for use. Please contact IDT for review of any other I^2C EEPROM’s compatibility with the 8T49N1012.

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

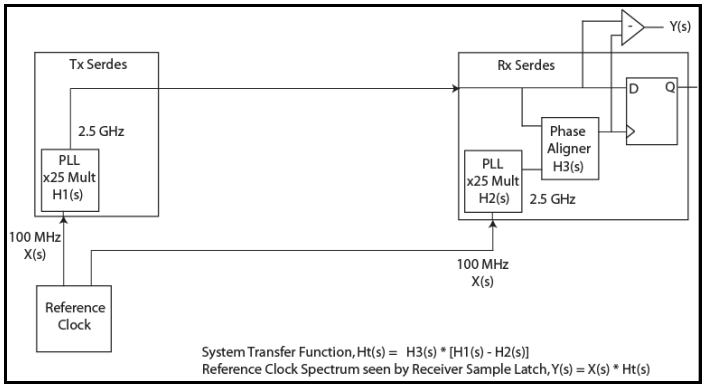
In the jitter analysis, the transmit (Tx) and receive (Rx) SerDes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

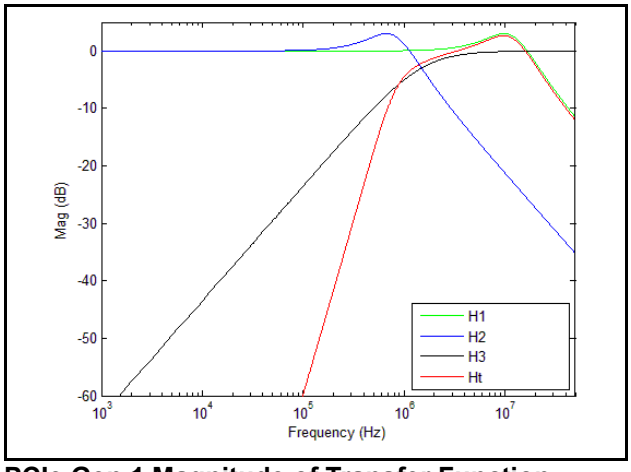
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



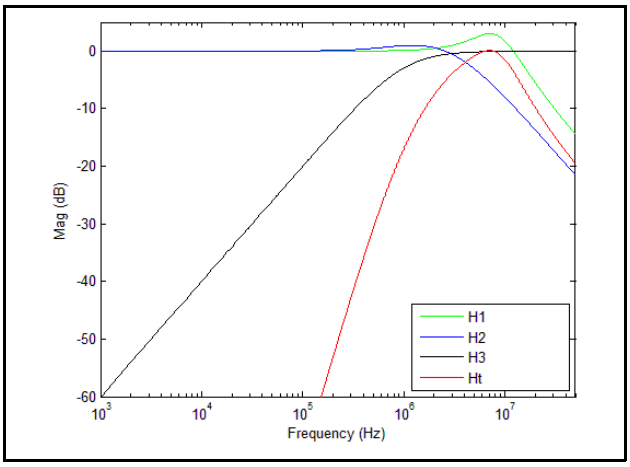
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

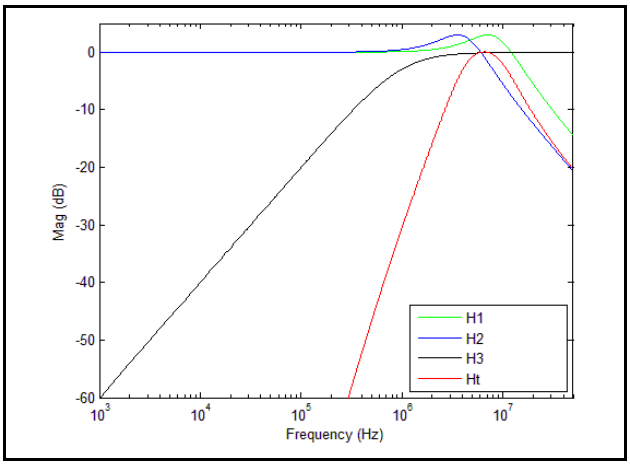


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

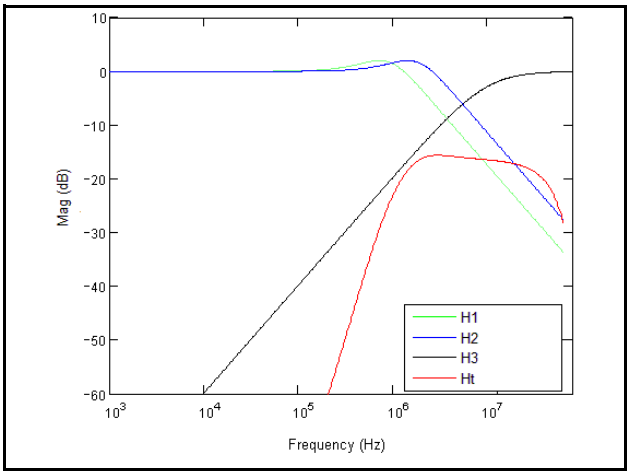


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note, *PCI Express Application Note*.

Power Dissipation and Thermal Considerations

The 8T49N1012 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

The 8T49N1012 device was designed and characterized to operate within the ambient industrial temperature range of -40°C to +85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

Power Domains

The 8T49N1012 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). *Figure 14* below indicates the individual domains and the associated power pins.

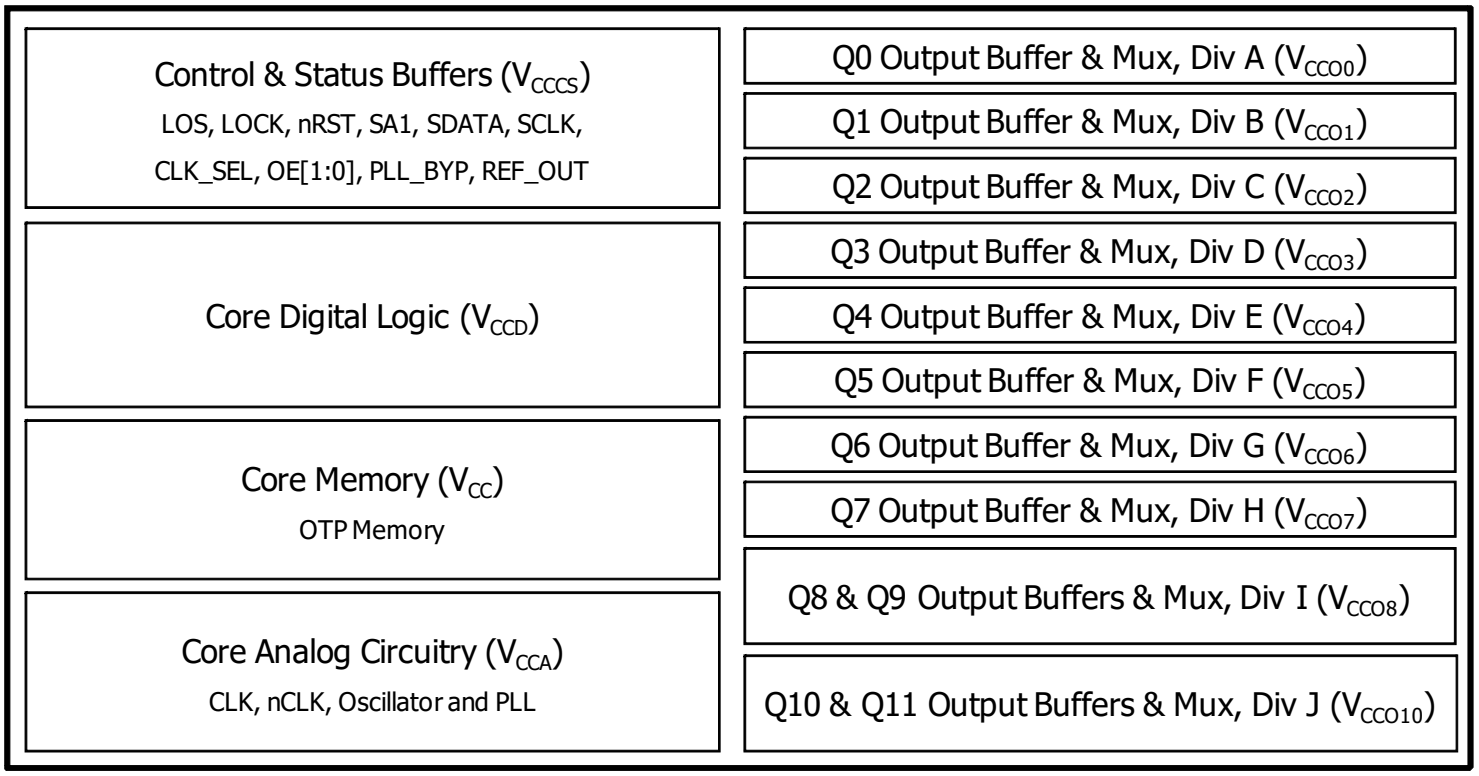


Figure 14. 8T49N1012 Power Domains

For the output paths shown above, there are many different structures that are used. Power consumption data will vary slightly depending on the structure used as shown in the Output Current Calculation tables on the following pages.

Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core and analog voltage supplies from *Table 8A* through *Table 8B*.
2. Determine the nominal power consumption of each enabled output path.
   a. This consists of a base amount of power that is independent of operating frequency, as shown in *Table 16A* through *Table 16G* (depending on the chosen output protocol).
   b. Then there is a variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in *Table 16A* through *Table 16G*.
3. All of the above totals are then summed.

Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heatsink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in *Table 15* below. Please contact IDT for assistance in calculating results under other scenarios.

Table 15. Thermal Resistance θ_{JA} for 72-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	16.1°C/W	12.4°C/W	11.1°C/W

Current Consumption Data and Equations

Table 16A. 3.3V LVPECL/HCSL Output Current Calculation Table

LVPECL/HCSL	FQ_Factor (µA/MHz)	Base_Current (mA)
Q[0:7][1]	15.0	43.2
Q[8:9], Q[10:11][2]	16.4	34.7

NOTE 1. The values are per channel (one divider and an output pair.

NOTE 2. The values are based on a divider and two output pairs.

Table 16B. 3.3V LVDS Output Current Calculation Table

LVDS	FQ_Factor (µA/MHz)	Base_Current (mA)
Q[0:7][1]	15.0	52.6
Q[8:9]], Q[10:11][2]	16.4	52.5

NOTE 1. The values are per channel (one divider and an output pair.

NOTE 2. The values are based on a divider and two output pairs.

Table 16C. 3.3V LVCMOS Output Current Calculation Table

LVCMOS	Base_Current (mA)
Q[0:7][1]	41.2
Q[8:9], Q[10:11][2]	30.5

NOTE 1. The values are per channel (one divider and two LVCMOS outputs).

NOTE 2. The values are based on a divider and four LVCMOS outputs.

Table 16D. 2.5V LVPECL/HCSL Output Current Calculation Table

LVPECL/HCSL	FQ_Factor (µA/MHz)	Base_Current (mA)
Q[0:7][1]	12.0	41.9
Q[8:9], Q[10:11][2]	11.5	32.0

NOTE 1. The values are per channel (one divider and an output pair.

NOTE 2. The values are based on a divider and two output pairs.

Table 16E. 2.5V LVDS Output Current Calculation Table

LVDS	FQ_Factor (µA/MHz)	Base_Current (mA)
Q[0:7][1]	12.0	50.6
Q[8:9], Q[10:11][2]	11.5	48.9

NOTE 1. The values are per channel (one divider and an output pair.

NOTE 2. The values are based on a divider and two output pairs.

Table 16F. 2.5V LVCMOS Output Current Calculation Table

LVCMOS	Base_Current (mA)
Q[0:7][1]	40.2
Q[8:9], Q[10:11][2]	28.7

NOTE 1. The values are per channel (one divider and two LVCMOS outputs).

NOTE 2. The values are based on a divider and four LVCMOS outputs

Table 16G. 1.8V LVCMOS Output Current Calculation Table

LVCMOS	Base_Current (mA)
Q[0:7][1]	39.7
Q[8:9], Q[10:11][2]	27.5

NOTE 1. The values are per channel (one divider and two LVCMOS outputs).

NOTE 2. The values are based on a divider and four LVCMOS outputs

Applying the values to the following equation will yield output current by frequency:

Qx Current = FQ_Factor * Frequency + Base_Current

where:

Qx Current is the specific output current according to output type and frequency

FQ_Factor is used for calculating current increase due to output frequency

Base_Current is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$T_J = T_A + (\theta_{JA} * Pd_{total})$

where:

T_J is the junction temperature (°C)

T_A is the ambient temperature (°C)

θ_{JA} is the thermal resistance value from *Table 15*, dependent on ambient airflow (°C/W)

Pd_{total} is the total power dissipation of the 8T49N1012 under usage conditions, including power dissipated due to loading (W).

Note that the power dissipation per output pair due to loading is assumed to be 27.95mW for LVPECL outputs and 44.5mW for HCSL outputs. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using C_{PD} (found in *Table 2*) and output frequency:

$Pd_{OUT} = C_{PD} * F_{OUT} * V_{CCO}^2$

where:

Pd_{OUT} is the power dissipation of the output (W)

C_{PD} is the power dissipation capacitance (F)

F_{OUT} is the output frequency of the selected output (Hz)

V_{CCO} is the voltage supplied to the appropriate output (V)

Example Calculations

Example 1. PLL is running in Integer mode and REF_OUT Off (3.3V Core Voltage)

Output	Output Type	Frequency (MHz)	V_{CCO}
Q0	LVCMOS	25	1.8
Q1	LVCMOS	125	3.3
Q2	LVPECL	25	3.3
Q3	HCSL	100	3.3
Q4	LVPECL	100	3.3
Q5	LVPECL	100	3.3
Q6	LVCMOS	100	2.5
Q7	LVDS	100	3.3
Q8	LVPECL	100	3.3
Q9	LVPECL	100	3.3
Q10	LVDS	150	2.5
Q11	LVDS	150	2.5

Core Power Dissipation:

- Core Supply Current, I_{CC} = **28mA (V_{CCD} = V_{CC} = V_{CCCS} = 3.3V)**
- Analog Supply Current, I_{CCA} = **170mA (V_{CCA} = 3.3V)**
- Total Core and Analog Power = 3.465V * (28 + 170)mA = **686.1mW**

Output Power Dissipation:

Q0 Current = 15pF * 25MHz * 1.89V + 39.7mA = 40.4mA

Q1 Current = 17pF * 125MHz * 3.465V + 41.2mA = 48.6mA

Q2 Current = 15µA/MHz * 25MHz + 43.2mA = 43.6mA

Q3 Current = 15µA/MHz * 100MHz + 43.2mA = 44.7mA

Q4 Current = 15µA/MHz * 100MHz + 43.2mA = 44.7mA

Q5 Current = 15µA/MHz * 100MHz + 43.2mA = 44.7mA

Q6 Current = 15pF * 100MHz * 2.5V + 40.2mA = 44mA

Q7 Current = 15µA/MHz * 100MHz + 52.6mA = 54.1mA

Q[8:9] Current = 16.4µA/MHz * 100MHz + 34.7mA = 36.3mA

Q[10:11] Current = 11.5µA/MHz * 150MHz + 48.9mA = 50.6mA

- Output Current @ 1.8V = **40.4mA**
- Output Current @ 2.5V = 44mA + 50.6mA = **94.6mA**
- Output Current @ 3.3V = 48.6mA + 43.6mA + 44.7mA + 44.7mA + 44.7mA + 54.1mA + 36.3mA = **316.7mA**
- Power dissipated due to switching:

  LVPECL Outputs = 5 * 27.95mW = **139.8mW**

  HCSL Output = 1 * 44.5mW = **44.5mW**

  Total Output Power = (1.89V * 40.4mA) + (2.625V * 94.6mA) + (3.465V * 316.7mA) + 139.8mW + 44.5mW = **1606.35mW**

Total Power Dissipation:

- Total Power = 686.1mW + 1606.35mW = **2292.4mW**

Junction Temperature Calculation:

With an ambient temperature of 85°C and no airflow, the junction temperature is:

T_J = 85°C + 16.1°C/W * 2.2924W = **121.9°C** (which is below the maximum allowable temperature)

Due to the 8T49N1012 flexibility and highly configurable outputs, the power dissipation will vary depending on the specific device configuration. The power calculations example shown above illustrates a single configuration and its corresponding power figures. If additional support on calculating power consumption for other configurations is needed, please contact IDT (clocks@idt.com).

Reliability Information

Table 17. θ_{JA} vs. Air Flow Table for a 72-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	16.1°C/W	12.4°C/W	11.1°C/W

NOTE: Theta JA (θ_{JA})values calculated using a 4-layer JEDEC PCB (114.3mm x 101.6mm), with 2oz. (70um) copper plating on all 4 layers.

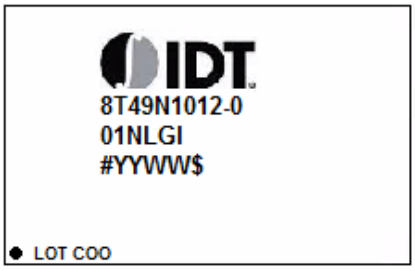
Transistor Count

The transistor count for 8T49N1012 is: 579,607

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Marking Diagram



1. Lines 1 and 2 indicate the part number.
2. “Line 3 indicates the following:
   - #” denotes sequential lot number.
   - “YYWW” is the last two digits of the year and week that the part was assembled.
   - “$” denotes the mark code.

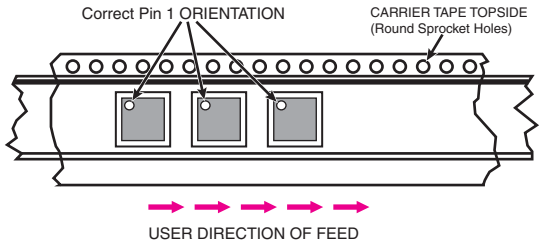
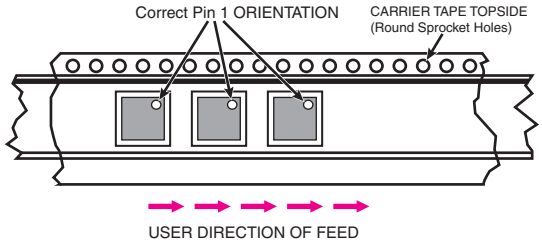
Ordering Information

Table 18. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N1012-dddNLGI	IDT8T49N1012-dddNLGI	72-Lead VFQFN, Lead-Free	Tray	-40°C to +85°C
8T49N1012-dddNLGI8	IDT8T49N1012-dddNLGI	72-Lead VFQFN, Lead-Free	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40°C to +85°C
8T49N1012-dddNLGI#	IDT8T49N1012-dddNLGI	72-Lead VFQFN, Lead-Free	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40°C to +85°C

NOTE: For the specific, publicly available -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document. For custom -ddd order codes, please contact IDT for more information.

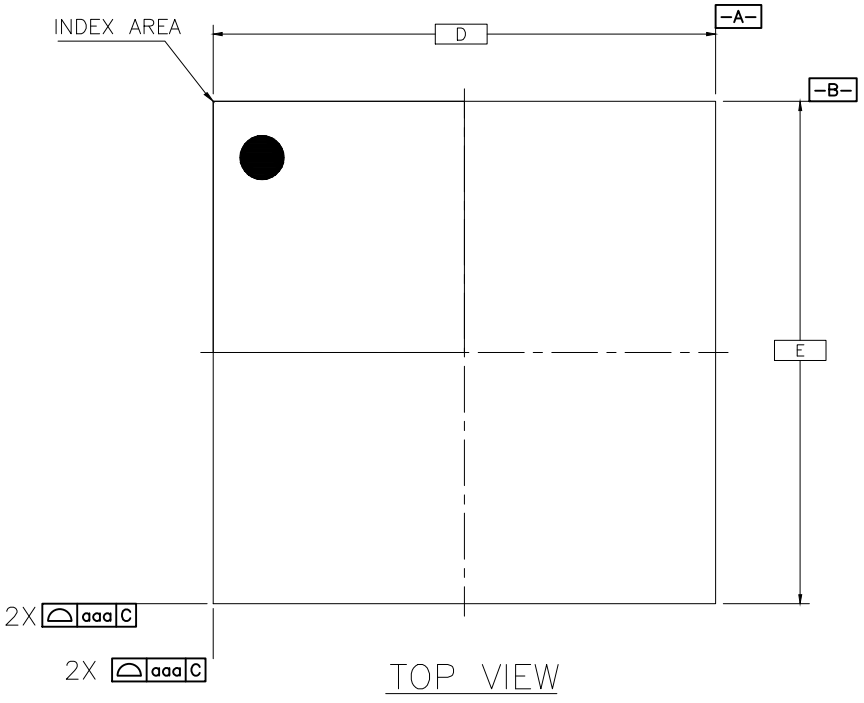
Table 19. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
NLGI8	Quadrant 1 (EIA-481-C)	
NLGI#	Quadrant 2 (EIA-481-D)	

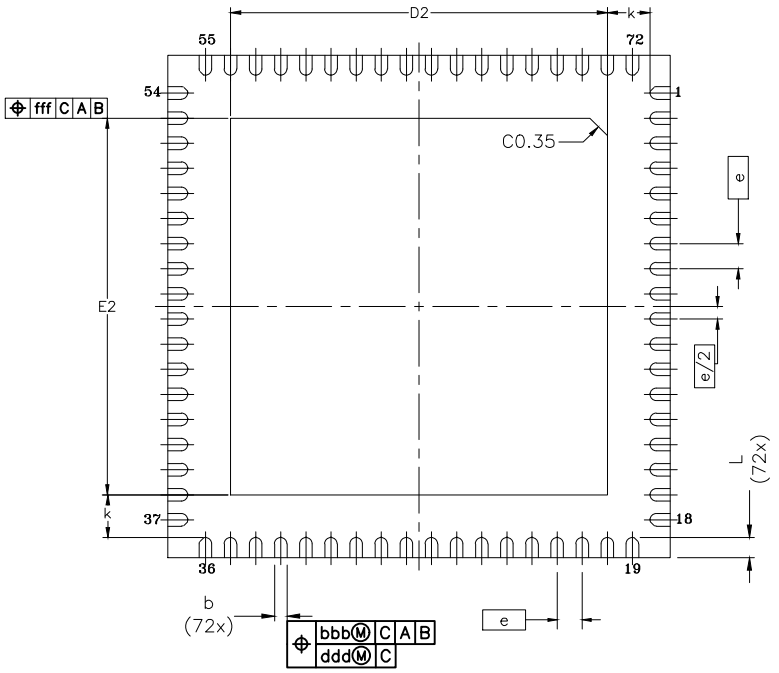
Revision History

Date	Description of Change
January 27, 2019	Corrected the I^2C read sequence diagrams in Figure 3 and Figure 4 to match I^2C specification and device actual performance. Note: Only the drawing was incorrect – the part's behavior did not change and continues to meet the I^2C specification. Added a Marking Diagram
January 31, 2018	Updated I2C Mode Operation to indicate support for v2.1 of the I2C specification.
October 28, 2016	Crystal Recommendation - deleted IDT crystal reference.

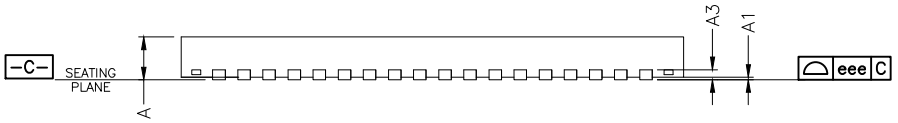
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE.	2/2/16	JH



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)

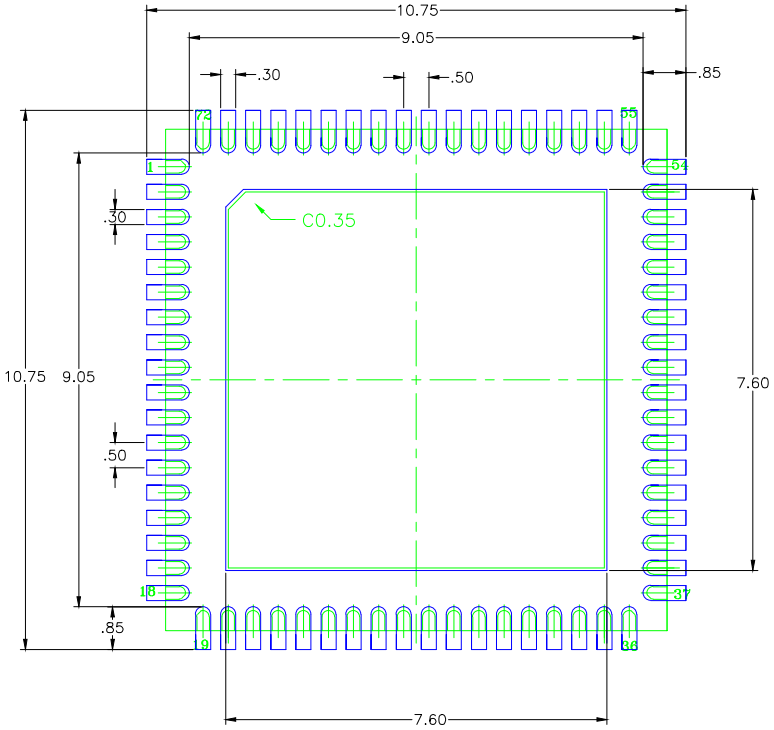
TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± XX± XXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE	NL/NLG72 PACKAGE OUTLINE 10.0 x 10.0 mm BODY, EPAD 7.5mm SQ. 0.50 mm Pitch QFN (SAWN)
DRAWN RAC	2/2/16		
CHECKED			
		SIZE: C	DRAWING No.: PSC-4208-02 / REV: 00
		DO NOT SCALE DRAWING	SHEET 1 OF 3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE.	2/12/16	JH

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
D2	7.40	7.50	7.60
E2	7.40	7.50	7.60
A2	0.00	0.65	1.00
L	0.30	0.40	0.50
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20 ref.		
b	0.18	0.25	0.30
e	0.50 BSC		
D	10.00 BSC		
E	10.00 BSC		
k	0.85 ref.		
TOLERANCES			
aaa	0.15		
bbb	0.10		
ccc	0.05		
eee	0.8		
fff	0.10		

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± XX± XXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE NL/NLG72 PACKAGE OUTLINE 10.0 x 10.0 mm BODY, EPAD 7.5mm SQ. 0.50 mm Pitch QFN (SAWN)	
DRAWN RAC	2/2/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4208-02 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE.	2/2/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± XX± XXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE	NL/NLG72 PACKAGE OUTLINE 10.0 x 10.0 mm BODY, EPAD 7.5mm SQ. 0.50 mm Pitch QFN (SAWN)
DRAWN PAC	2/2/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4208-02 REV 00
		DO NOT SCALE DRAWING	SHEET 3 OF 3

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.