GX39221

2 × 96Gbaud Linear TIA

The GX39221 is a dual channel 96Gbaud linear Trans-Impedance Amplifier (TIA) for 800G and beyond Integrated Coherent Receivers (ICRs).

The GX39221 integrates two TIA signal paths for “I” and “Q” channels. The high-performance, low power, and compact design of the GX39221 also enables a small-form factor integrated optical module such as CFP2 and CFP4.

Features

- Dual-channel integrated 96Gbaud linear TIA with analog control interface
- Differential linear gain: 70–3,250Ω and > 30dB dynamic range
- > 60GHz adjustable 3dB bandwidth
- Automatic and manual gain control, Output Voltage Control, Peak Detection and Shutdown functionalities
- Low THD, low crosstalk, and low power consumption for covering 64QAM receiver

Applications

- 800G and beyond coherent systems with 96Gbaud higher-order QAM modulation format
- Integrated optical modules for CFP/CFP2/CFP4 form factors

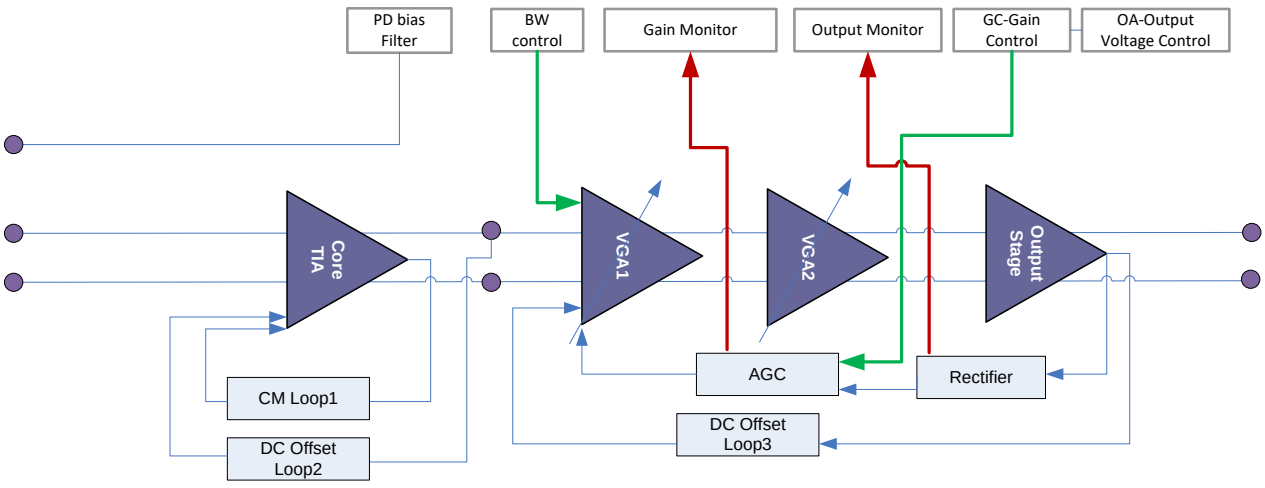

Figure 1. Block Diagram

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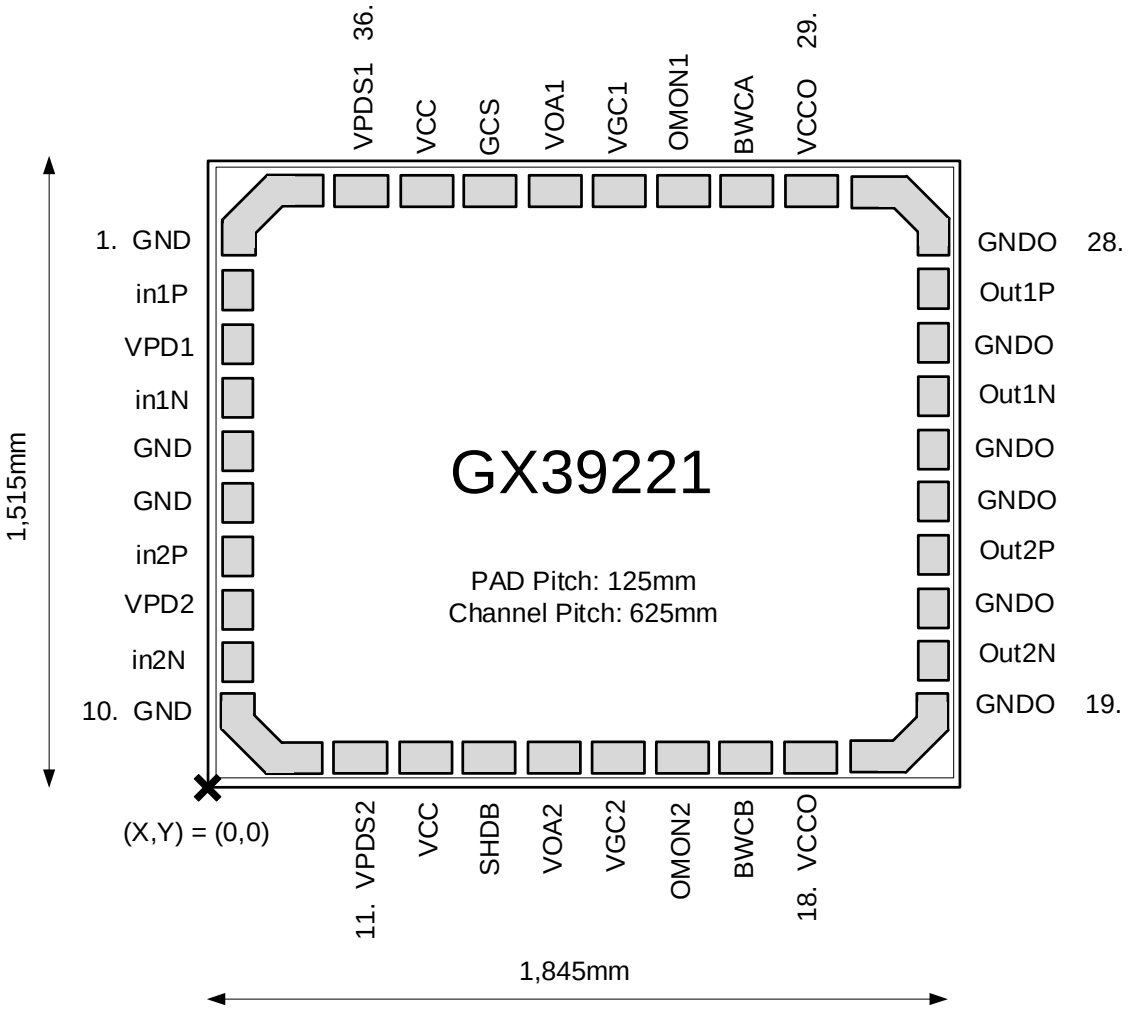
1. Pad Information

1.1 Pad Assignments



1. Thickness of Die: 100µm ±15µm.
2. Bond Pad metallization is aluminum (4µm thick). Passivation on the die is 4.3µm thick.
3. Chip size 1845 ±30µm × 1515 ±30µm including scribe line and saw cut loss.
4. RF input and output pad open area: 70µm × 90µm.
5. DC pad open area: 120µm × 70µm.
6. RF input and output pads have a pitch of 250µm (P to N).
7. DC pads have a pitch of 155µm.

1.2 Pad Descriptions

1.2.1. Data Path Signals

Pad Name	Type	Description
INxP, INxN	Analog Input	The Photodetector input is an analog input that is connected to the anode (p-side) of the photodetector. The cathode of the detector must be connected to a positive power supply. Balanced photodiode configuration will have a PD connected to each input (INP, INN). In case of single photodiode configuration, the PD has to be connected to the INP pad.
OUTxP, OUTxN	Differential Data Output	The Data Output is a high-speed differential output, where P is the positive (non-inverted) node and N is the negative (inverted) node.

1.2.2. Management Interface Signals

Pad Name	Type	Description
OMONx	Analog Output	The output of the Peak Detection pin will provide a measurement in voltage of the average absolute value of the peak-to-peak output swing.
GCS	Analog Input	Selects AGC or Manual Gain Control. Automatic Gain Control (AGC) Mode is set when GCS = High; Manual Gain Control (MGC) Mode is set when GCS = Low. The default mode of the channel is AGC, when the GCS is left floating.
VGCx	Analog Input/Output	Voltage applied to the VGC pad (in MGC mode) results in variation of the differential gain of the channel. Higher the VGC, higher the differential gain. VGC pad works as gain monitor in AGC mode. External capacitance on this pin controls AGC loop bandwidth (in AGC mode).
BWCA/B	Analog Input	Digital selection of bandwidth control, BWCA pin works along with BWCB pin. Three level decoders are implemented on the BWCA and BWCB inputs which produce the following codes: BWCA,B Low level = 0V – 0.9V : BW = 8. BWCA,B Mid. Level = 1.1V – 1.8V (Floating = 1.5V) : BW = 16. BWCA,B High Level = 2V – 3.3V : BW = 31. In total, 9 possible peaking settings are provided with the combinations on BWCA and BWCB. The voltage level is 1.5V, when the BWCA,B pins are left floating. See Bandwidth Control truth table for control information.
VOAx	Analog Input	Voltage applied to the VOA pad (in AGC Mode) results in variation of output voltage swing. Higher the VOA, larger the swing. Detail analog input voltage level for each mode is described in the operating condition table.
SHDB	Analog Input	The Shutdown or squelch the output signal with turning off only the output stage. SHDB = High or FLT; Shutdown disable. The voltage level is pull up to V_{CC} when the terminal is floating. SHDB = Low; Shutdown enable. Detail analog input voltage level for each mode is described in the operating condition table.

1.2.3. Power and Ground Signals

Pad Name	Type	Description
VCC	Supply	Positive supply, 3.3V.
VCCO	Supply	Positive supply for output stage, 3.3V.
VPDx	Bias	Bias supply pads to the Cathode of the balanced photodiodes.
VPDSx	Supply	Positive supplies for the Cathode of the photodiodes with on-chip filtering circuits, 3.3V or 5.0V.
GND	GND	Ground.
GNDO	GND	Ground for output stage.

1. All pads (with the exception of INxP, INxN, OUTxP, and OUTxN) have ESD protection.
2. VCC and VCCO are not connected inside the die.
3. GND and GNDO are not connected inside the die.

1.2.4. Pad Descriptions

Pad #	Name	Type	Description
1	GND	Ground	Ground for input stage/large size pad.
2	In1P	RF	RF Input signal channel 1 P polarity.
3	VPD1	PD1 Bias	PD1 cathode bias pad.
4	In1N	RF	RF Input signal channel 1 N polarity.
5	GND	Ground	Ground for input stage.
6	GND	Ground	Ground for input stage.
7	In2P	RF	RF Input signal channel 2 P polarity.
8	VPD2	PD2 Bias	PD2 cathode bias pad.
9	In2N	RF	RF Input signal channel 1 N polarity.
10	GND	Ground	Ground for input stage/large size pad.
11	VPDS2	PD2 Bias Supply	PD2 Bias supply.
12	VCC	Power Supply	3.3V positive Bias supply.
13	SHDB	DC Digital Input	Channel 1 and 2 shutdown control.
14	VOA2	DC Input	Ch 2 output level adjustment input (in AGC mode).
15	VGC2	DC Input or Output	Ch 2 external gain control input (in MGC mode). Gain Monitor output (in AGC mode).
16	OMON2	DC Output	Ch 2 output monitor (peak detector) output.
17	BWCB	DC Digital Input	Digital selection of bandwidth control; works along with BWCA pin. See the Bandwidth Control truth table.
18	VCCO	Power Supply	3.3V positive Bias supply for the output stages.
19	GNDO	Ground	Ground for output stage/large size pad.

Pad #	Name	Type	Description
20	Out2N	RF	Ch 2 RF output, inverting.
21	GNDO	Ground	Ground for output stage.
22	Out2P	RF	Ch 2 RF output, non-inverting.
23	GNDO	Ground	Ground for output stage.
24	GNDO	Ground	Ground for output stage.
25	Out1N	RF	Ch 1 RF output, inverting.
26	GNDO	Ground	Ground for output stage.
27	Out1P	RF	Ch 1 RF output, non-inverting.
28	GNDO	Ground	Ground for output stage/large size pad.
29	VCCO	Power Supply	3.3V positive Bias supply for the output stage.
30	BWCA	DC Digital Input	Digital selection of bandwidth control; works along with BWCB pin. See Bandwidth Control truth table.
31	OMON1	DC Output	Ch 1 output monitor (peak detector) output
32	VGC1	DC Input or Output	Ch 1 external gain control input (in MGC mode). Gain Monitor output (in AGC mode).
33	VOA1	DC Input	Ch 1 output level adjustment input (in AGC mode).
34	GCS	DC Digital Input	Ch 1 and Ch 2 selects AGC/Manual Gain control.
35	VCC	Power Supply	3.3V positive Bias supply.
36	VPDS1	PD1 Bias Supply	PD2 Bias supply.

1. All GNDs to be downbonded first during assembly.
2. All VCCOs have to be bonded (not short on chip). VCCs are shorted on chip but recommended to be bonded.
3. In case of single photodiode configuration for each channel, the PDs have to be connected to IN1P and IN2P pads.

2. Specifications

2.1 Absolute Maximum Ratings

Exceeding the maximum ratings may cause damage to the product or lead to a reduction in reliability. These are solely stress ratings and functional operation of the device at these or any conditions beyond those indicated in recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage	VCC	-	-0.5	4.5	V
Supply Voltage	VCCob	-	-0.5	4.5	V
PD Supply Voltage	VPDSx	-	-0.5	7.0	V
DC Input Current (for each PD)	I_{DCIN}	-	-1.5	6	mA
RF Input Current (for each PD)	I_{RFIN}	-	-	12	mApp
Gain Control Voltage [1]	V_{GC}	-	-0.5	4.5	V
Bandwidth Control Voltage [1]	$V_{BWCA/B}$	-	-0.5	4.5	V
Output Voltage Amplitude Control Voltage [1]	V_{OA}	-	-0.5	4.5	V
Gain Control Mode [1]	V_{GCS}	-	-0.5	4.5	V
Shutdown [1]	V_{SHDB}	-	-0.5	4.5	V
Channel Temperature	Tch	-	-	150	°C
Storage Temperature in sealed package	Tst	-	-40	125	°C
ESD (RF Pins)		HBM	250	-	V
ESD (PDx and PDSx Pins)		HBM	250	-	V
ESD (All other pins)		HBM	2000	-	V
Humidity (Storage)	RH	-	5	95	%

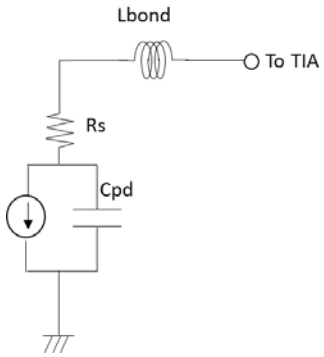
1. If Voltage on control pins > VCC + 0.7V, ESD protection circuits start to draw current. Absolute maximum DC current through the control pins is 5mA.

2.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage	VCC	-	3.07	3.3	3.47	V
Supply Voltage	VCCob	-	3.07	3.3	3.47	V
Total Supply Current for VCC and VCCob [1]	Icc	-	-	200	228	mA
Per Channel Supply Current [1]	Ichan	-	-	100	114	mA
Power Dissipation [1]	Pd	-	-	660	833 at 3.47V	mW
PD Supply Voltage	VPDSx	-	3.0	-	5.25	V
Gain Control Voltage [2][3]	V_{GC}	-	0	-	VCC	V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Bandwidth Control Voltage [3]	$V_{BWCA/B}$	-	0	FLT	VCC	V
Output Amplitude Control Voltage	V_{OA}	-	0	-	VCC	V
Gain Control Mode – MGC mode [3]	V_{GCS}	-	0	-	1.2	V
Gain Control Mode – AGC mode [3]		-	1.8	FLT	VCC	V
Shutdown – Enable [3]	V_{SHDN}	-	0	-	1.2	V
Shutdown – Disable [4]		-	1.8	FLT	VCC	V
Operating Temperature	Tb	-	-5	-	95	°C
Detector Diode Capacitance [5]	Cpd	-	30	40	50	fF
Detector Diode Resistance [5]	Rs	-	10	20	40	Ω
Input Bond Wire [5]	Lb	-	150	250	300	pH

1. Maximum value is given at Max.-BW setting 95°C at V_{CC} = 3.47V. Typical value is given at Mid.-BW setting 27°C at V_{CC} = 3.3V.
2. V_{GC} = V_{CC} corresponds to maximum gain condition and V_{GC} = 0.5V refers to minimum gain condition.
3. For typical operation, it is not necessary to control those pads.
4. In the case of FLT, the pin is pull up to V_{CC}.
5. Please refer to the following PD model.



2.3 Electrical Specifications

All characteristics specified at recommended operating conditions unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Symbol Rate		-	-	96	-	Gbaud
Differential Input RF Current [2]	I_{RFIN}	-	0.03	-	3	mAppd
Input DC Current [3]	I_{DCIN}	Each Input	-	-	4	mA
Input DC Offset Current [4]		-	-0.5	-	0.5	mA
Input DC Level	V_{input}	-	-	0.8	-	V
Differential Trans-impedance Gain	Zt	Min Gain setting	-	-	70	Ω
		Max Gain setting	2,750	3,250	-	
VGA Dynamic Range	ΔVGA	-	30	-	-	dB
Zt Bandwidth	f_{3dB}	3dB down bandwidth with PD model	59	65	-	GHz
Bandwidth Control [5]	BW_{cnt}	-	-3	-	3	GHz
Zt Group Delay Variation	ΔGD	Up to 40GHz	-	-	7	ps
		40G < f < 48G	-	-	12.5	
		48G < f < f3dB	-	-	12.5	
Differential Output Impedance Match	SDD_{22}	50MHz < 32GHz	-	-	-16	dB
		32 to 48 GHz	-	-	-14	
		48 to 64 GHz	-	-	-8	
Noise Density [1]	Ieq	Zt = 3,250Ω, f < f3dB	-	19	-	pA/√Hz
		Zt = 1,000Ω, f < f3dB	-	22	-	
		Zt = 500Ω, f < f3dB	-	28	-	
Total Harmonic Distortion	THD	f = 1GHz, 0.06 < IinRF < 3mAppd 0 < IinDC < 4mAs Vout < 500mVppd	-	0.5	1	%
		f = 1GHz, 0.06 < IinRF < 3mAppd IinDC < 4mAs 500 < Vout < 700mVppd	-	1	1.5	
Zt Common Mode Rejection Ratio	CMRR	100MHz < f < 60GHz	25	40	-	dB
Crosstalk	Xtalk	Up to 60GHz	-	-	-40	dB
Low Frequency Cutoff	f_{Low}	3dB cut-off	-	-	200	kHz
Differential Output Amplitude	Vout	Min. Output	-	-	200	mVppd
		Max. Output	700	-	-	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vout in SHD Mode	$Vout\text{-}_{SHD}$	-	-	-	2	mV_{rms}
AGC Loop Bandwidth		No external capacitors	-	1.1	-	MHz
Gain Control Pin Bandwidth	BW_{GC}	-	-	3	-	MHz
P/N Skew	$Skew_{PN}$	-	-	-	1	ps
I/Q Skew	$Skew_{IQ}$	-	-	-	5	ps
X/Y Skew	$Skew_{XY}$	-	-	-	10	ps
Channel Skew Variation	$Skew_{VAR}$	-	-	-	1	ps
Power Supply Rejection Ratio	PSRR	-	-	11	30	mV/V
Output Monitor (peak detection) Voltage	V_{PK}	-	0.5	-	2.7	V

1. Average input noise at photo diode model current source up to f3dB bandwidth. The input differential current (Iin) is defined as “(Iin/2) (on INP) – (–Iin/2) (on INN)”.
2. Input differential RF current sourced into both differential inputs.
3. Input DC current sourced into each input (IINP and IINN).
4. In case of differential input photodiode configuration, this refers to the relative DC offset current between the two PDs = $I_{INP} – I_{INN}$. The maximum of 0.5mA refers to $I_{INP} > I_{INN}$ and minimum of -0.5mA is when $I_{INN} > I_{INP}$. I_{INP} is the current sourced into I_{INP}, and I_{INN} is the current sourced into I_{NN}.
5. Bandwidth adjust is provided by voltages applied on the BWCA and BWCB pads. See Bandwidth Control truth table.

3. Functional Description

The GX39221 consists of the following:

- Trans-Impedance Amplifier
- Automatic threshold control
- Peak Detection/Output Monitor
- Automatic gain control
- Bandwidth control
- Differential output stage

3.1 Single-ended Input Trans-Impedance Amplifier

The photodiode p (anode) and n (cathode) are bonded directly to INxP and to positive power supply pad VPDx, respectively. VPDx is connected to the VPDSx PAD with RC filter circuit consisting of 25Ω and 6pF on the substrate. Optimum performance will be obtained by supplying the Cathode bias to the VPDSx.

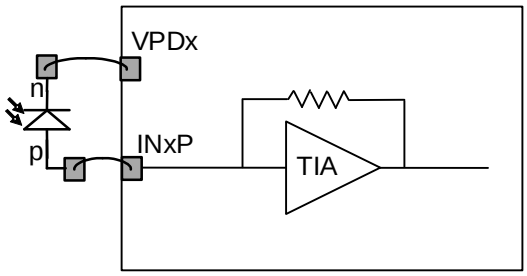


Figure 2. Equivalent Circuit of Trans-Impedance Stage

3.2 Automatic Threshold Control (ATC) Stage

The automatic threshold circuit (ATC) uses a low frequency feedback loop to remove the DC component of the input signal. This DC cancellation centers the signal within the amplifier's dynamic range and reduces pulse-width distortion.

3.3 Peak Detection

Peak detection circuitry provides a measurement in voltage of the average absolute value of the peak-to-peak output swing. The output voltage signal is rectified and properly amplified to provide a suitable DC voltage on the OMON pad. Typical OMON slope will result according to Figure 4.

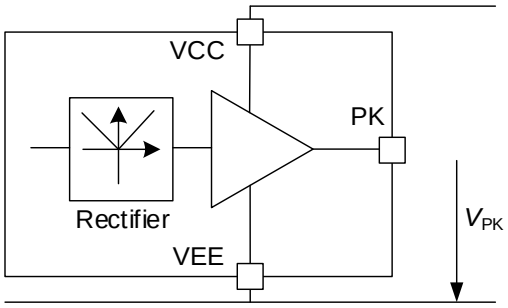


Figure 3. Peak Detection Circuitry

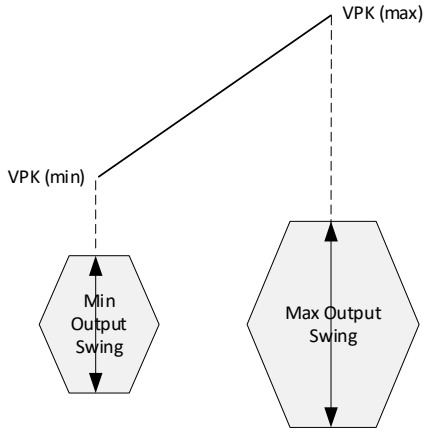


Figure 4. Typical V_{PK} Slope

3.4 Automatic Gain Control (AGC)

The AGC circuit consists of a variable gain amplifier and an automatic gain-control mechanism that keeps the output swing constant over a wide range of input swings. The gain of the amplifier is controlled by the rectified signal amplitude. The DC transfer function of an AGC amplifier depends on the input signal strength as shown in Figure 4. For very large signals, the AGC cannot reduce its gain any further and limiting will eventually occur. This defines the upper end of the input dynamic range. The gain is the slope of the linear region.

The linear operation region shown in Figure 5 defines the maximum peak-to-peak input signal that is amplified with low total harmonic distortion. The AGC circuit is enabled when GCS = high or left floating.

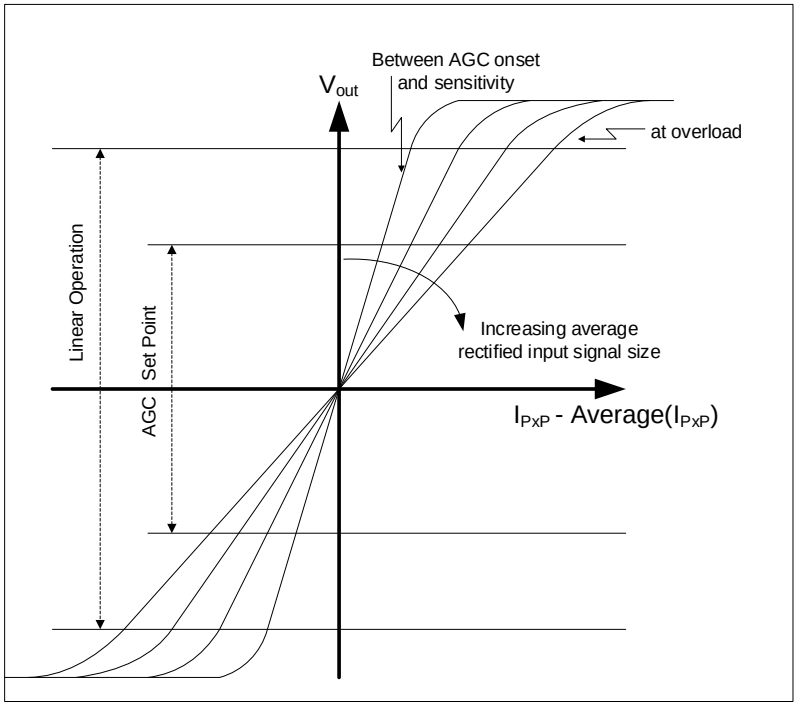


Figure 5. Channel Characteristic when the AGC Circuit is Switched On

The set point of the AGC is determined by the voltage applied to the VOA pin. The output voltage swing remains constant independent of the input current swing as long as the gain required for the operating condition is within the dynamic range of the amplifier.

3.5 Bandwidth Control

The GX39221 has bandwidth control circuitry which is controlled by the BWCA and BWCB pads. The SDD21 bandwidth and peaking versus the bandwidth setting is shown below.

BWC1	BWC2	Approximate Bandwidth (GHz)	Approximate Peaking (dB)
Low	**Low**	**55.4**	**3.2**
Low	Floating	58.2	4.6
Floating	Low	60	4
Floating	**Floating**	**62.7**	**5.1**
Floating	High	64.8	6
High	Floating	67.3	5.4
High	**High**	**69.5**	**6.5**

3.6 Differential Output Stage

The differential output stage is compatible with CML standards. The load impedances at the two outputs should be matched to minimize switching noise.

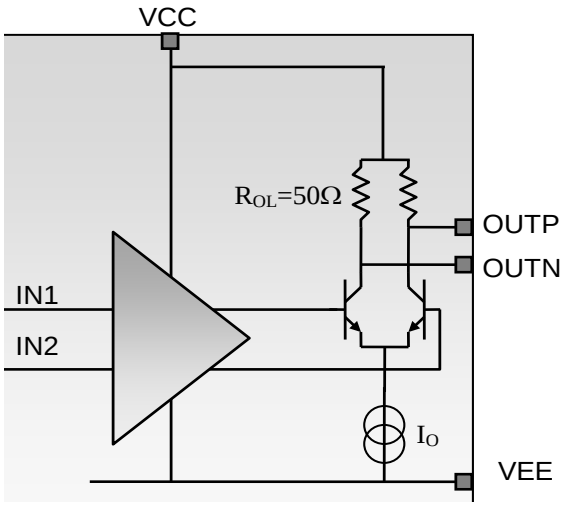
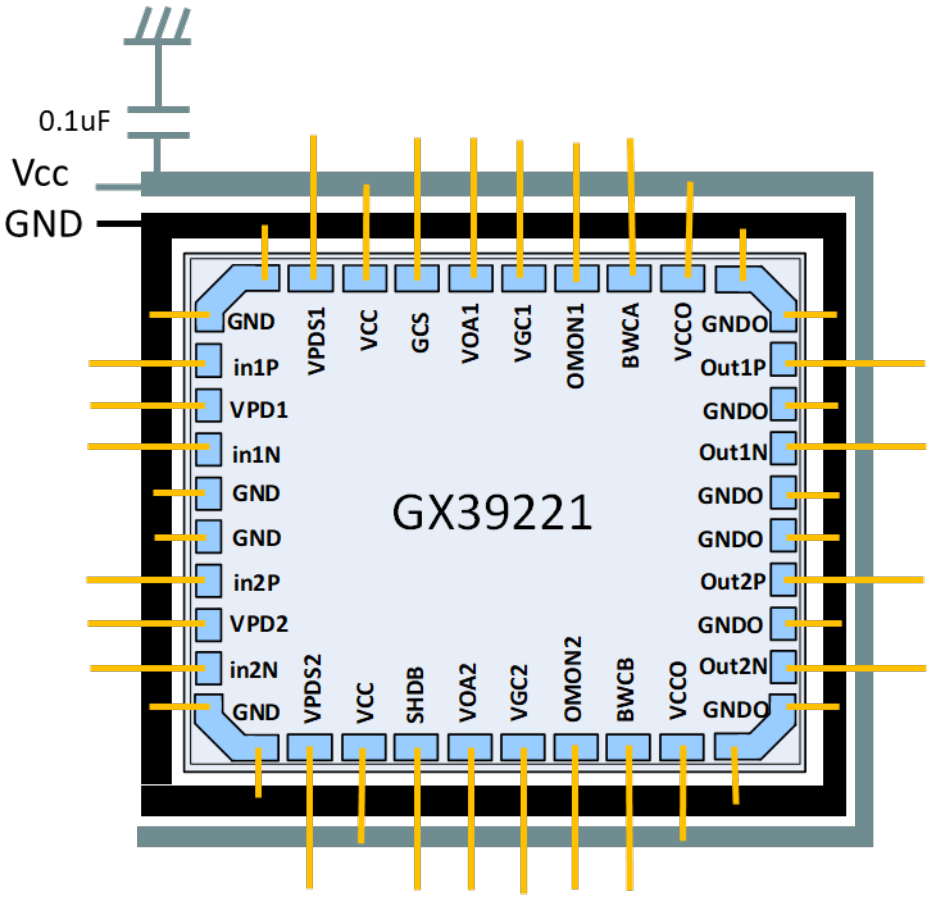


Figure 6. Output Stage Equivalent Circuit

4. Assembly Drawing



1. All the bondwire lengths are recommended to be as short as possible. The following inductance values are suggested:, 300pH maximum for RF input/output ports, 400pH maximum for power supply, 400pH maximum for ground ports, and 400pH maximum for control and monitor ports.
2. One large capacitor at supply is recommended.
3. No external capacitor is needed at VGC1 or VGC2.

5. Ordering Information

Part Number	Description	Temperature Range
GX39221-DNT	Die: 1.845 × 1.515 × 0.1 mm^3	-5°C to +95°C

6. Revision History

Revision	Date	Description
1.00	Nov 28, 2022	Initial release.

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