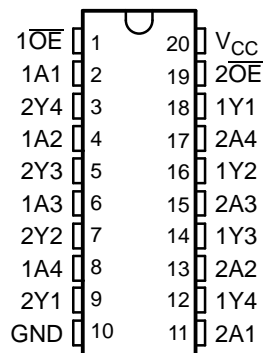


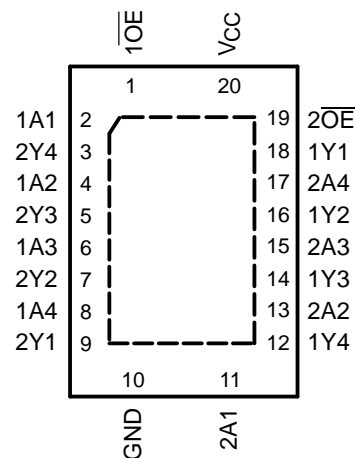
FEATURES

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V V_{CC} Operation
- Typical $t_{pd} = 5.4$ ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV244AT is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|----------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LV244ATRGYR | VV244 |
| | SOIC – DW | Tube of 25 | SN74LV244ATDW | LV244AT |
| | | Reel of 2000 | SN74LV244ATDWR | |
| | SOP – NS | Reel of 2000 | SN74LV244ATNSR | 74LV244AT |
| | SSOP – DB | Reel of 2000 | SN74LV244ATDBR | LV244AT |
| | TSSOP – PW | Tube of 70 | SN74LV244ATPW | LV244AT |
| | | Reel of 2000 | SN74LV244ATPWR | |
| | | Reel of 250 | SN74LV244ATPWT | |
| TVSOP – DGV | Reel of 2000 | SN74LV244ATDGV | LV244AT | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LV244AT
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES572C–JUNE 2004–REVISED AUGUST 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

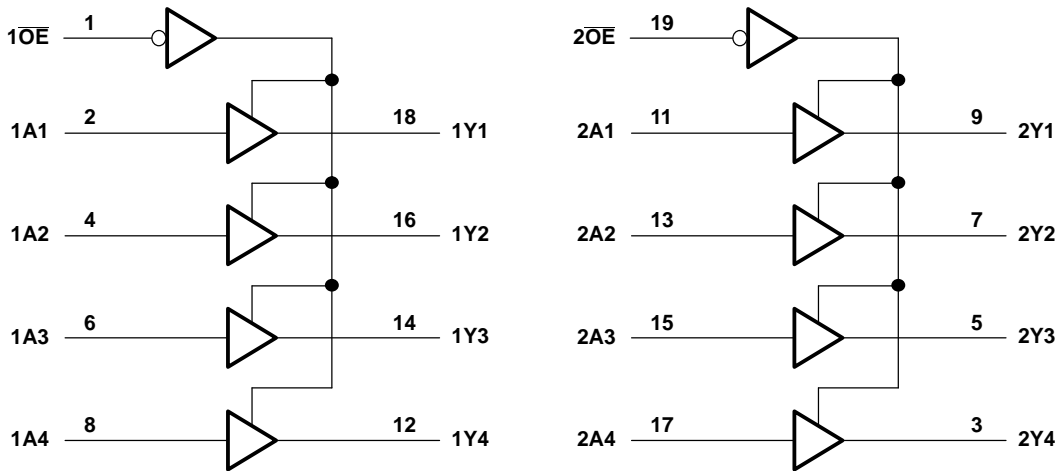
To ensure the high-impedance state during power up or power down, \overline{OE} shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE
(EACH 4-BIT BUFFER/DRIVER)

| INPUTS | | OUTPUT Y |
|-----------------|---|-------------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |
| H | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|----------------------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 7 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 7 | V |
| V_O | Output voltage range applied in the high or low state ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current $V_I < 0$ | | -20 | mA |
| I_{OK} | Output clamp current $V_O < 0$ | | -50 | mA |
| I_O | Continuous output current $V_O = 0$ to V_{CC} | | ± 35 | mA |
| | Continuous current through V_{CC} or GND | | ± 70 | mA |
| θ_{JA} | Package thermal impedance | DB package ⁽⁴⁾ | 70 | °C/W |
| | | DGV package ⁽⁴⁾ | 92 | |
| | | DW package ⁽⁴⁾ | 58 | |
| | | NS package ⁽⁴⁾ | 60 | |
| | | PW package ⁽⁴⁾ | 83 | |
| | | RGY package ⁽⁵⁾ | 37 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|---|-------------------|-----|----------|
| V_{CC} | Supply voltage | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage $V_{CC} = 4.5$ V to 5.5 V | 2 | | V |
| V_{IL} | Low-level input voltage $V_{CC} = 4.5$ V to 5.5 V | | 0.8 | V |
| V_I | Input voltage | 0 | 5.5 | V |
| V_O | Output voltage | High or low state | 0 | V_{CC} |
| | | 3-state | 0 | 5.5 |
| I_{OH} | High-level output current $V_{CC} = 4.5$ V to 5.5 V | | -16 | mA |
| I_{OL} | Low-level output current $V_{CC} = 4.5$ V to 5.5 V | | 16 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate $V_{CC} = 4.5$ V to 5.5 V | | 20 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LV244AT

OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES572C–JUNE 2004–REVISED AUGUST 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | T _A = –40°C to 85°C | | UNIT |
|---------------------------------|---|-----------------|-----------------------|-----|-------|--------------------------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | I _{OH} = –16 mA | 4.5 V | 3.8 | | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | 0 | 0.1 | | 0.1 | V |
| | I _{OL} = 16 mA | 4.5 V | | | 0.55 | | 0.55 | |
| I _I | V _I = 5.5 V or GND | 0 to 5.5 V | | | ±0.1 | | ±1 | μA |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | ±0.25 | | ±2.5 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 20 | μA |
| ΔI _{CC} ⁽¹⁾ | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | | 1.5 | mA |
| I _{off} | V _I or V _O = 0 to 5.5 V | 0 | | | 0.5 | | 5 | μA |
| C _i | V _I = V _{CC} or GND | | | 4.5 | | | | pF |

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------|--------------|-------------|------------------------|-----------------------|-----|------|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t _{PLH} | A or B | B or A | C _L = 15 pF | 2.6 | 5/4 | 7.4 | 1 | 8.5 | ns |
| t _{PHL} | | | | 2.4 | 5.4 | 7.4 | 1 | 8.5 | |
| t _{PZH} | OE | A or B | C _L = 15 pF | 2.2 | 7.7 | 10.4 | 1 | 12 | ns |
| t _{PZL} | | | | 2.7 | 7.7 | 10.4 | 1 | 12 | |
| t _{PHZ} | OE | A or B | C _L = 15 pF | 2.2 | 3.9 | 7.7 | 1 | 8 | ns |
| t _{PLZ} | | | | 2.5 | 3.9 | 7.7 | 1 | 8 | |
| t _{PLH} | A or B | B or A | C _L = 50 pF | 4 | 5.9 | 8.9 | 1 | 9.5 | ns |
| t _{PHL} | | | | 4.7 | 5.9 | 8.9 | 1 | 9.5 | |
| t _{PZH} | OE | A or B | C _L = 50 pF | 3.9 | 8.2 | 11.4 | 1 | 13 | ns |
| t _{PZL} | | | | 4.9 | 8.2 | 11.4 | 1 | 13 | |
| t _{PHZ} | OE | A or B | C _L = 50 pF | 3.3 | 8.8 | 11.4 | 1 | 13 | ns |
| t _{PLZ} | | | | 3.2 | 8.8 | 11.4 | 1 | 13 | |
| t _{sk(o)} | | | C _L = 50 pF | | | 1 | | 1 | ns |

Noise Characteristics⁽¹⁾

V_{CC} = 5 V, C_L = 50 pF

| PARAMETER | DESCRIPTION | T _A = 25°C | | | UNIT |
|--------------------|---|-----------------------|-----|-----|------|
| | | MIN | TYP | MAX | |
| V _{OL(P)} | Quiet output, maximum dynamic V _{OL} | 0.8 | | 1 | V |
| V _{OL(V)} | Quiet output, minimum dynamic V _{OL} | –0.8 | | –1 | V |
| V _{OH(V)} | Quiet output, minimum dynamic V _{OH} | | 4 | | V |
| V _{IH(D)} | High-level dynamic input voltage | | 2 | | V |
| V _{IL(D)} | Low-level dynamic input voltage | | | 0.8 | V |

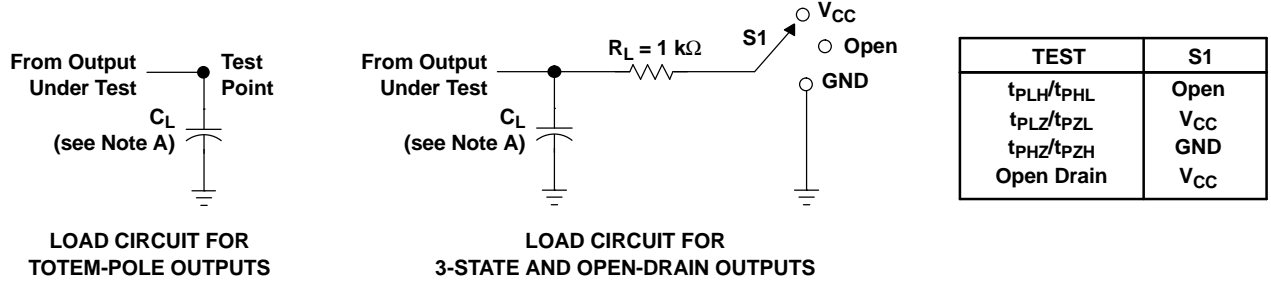
(1) Characteristics are for surface-mount packages only.

Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

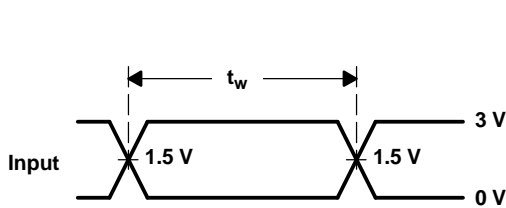
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|---|-----|------|
| C_{pd} | Power dissipation capacitance | Outputs enabled $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 8 | pF |

PARAMETER MEASUREMENT INFORMATION

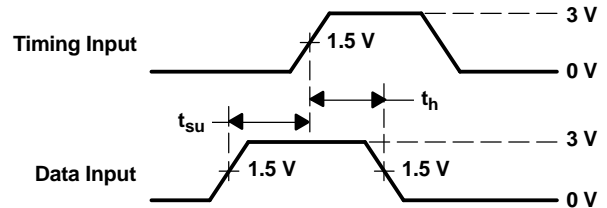


LOAD CIRCUIT FOR
 TOTEM-POLE OUTPUTS

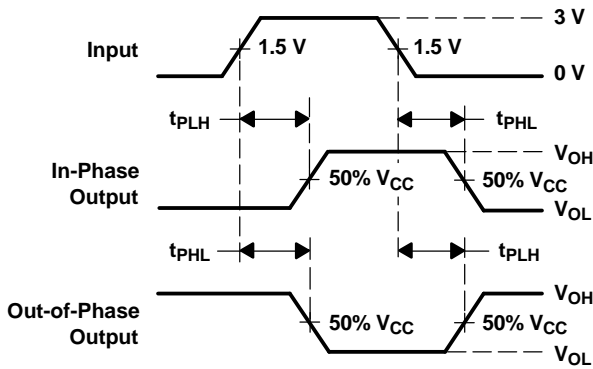
LOAD CIRCUIT FOR
 3-STATE AND OPEN-DRAIN OUTPUTS



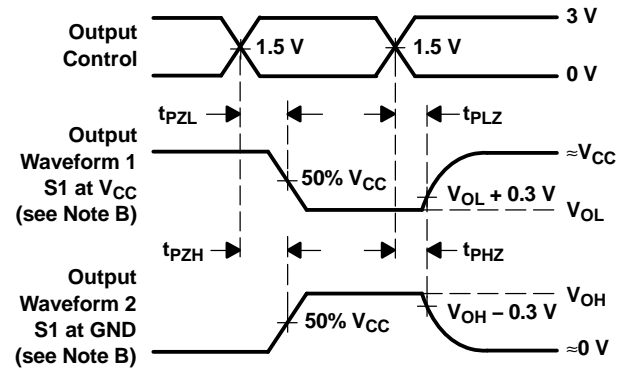
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV244ATDWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV244AT | Samples |
| SN74LV244ATNSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV244AT | Samples |
| SN74LV244ATPW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV244AT | Samples |
| SN74LV244ATPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV244AT | Samples |
| SN74LV244ATRGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VV244 | Samples |
| SN74LV244ATRGYRG4 | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VV244 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV244ATDWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LV244ATNSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 12.0 | 24.0 | Q1 |
| SN74LV244ATPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV244ATRGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV244ATDWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV244ATNSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV244ATPWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV244ATRGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

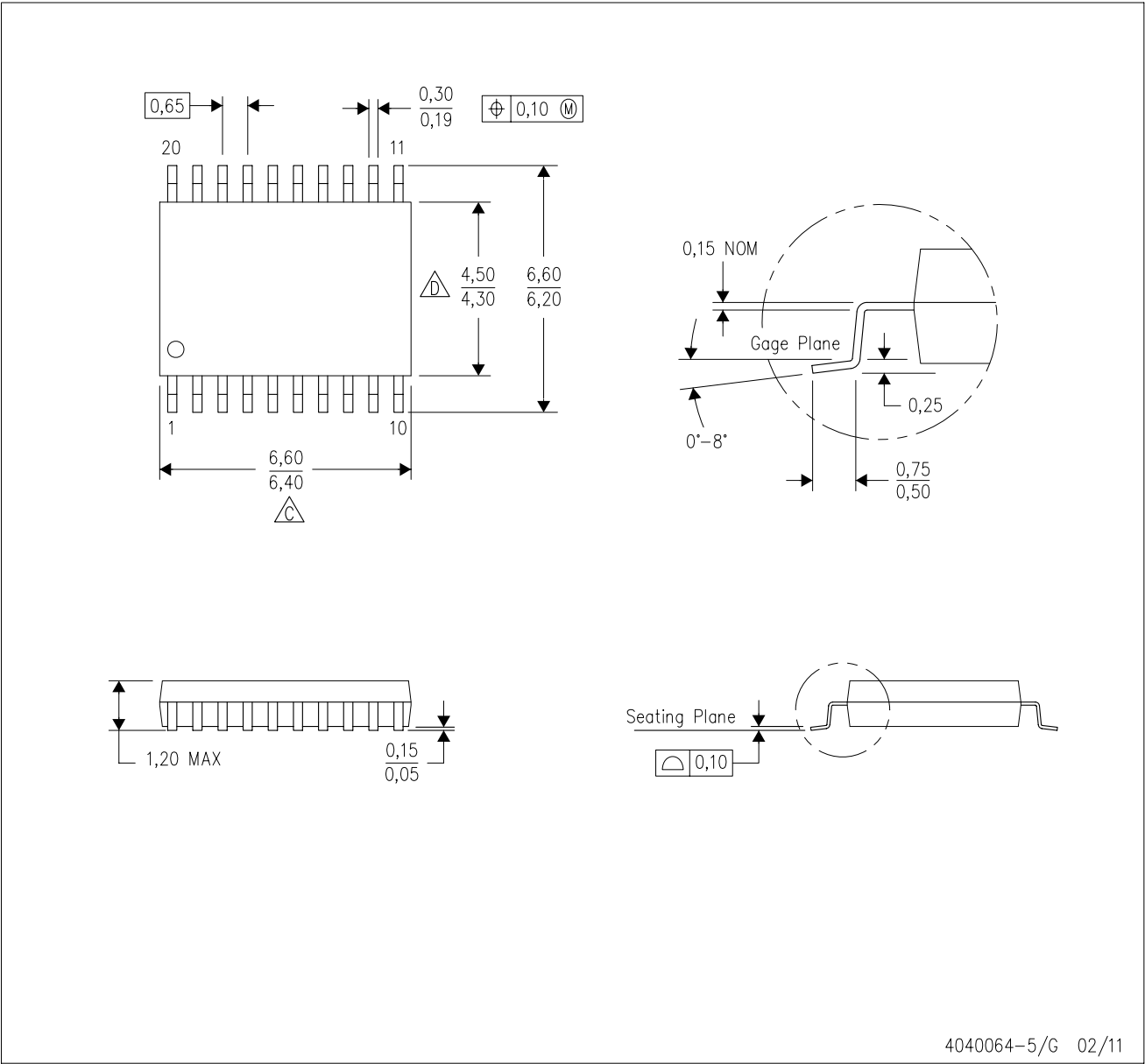
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

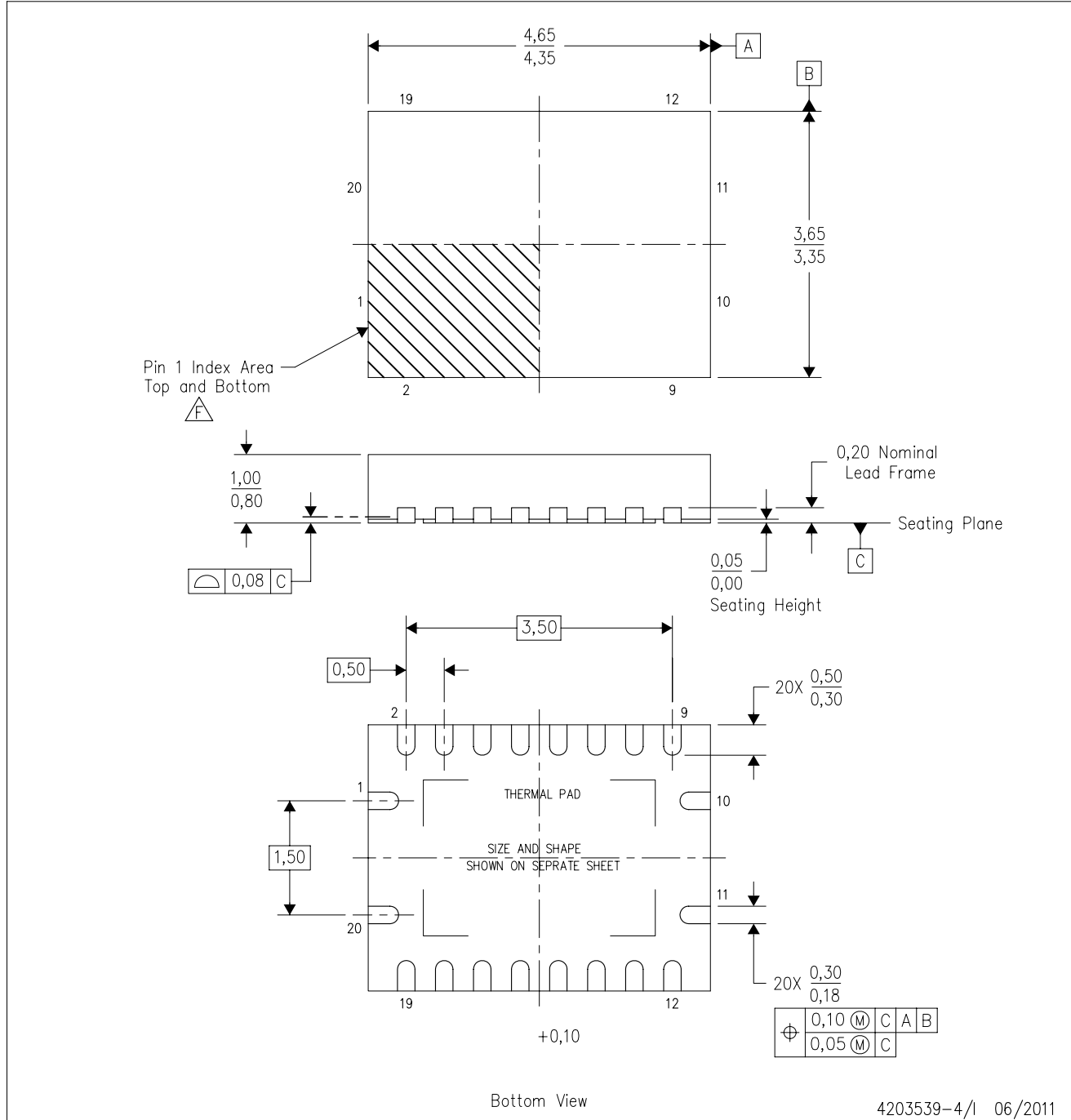
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

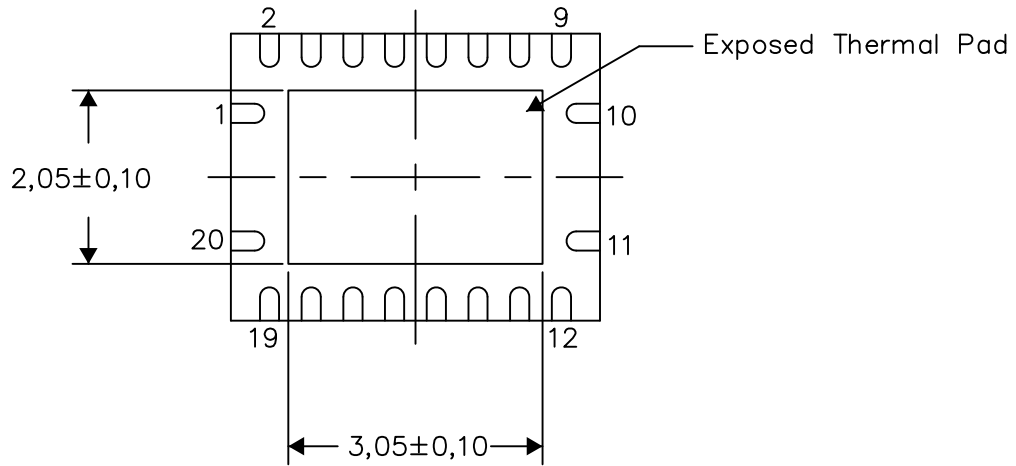
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

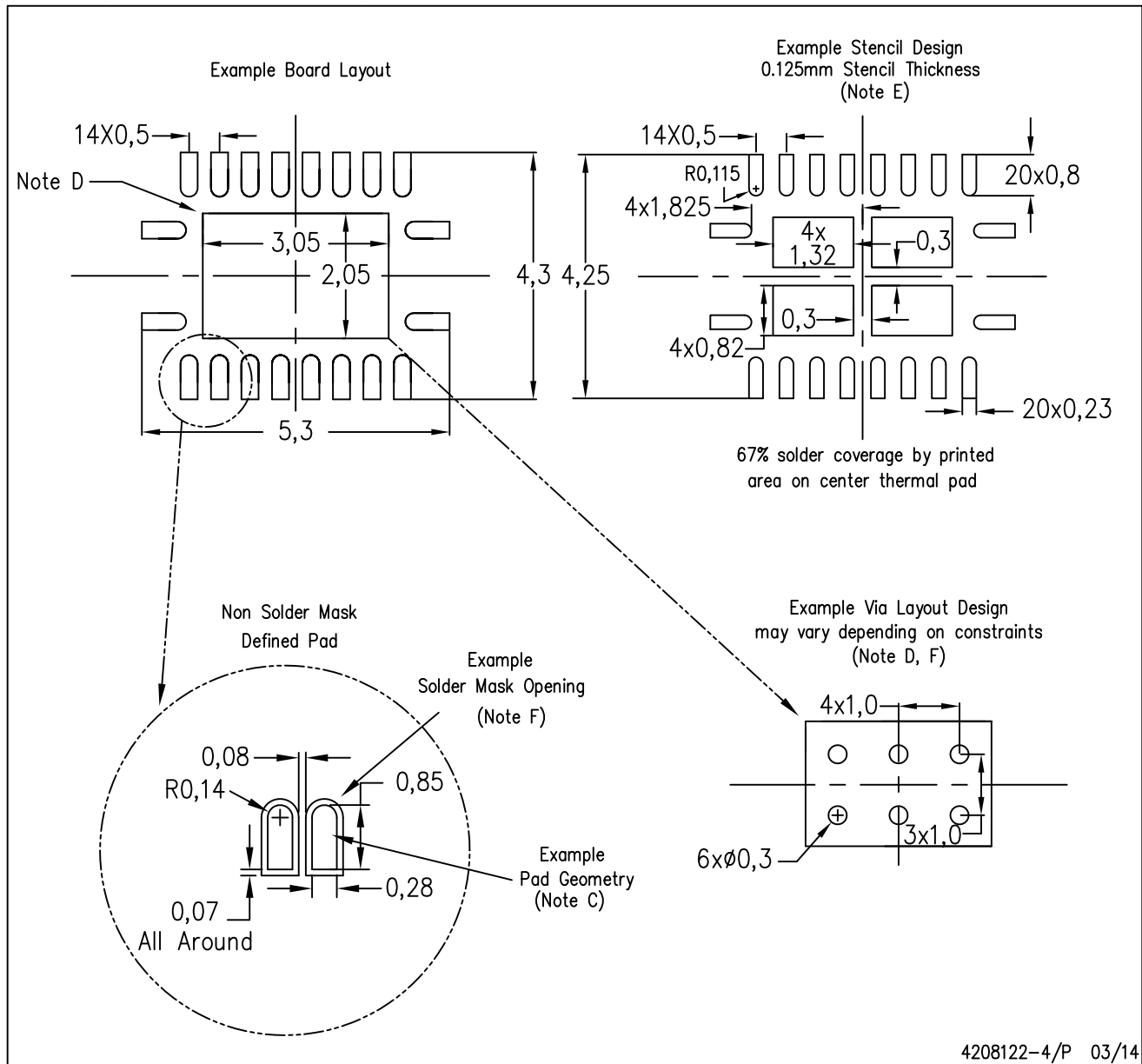
Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

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