RENESAS

R7F0C901B2, R7F0C902B2

RENESAS MCU

True Low Power Platform (as low as 66 μA/MHz), 1.6 V to 5.5 V
operation, 48 to 64 Kbyte Flash, 41 DMIPS at 32 MHz, for General Purpose Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 1.6 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μA, (LVD enabled): 0.31 μA
- Snooze: 0.70 mA (UART), 1.20 mA (ADC)
- Operating: 66 μA/MHz

16-bit RL78 CPU Core
- Delivers 41 DMIPS at maximum operating frequency of 32 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Main Flash Memory
- Density: 48 KB to 64 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory
- Data Flash with background operation
- Data flash size: 4 KB
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM
- 4 KB size
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 32 MHz with +/− 1% accuracy over voltage (1.8 V to 5.5 V) and temperature (−20 °C to 85 °C)
- Pre-configured settings: 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz

Reset and Supply Management
- Power-on reset (POR) generator
- Low voltage detection (LVD) with 14 setting options (Interrupt and/or reset function)

Multiple Communication Interfaces
- Up to 3 x simplified I²C
- Up to 3 x CSI/SPI (7-, 8-bit)
- Up to 3 x UART (7-, 8-, 9-bit)

Extended-Function Timers
- Multi-function 16-bit timers: Up to 8 channels
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer : 1 channel (window function)

Rich Analog
- ADC: Up to 8 channels, 10-bit resolution, 2.1 μs conversion time
- Supports 1.6 V
- Internal voltage reference (1.45 V)

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/ frequency detection
- ADC self-test

General Purpose I/O
- 5V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support
- Different potential interface support: Can connect to a 1.8/2.5/3 V device

Operating Ambient Temperature
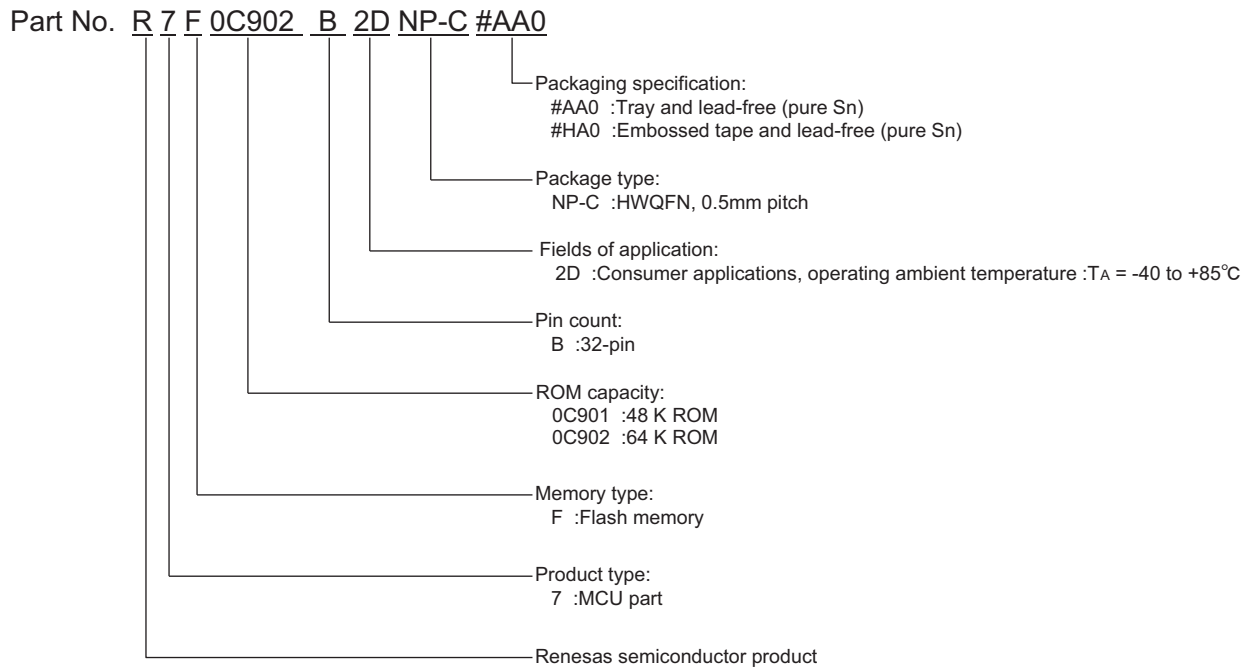- Standard: −40 °C to +85 °C

Package Type and Pin Count
32-pin HWQFN (5 x 5 mm, 0.5 mm pitch)

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	R7F0C901B2, R7F0C902B2
			32 pins
64 KB	4 KB	4 KB [Note]	R7F0C902B2
48 KB	4 KB	4 KB [Note]	R7F0C901B2

Notes   This is about 3 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3 in the RL78/G13 User's Manual Hardware**)

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of R7F0C901B2, R7F0C902B2

Part No. R 7 F 0C902 B 2D NP-C #AA0

Packaging specification:
#AA0 :Tray and lead-free (pure Sn)
#HA0 :Embossed tape and lead-free (pure Sn)

Package type:
NP-C :HWQFN, 0.5mm pitch

Fields of application:
2D :Consumer applications, operating ambient temperature :T_A = -40 to +85℃

Pin count:
B :32-pin

ROM capacity:
0C901 :48 K ROM
0C902 :64 K ROM

Memory type:
F :Flash memory

Product type:
7 :MCU part

Renesas semiconductor product

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Flash ROM	RAM	Packaging specification and environmental compliance	Ordering part number
32 pins	32-pin plastic HWQFN (5 x 5 mm, 0.5mm pitch)	64 KB	4 KB	Tray and lead-free (pure Sn)	R7F0C902B2DNP-C#AA0
				Embossed tape and lead-free (pure Sn)	R7F0C902B2DNP-C#HA0
		48 KB		Tray and lead-free (pure Sn)	R7F0C901B2DNP-C#AA0
				Embossed tape and lead-free (pure Sn)	R7F0C901B2DNP-C#HA0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of R7F0C901B2, R7F0C902B2**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)
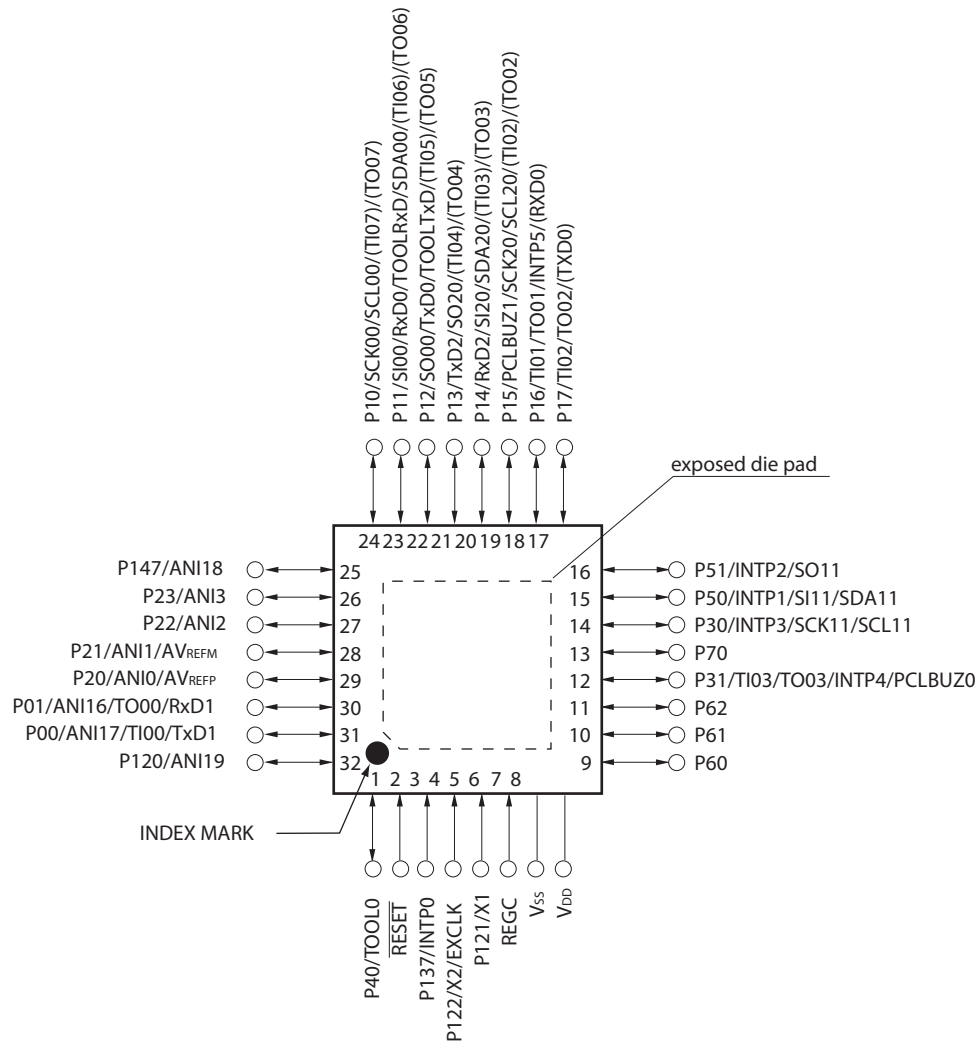
**Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remarks 1. For pin identification, see **1.4 Pin Identification**.
   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual Hardware**.
   3. It is recommended to connect an exposed die pad to Vss.

1.4 Pin Identification

ANI0 to ANI3		REGC:	Regulator capacitance
ANI16 to ANI19:	Analog input	$\overline{\text{RESET}}$:	Reset
AV$_{REFM}$:	A/D converter reference potential (− side) input	RxD0 to RxD2:	Receive data
		SCK00, SCK11, SCK20,:	Serial clock input/output
AV$_{REFP}$:	A/D converter reference potential (+ side) input	SCL00, SCL11, SCL20,:	Serial clock output
		SDA00, SDA11, SDA20:	Serial data input/output
EXCLK:	External clock input (Main system clock)	SI00, SI11, SI20:	Serial data input
		SO00, SO11, SO20:	Serial data output
INTP0 to INTP5:	Interrupt request from peripheral	TI00 to TI07:	Timer input
		TO00 to TO07:	Timer output
P00, P01:	Port 0	TOOL0:	Data input/output for tool
P10 to P17:	Port 1	TOOLRxD, TOOLTxD:	Data input/output for external device
P20 to P23:	Port 2	TxD0 to TxD2:	Transmit data
P30, P31:	Port 3	V$_{DD}$:	Power supply
P40:	Port 4	V$_{SS}$:	Ground
P50, P51:	Port 5	X1, X2:	Crystal oscillator (main system clock)
P60 to P62:	Port 6		
P70:	Port 7		
P120 to P122:	Port 12		
P137:	Port 13		
P147:	Port 14		
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output		

1.5 Block Diagram
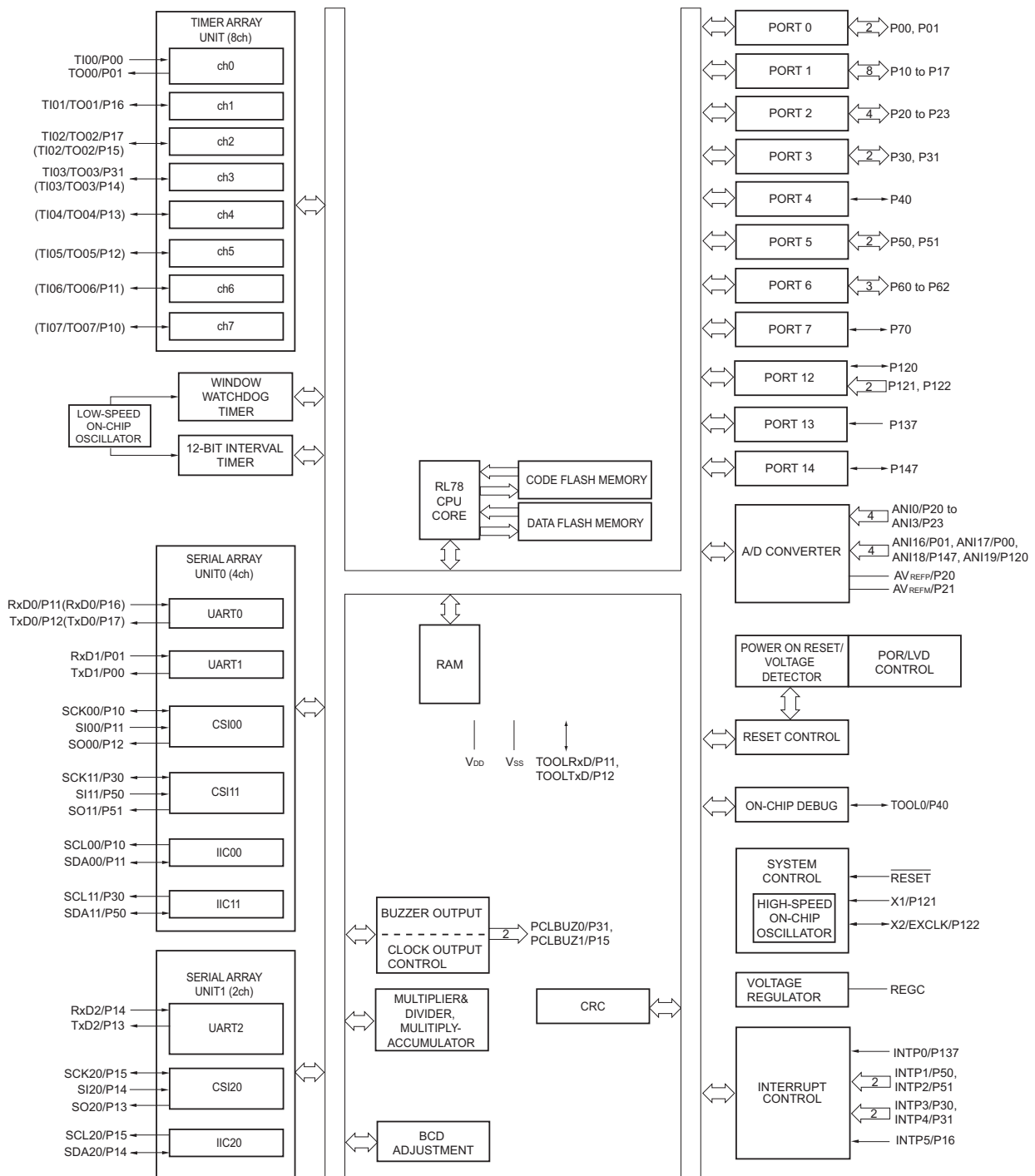
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual Hardware**.

1.6 Outline of Functions

**Caution   This outline describes the functions at the time when Peripheral I/O redirection register (PIOR)
is set to 00H.**

(1/2)

Item		32-pin	
		R7F0C901B2	R7F0C902B2
Code flash memory (KB)		48	64
Data flash memory (KB)		4	
RAM (KB)		4[Note1]	
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V	
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
Subsystem clock		−	
Low-speed on-chip oscillator		15 kHz (TYP.)	
General-purpose registers		(8-bit register × 8) × 4 banks	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	28	
	CMOS I/O	22 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)	
	CMOS input	3	
	CMOS output	−	
	N-ch O.D. I/O (withstand voltage: 6 V)	3	
Timer	16-bit timer	8 channels	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	-	
	12-bit interval timer (IT)	1 channel	
	Timer output	4 channels (PWM outputs: 3[Note 2]), 8 channels (PWM outputs: 7[Note 2])[Note 3]	
	RTC output	−	

Notes 1. This is about 3 KB when the self-programming function and data flash function are used. (For details,
see **CHAPTER 3 in the RL78/G13 User's Manual Hardware**)

　　　2. The number of PWM outputs varies depending on the setting of channels in use (the number of
masters and slaves). (**6.9.3   Operation as multiple PWM output function in the RL78/G13 User's
Manual Hardware**)

　　　3.　When setting to PIOR0 = 1

(2/2)

Item		32-pin	
		R7F0C901B2	R7F0C902B2
Clock output/buzzer output		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)	
8/10-bit resolution A/D converter		8 channels	
Serial interface		• CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel	
	I^{2}C bus	−	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)	
DMA controller		−	
Vectored interrupt sources	Internal	23	
	External	6	
Key interrupt		−	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)	
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V	
Operating ambient temperature		T_A = -40 to +85°C (2D: Consumer applications)	

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.
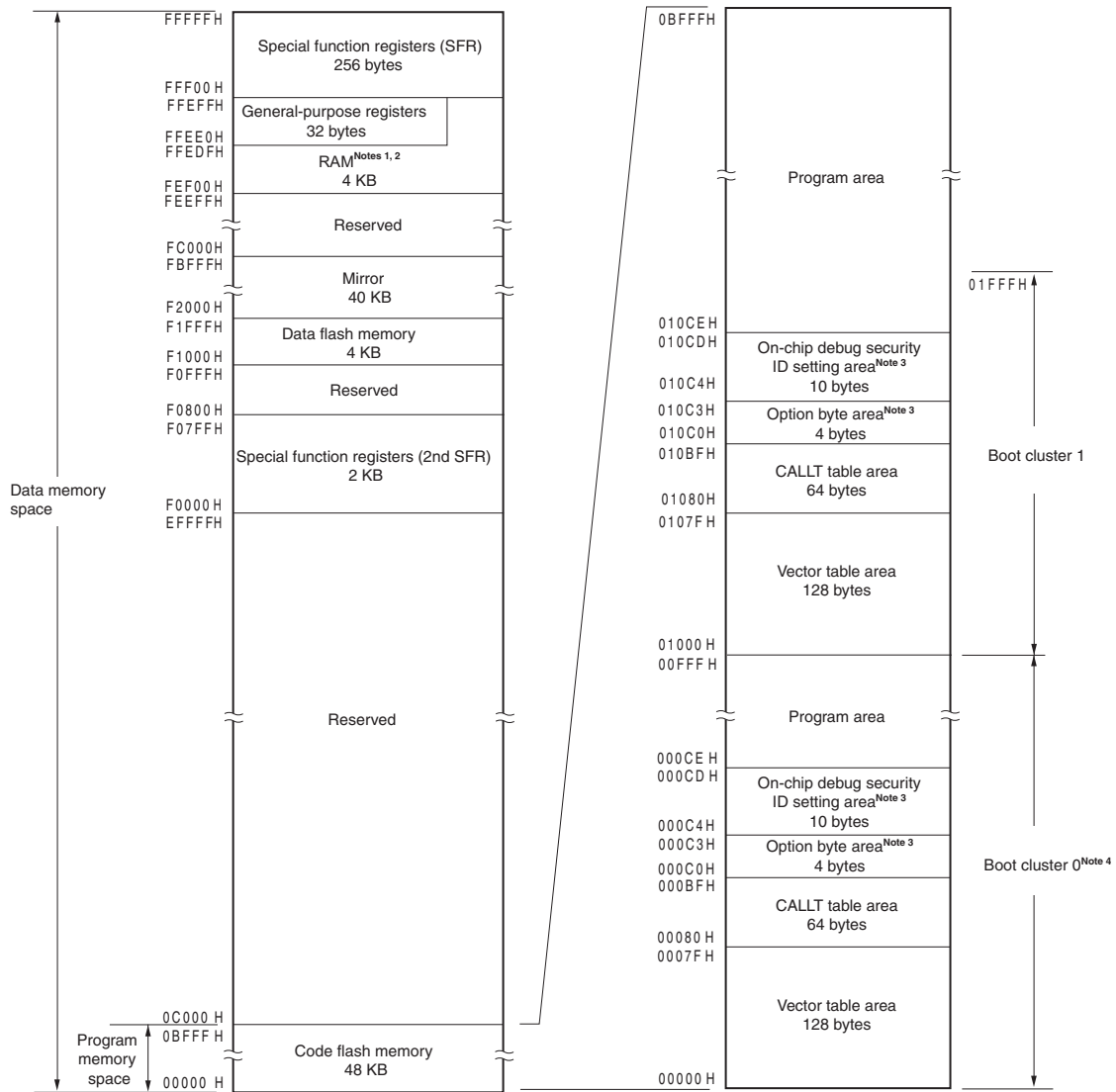
2. PIN FUNCTIONS

Refer to 32-pin of **CHAPTER 2 PIN FUNCTIONS** in the **RL78/G13 User's Manual Hardware**.

However, R7F0C901B2, R7F0C902B2 does not have IICA0 related pins.

3. CPU ARCHITECTURE

Refer to 48 KB and 64 KB code flash memories of **CHAPTER 3 CPU ARCHITECTURE** in the **RL78/G13 User's Manual Hardware**.
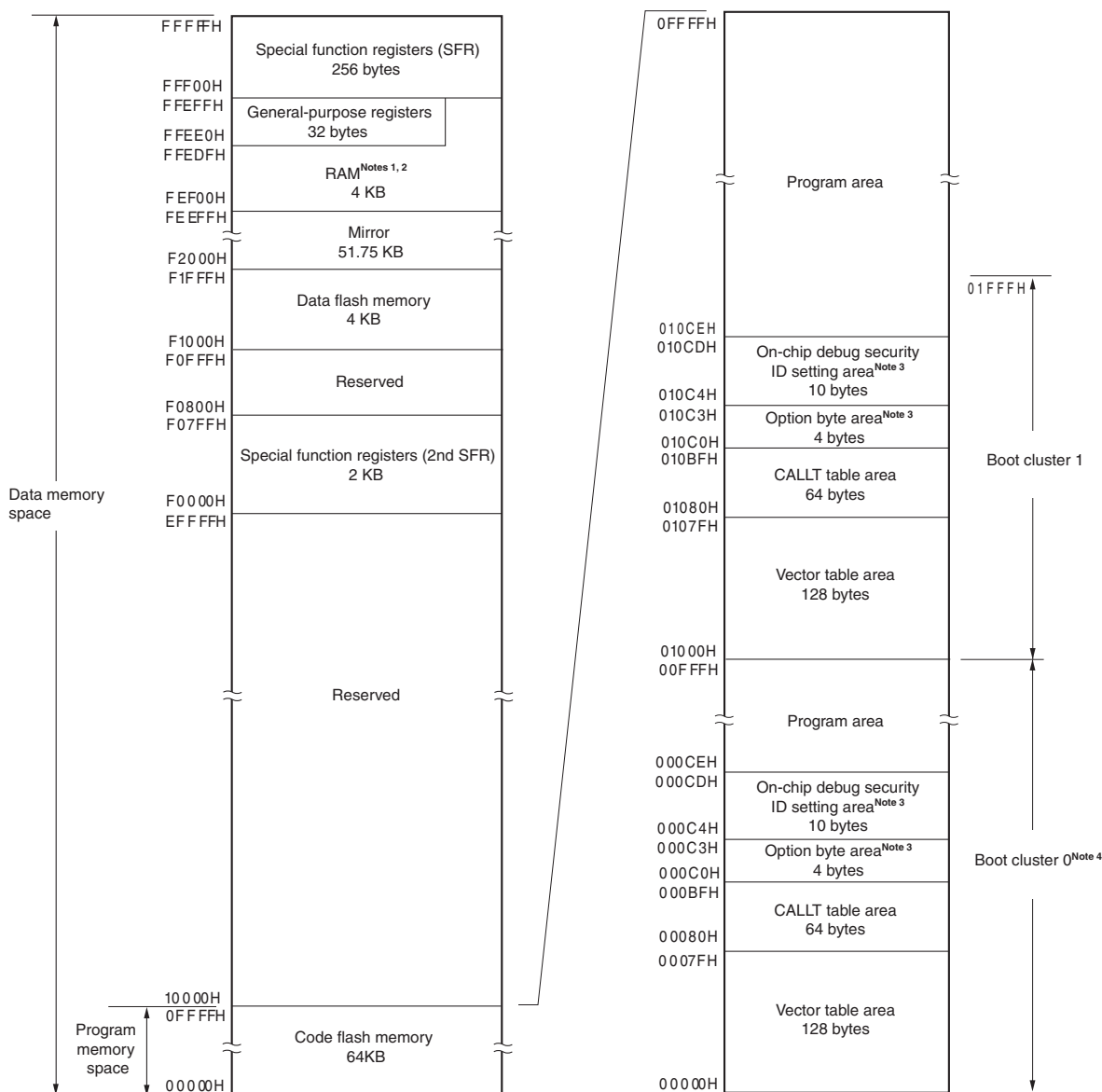
figure 3-1 Memory Map(R7F0C901)

Notes1. Do not allocate RAM addresses which are used as a stack area, a data buffer, a branch destination of vector interrupt processing to the area FFE20H to FFEDFH when performing self-programming and rewriting the data flash memory. Also, use of the area FEF00H to FF309H is prohibited, because this area is used for each library.

2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH. When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see 25.7 Security Setting in the RL78/G13 User's Manual Hardware).

Caution   While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively. Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 22.3.3 RAM parity error detection function in the RL78/G13 User's Manual Hardware.

figure 3-2 Memory Map(R7F0C902)

Notes 1. Do not allocate RAM addresses which are used as a stack area, a data buffer, a branch destination of vector interrupt processing to the area FFE20H to FFEDFH when performing self-programming and rewriting the data flash memory. Also, use of the area FEF00H to FF309H is prohibited, because this area is used for each library.

2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH. When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4Hto 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see 25.7 Security Setting in the RL78/G13 User's Manual Hardware).

Caution　While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas　　　where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively. Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 22.3.3 RAM parity error detection function in the RL78/G13 User's Manual Hardware.

4. PORT FUNCTIONS

Refer to 32-pin of **CHAPTER 4 PORT FUNCTIONS** in the **RL78/G13 User's Manual Hardware**.

However, R7F0C901B2, R7F0C902B2 does not have IICA0 related pins.

5. CLOCK GENERATOR

Refer to 32-pin of **CHAPTER 5 CLOCK GENERATOR** in the **RL78/G13 User's Manual Hardware**.

However, bit 4 is deleted and bit 7 (RTCEN) is changed to TMKAEN in PER0 register of R7F0C901B2, R7F0C902B2.

6. TIMER ARRAY UNIT

Refer to 32-pin of **CHAPTER 6 TIMER ARRAY UNIT** in the **RL78/G13 User's Manual Hardware**.

However, R7F0C901B2, R7F0C902B2 does not have ISC register.

7. 12-BIT INTERVAL TIMER

Refer to **CHAPTER 8 12-BIT INTERVAL TIMER** in the **RL78/G13 User's Manual Hardware**.

8. CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

Refer to **CHAPTER 9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER** in the **RL78/G13 User's Manual Hardware**.

9. WATCHDOG TIMER

Refer to **CHAPTER 10 WATCHDOG TIMER** in the **RL78/G13 User's Manual Hardware**.

10. A/D CONVERTER

Refer to **CHAPTER 11 A/D CONVERTER** in the **RL78/G13 User's Manual Hardware**.

However, R7F0C901B2, R7F0C902B2 does not have temperature sensor and INTRTC, and hardware trigger can not be selected in ADM1 register.

11. SERIAL ARRAY UNIT

Refer to 32-pin of **CHAPTER 12 SERIAL ARRAY UNIT** in the **RL78/G13 User's Manual Hardware**.

However, R7F0C901B2, R7F0C902B2 does not have LIN function and ISC register.

12. MULTIPLIER AND DIVIDER/MULTIPLY-ACCUMULATOR

Refer to **CHAPTER 14 MULTIPLIER AND DIVIDER/MULTIPLY-ACCUMULATOR** in the **RL78/G13 User's Manual Hardware**

13. INTERRUPT FUNCTIONS

Refer to 32-pin of **16 INTERRUPT FUNCTIONS** in the **RL78/G13 User's Manual Hardware**.

However, R7F0C901B2, R7F0C902B2 does not have DMA, IICA0 and RTC related interrupt sources.

14. STANDBY FUNCTION

Refer to **CHAPTER 18 STANDBY FUNCTION** in the **RL78/G13 User's Manual Hardware**.

However, R7F0C901B2, R7F0C902B2 does not have DMA, IICA0 and RTC related items.

15. RESET FUNCTION

Refer to **CHAPTER 19 RESET FUNCTION** in the **RL78/G13 User's Manual Hardware**.

16. POWER-ON-RESET CIRCUIT

Refer to **CHAPTER 20 POWER-ON-RESET CIRCUIT** in the **RL78/G13 User's Manual Hardware**.

17. VOLTAGE DETECTOR

Refer to **CHAPTER 21 VOLTAGE DETECTOR** in the **RL78/G13 User's Manual Hardware**.

18. SAFETY FUNCTIONS

Refer to **CHAPTER 22 SAFETY FUNCTIONS** in the **RL78/G13 User's Manual Hardware**.

19. REGULATOR

Refer to **CHAPTER 23 REGULATOR** in the **RL78/G13 User's Manual Hardware**.

20. OPTION BYTE

Refer to **CHAPTER 24 OPTION BYTE** in the **RL78/G13 User's Manual Hardware**.

21. FLASH MEMORY

Refer to 32-pin of **CHAPTER 25 FLASH MEMORY** in the **RL78/G13 User's Manual Hardware**.

Table 21-1. Example of Signature Data

Field name	Description	Number of transmit data	Data (hexadecimal)
Device code	RL78 protocol A	3 bytes	10 00 06
Device name	R7F0C901	10 bytes	52 = "R" 37 = "7" 46= "F" 30 = "0" 43= "C" 39 = "9" 30 = "0" 31 = "1" 20 = " " 20 = " "
Code flash memory area last address	Code flash memory area 00000H to 0BFFFH (48 KB)	3 bytes	FF BF 00
Data flash memory area last address	Data flash memory area F1000H to F1FFFH (4 KB)	3 bytes	FF 1F 0F
Firmware version	Ver. 1.23	3 bytes	01 02 03

22. ON-CHIP DEBUG FUNCTION

Refer to **CHAPTER 26 ON-CHIP DEBUG FUNCTION** in the **RL78/G13 User's Manual Hardware**.

23. BCD CORRECTION CIRCUIT

Refer to **CHAPTER 27 BCD CORRECTION CIRCUIT** in the **RL78/G13 User's Manual Hardware**.

24. INSTRUCTION SET

Refer to **CHAPTER 28 INSTRUCTION SET** in the **RL78/G13 User's Manual Hardware**.

25. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)

Cautions   The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

25.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3[Note 1]	V
Input voltage	V_{I1}	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	−0.3 to V_{DD} +0.3[Note 2]	V
	V_{I2}	P60 to P62 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P23, P121, P122, P137, EXCLK, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3[Note 2]	V
Output voltage	V_{O1}	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P60 to P62, P70, P120, P147	−0.3 to V_{DD} +0.3 [Note 2]	V
	V_{O2}	P20 to P23	−0.3 to V_{DD} +0.3 [Note 2]	V
Analog input voltage	V_{AI1}	ANI16 to ANI19	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF}(+) +0.3[Notes 2, 3]	V
	V_{AI2}	ANI0 to ANI3	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF}(+) +0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

    2. Must be 6.5 V or lower.

    3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

    2. AV_{REF} (+) : + side reference voltage of the A/D converter.

    3. V_{SS} : Reference voltage

Absolute Maximum Ratings (T$_A$ = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	−40	mA
		Total of all pins −170 mA	P00, P01, P40, P120	−70	mA
			P10 to P17, P30, P31, P50, P51, P70, P147	−100	mA
	I$_{OH2}$	Per pin	P20 to P23	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I$_{OL1}$	Per pin	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P60 to P62, P70, P120, P147	40	mA
		Total of all pins 170 mA	P00, P01, P40, P120	70	mA
			P10 to P17, P30, P31, P50, P51, P60 to P62, P70, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P23	1	mA
		Total of all pins		4	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution　**Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark　Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

25.2 Oscillator Characteristics

25.2.1 X1 oscillator characteristics

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	MHz

Note   Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark   When using the X1 oscillator, refer to **5.4 System Clock Oscillator in the RL78/G13 User's Manual Hardware**.

25.2.2 On-chip oscillator characteristics

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Notes 1, 2]	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	−1.0		+1.0	%
			1.6 V ≤ V_{DD} < 1.8 V	−5.0		+5.0	%
		−40 to −20 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	−1.5		+1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	−5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1.   High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

    2.   This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

25.3 DC Characteristics

25.3.1 Pin characteristics

(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I$_{OH1}$	Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−10.0 [Note 2]	mA
		Total of P00, P01, P40, P120 (When duty ≤ 70% [Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			−28.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			−10.0	mA
			1.8 V ≤ V$_{DD}$ < 2.7 V			−5.0	mA
			1.6 V ≤ V$_{DD}$ < 1.8 V			−2.5	mA
		Total of P10 to P17, P30, P31, P50, P51, P70, P147 (When duty ≤ 70% [Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			−80.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			−19.0	mA
			1.8 V ≤ V$_{DD}$ < 2.7 V			−10.0	mA
			1.6 V ≤ V$_{DD}$ < 1.8 V			−5.0	mA
		Total of all pins (When duty ≤ 70% [Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−108.0	mA
	I$_{OH2}$	Per pin for P20 to P23	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−0.1 [Note 2]	mA
		Total of all pins (When duty ≤ 70% [Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V$_{DD}$ pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and I$_{OH}$ = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution   P00, P10 to P15, P17 and P50 do not output high level in N-ch open-drain mode.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = –40 to +85°C, 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147				20.0[Note 2]	mA
		Per pin for P60 to P62				15.0[Note 2]	mA
		Total of P00, P01, P40, P120 (When duty $\leq$ 70%[Note 3])	4.0 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			56.0	mA
			2.7 V $\leq$ V$_{DD}$ < 4.0 V			15.0	mA
			1.8 V $\leq$ V$_{DD}$ < 2.7 V			9.0	mA
			1.6 V $\leq$ V$_{DD}$ < 1.8 V			4.5	mA
		Total of P10 to P17, P30, P31, P50, P51, P60 to P62, P70, P147 (When duty $\leq$ 70%[Note 3])	4.0 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			80.0	mA
			2.7 V $\leq$ V$_{DD}$ < 4.0 V			35.0	mA
			1.8 V $\leq$ V$_{DD}$ < 2.7 V			20.0	mA
			1.6 V $\leq$ V$_{DD}$ < 1.8 V			10.0	mA
		Total of all pins (When duty $\leq$ 70%[Note 3])				136.0	mA
	I$_{OL2}$	Per pin for P20 to P23				0.4[Note 2]	mA
		Total of all pins (When duty $\leq$ 70%[Note 3])	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V$_{SS}$ pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq$ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and I$_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) $\cong$ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = –40 to +85°C, 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	Normal input buffer	0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P01, P10, P11, P13 to P17	TTL input buffer 4.0 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	2.2		V$_{DD}$	V
			TTL input buffer 3.3 V $\leq$ V$_{DD}$ < 4.0 V	2.0		V$_{DD}$	V
			TTL input buffer 1.6 V $\leq$ V$_{DD}$ < 3.3 V	1.5		V$_{DD}$	V
	V$_{IH3}$	P20 to P23		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60 to P62		0.7V$_{DD}$		6.0	V
	V$_{IH5}$	P121, P122, P137, EXCLK, $\overline{\text{RESET}}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	Normal input buffer	0		0.2V$_{DD}$	V
	V$_{IL2}$	P01, P10, P11, P13 to P17	TTL input buffer 4.0 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V $\leq$ V$_{DD}$< 4.0 V	0		0.5	V
			TTL input buffer 1.6 V $\leq$ V$_{DD}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P23		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60 to P62		0		0.3V$_{DD}$	V
	V$_{IL5}$	P121, P122, P137, EXCLK, $\overline{\text{RESET}}$		0		0.2V$_{DD}$	V

Caution   **The maximum value of V$_{IH}$ of P00, P10 to P15, P17 and P50 is V$_{DD}$, even in the N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OH1} = −10.0 mA	V_{DD} − 1.5			V
			4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OH1} = −3.0 mA	V_{DD} − 0.7			V
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OH1} = −2.0 mA	V_{DD} − 0.6			V
			1.8 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OH1} = −1.5 mA	V_{DD} − 0.5			V
			1.6 V $\leq$ V_{DD} < 5.5 V, I_{OH1} = −1.0 mA	V_{DD} − 0.5			V
	V_{OH2}	P20 to P23	1.6 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OH2} = −100 μA	V_{DD} − 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 20 mA			1.3	V
			4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V $\leq$ V_{DD} < 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P23	1.6 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P62	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V $\leq$ V_{DD} < 5.5 V, I_{OL3} = 1.0 mA			0.4	V

Caution　**P00, P10 to P15, P17 and P50 do not output high level in N-ch open-drain mode.**

Remark　Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (5/5)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P60 to P62, P70, P120, P147	V$_I$ = V$_{DD}$				1	μA
	I$_{LIH2}$	P20 to P23, P137, $\overline{RESET}$	V$_I$ = V$_{DD}$				1	μA
	I$_{LIH3}$	X1, X2, EXCLK	V$_I$ = V$_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I$_{LIL1}$	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P60 to P62, P70, P120, P147	V$_I$ = V$_{SS}$				−1	μA
	I$_{LIL2}$	P20 to P23, P137, $\overline{RESET}$	V$_I$ = V$_{SS}$				−1	μA
	I$_{LIL3}$	X1, X2, EXCLK	V$_I$ = V$_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pll-up resistance	R$_U$	P00, P01, P10 to P17, P30, P31, P40, P50, P51, P70, P120, P147	V$_I$ = V$_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

25.3.2 Supply current characteristics

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD1}$	Operating mode	HS (high-speed main) mode [Note 4]	f$_{IH}$ = 32 MHz [Note 3]	Basic operation	V$_{DD}$ = 5.0 V		2.1		mA
						V$_{DD}$ = 3.0 V		2.1		mA
					Normal operation	V$_{DD}$ = 5.0 V		4.6	7.0	mA
						V$_{DD}$ = 3.0 V		4.6	7.0	mA
				f$_{IH}$ = 24 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		3.7	5.5	mA
						V$_{DD}$ = 3.0 V		3.7	5.5	mA
				f$_{IH}$ = 16 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		2.7	4.0	mA
						V$_{DD}$ = 3.0 V		2.7	4.0	mA
			LS (low-speed main) mode [Note 4]	f$_{IH}$ = 8 MHz [Note 3]	Normal operation	V$_{DD}$ = 3.0 V		1.2	1.8	mA
						V$_{DD}$ = 2.0 V		1.2	1.8	mA
			LV (low-voltage main) mode [Note 4]	f$_{IH}$ = 4 MHz [Note 3]	Normal operation	V$_{DD}$ = 3.0 V		1.2	1.7	mA
						V$_{DD}$ = 2.0 V		1.2	1.7	mA
			HS (high-speed main) mode [Note 4]	f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
			LS (low-speed main) mode [Note 4]	f$_{MX}$ = 8 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				f$_{MX}$ = 8 MHz [Note 2], V$_{DD}$ = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA

Notes 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

    2. When high-speed on-chip oscillator is stopped.

    3. When high-speed system clock is stopped.

    4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

      HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

                                  2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

      LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 8 MHz

      LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

    2. f$_{IH}$: High-speed on-chip oscillator clock frequency

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 6]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.54	1.63	mA
					V$_{DD}$ = 3.0 V		0.54	1.63	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.28	mA
					V$_{DD}$ = 3.0 V		0.44	1.28	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.40	1.00	mA
					V$_{DD}$ = 3.0 V		0.40	1.00	mA
			LS (low-speed main) mode [Note 6]	f$_{IH}$ = 8 MHz [Note 4]	V$_{DD}$ = 3.0 V		260	530	μA
					V$_{DD}$ = 2.0 V		260	530	μA
			LV (low-voltage main) mode [Note 6]	f$_{IH}$ = 4 MHz [Note 4]	V$_{DD}$ = 3.0 V		420	640	μA
					V$_{DD}$ = 2.0 V		420	640	μA
			HS (high-speed main) mode [Note 6]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			LS (low-speed main) mode [Note 6]	f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
				f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
	I$_{DD3}$ [Note 5]	STOP mode	T$_A$ = −40°C				0.18	0.50	μA
			T$_A$ = +25°C				0.23	0.50	μA
			T$_A$ = +50°C				0.30	1.10	μA
			T$_A$ = +70°C				0.46	1.90	μA
			T$_A$ = +85°C				0.75	3.30	μA

Notes 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

　　　　2. During HALT instruction execution by flash memory.

　　　　3. When high-speed on-chip oscillator is stopped.

　　　　4. When high-speed system clock is stopped.

　　　　5. Not including the current flowing into 12-bit interval timer, and watchdog timer.

　　　　6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

　　　　　　HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

　　　　　　　　　　　　　　　　　　　2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

　　　　　　LS (low-speed main) mode:　1.8 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 8 MHz

　　　　　　LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

　　　　　2. f$_{IH}$: High-speed on-chip oscillator clock frequency

(1) Peripheral Functions

(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I$_{FIL}$[Note 1]				0.20		μA
12-bit interval timer operating current	I$_{IT}$[Notes 1, 2, 3]				0.02		μA
Watchdog timer operating current	I$_{WDT}$[Notes 1, 2, 4]	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$[Notes 1, 5]	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I$_{ADREF}$[Note 1]				75.0		μA
LVD operating current	I$_{LVD}$[Notes 1, 6]				0.08		μA
Self-programming operating current	I$_{FSP}$[Notes 1, 8]				2.50	12.20	mA
BGO operating current	I$_{BGO}$[Notes 1, 7]				2.50	12.20	mA
SNOOZE operating current	I$_{SNOZ}$[Note 1]	ADC operation	The mode is performed[Note 9]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V$_{DD}$.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer is in operation.

5 Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$ or I$_{DD2}$ and I$_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{LVD}$ when the LVD circuit is in operation.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode in the RL78/G13 User's Manual Hardware.**

Remarks 1. f$_{IL}$: Low-speed on-chip oscillator clock frequency

2. f$_{CLK}$: CPU/peripheral hardware clock frequency

3. Temperature condition of the TYP. value is T$_A$ = 25°C

25.4 AC Characteristics

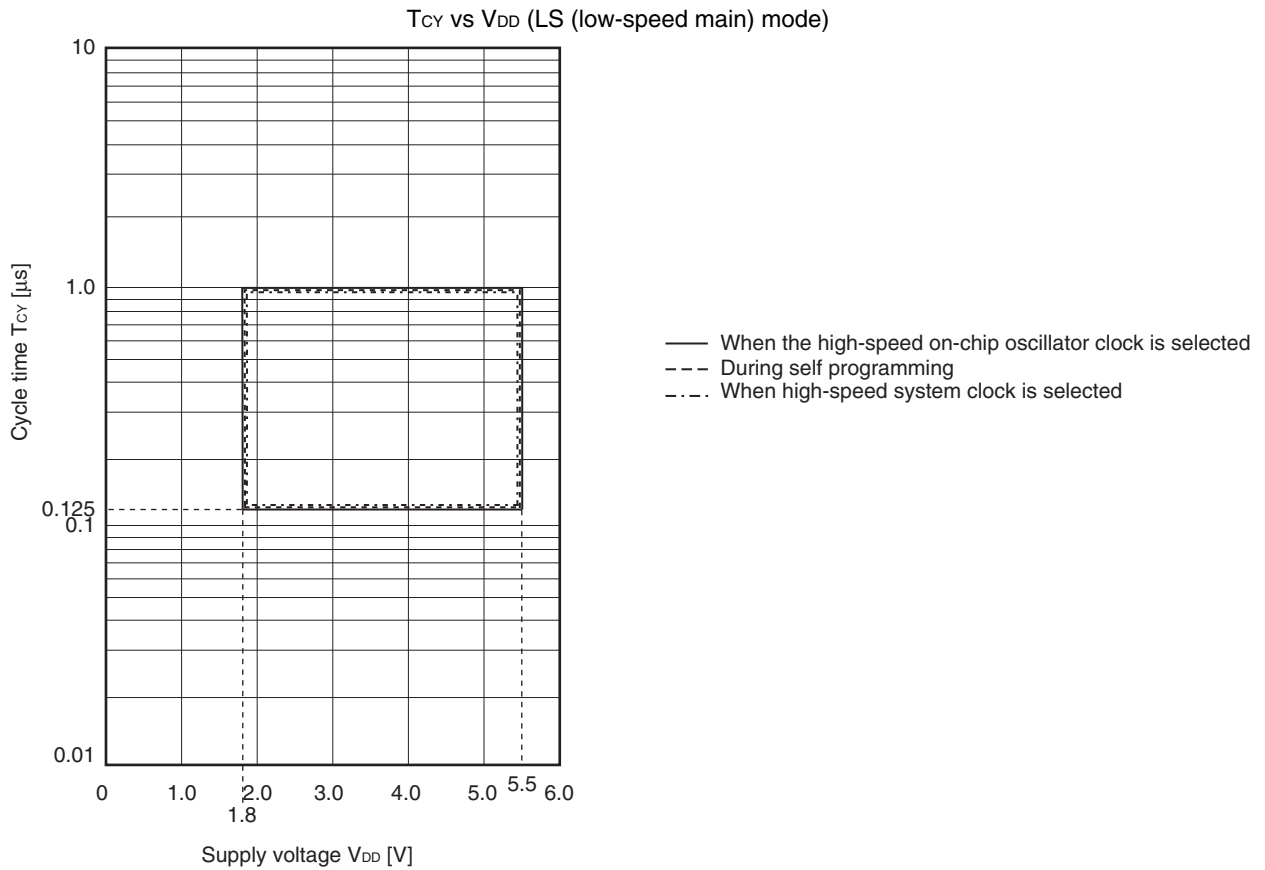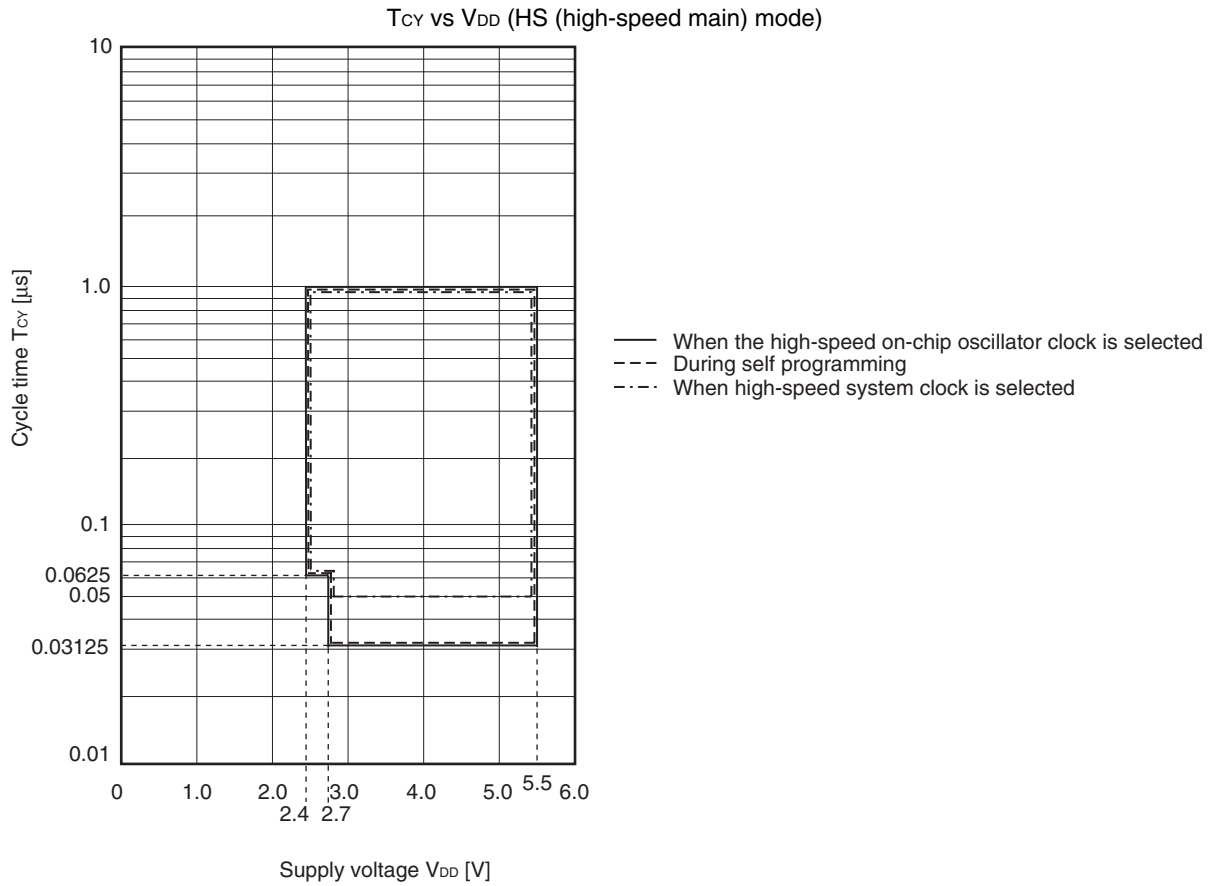**(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**

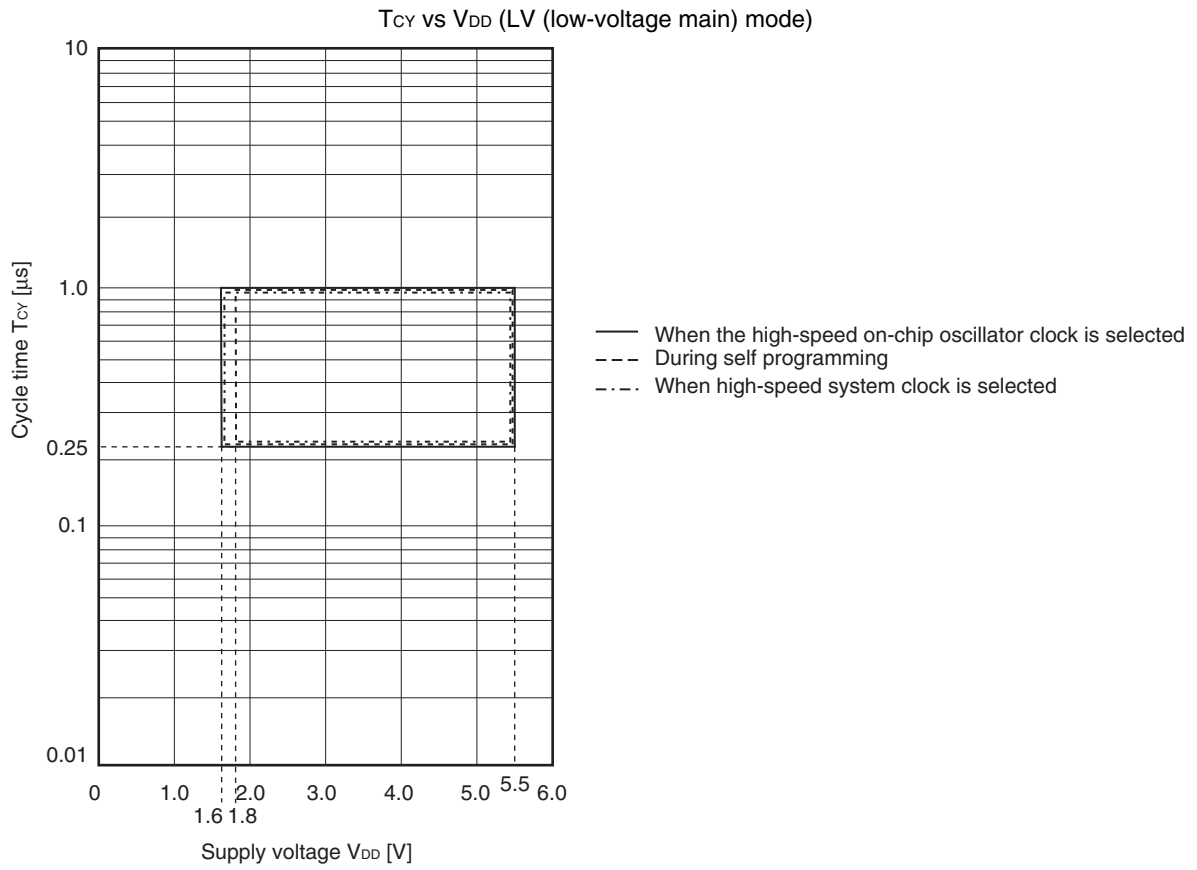| Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V$_{DD}$ ≤ 5.5 V	0.25		1	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.25		1	μs
External system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V$_{DD}$ < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V$_{DD}$ < 1.8 V			1.0		4.0	MHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
		1.8 V ≤ V$_{DD}$ < 2.4 V			60			ns
		1.6 V ≤ V$_{DD}$ < 1.8 V			120			ns
TI00 to TI07 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns
TO00 to TO07 output frequency	f$_{TO}$	HS (high-speed main) mode	4.0 V ≤ V$_{DD}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ V$_{DD}$ < 4.0 V				8	MHz
			1.8 V ≤ V$_{DD}$ < 2.7 V				4	MHz
			1.6 V ≤ V$_{DD}$ < 1.8 V				2	MHz
		LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V				4	MHz
			1.6 V ≤ V$_{DD}$ < 1.8 V				2	MHz
		LV (low-voltage main) mode	1.6 V ≤ V$_{DD}$ ≤ 5.5 V				2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode	4.0 V ≤ V$_{DD}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ V$_{DD}$ < 4.0 V				8	MHz
			1.8 V ≤ V$_{DD}$ < 2.7 V				4	MHz
			1.6 V ≤ V$_{DD}$ < 1.8 V				2	MHz
		LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V				4	MHz
			1.6 V ≤ V$_{DD}$ < 1.8 V				2	MHz
		LV (low-voltage main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V				4	MHz
			1.6 V ≤ V$_{DD}$ < 1.8 V				2	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0	1.6 V ≤ V$_{DD}$ ≤ 5.5 V		1			μs
		INTP1 to INTP5	1.6 V ≤ V$_{DD}$ ≤ 5.5 V		1			μs
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$				10			μs

Remark   f$_{MCK}$: Timer array unit operation clock frequency

       (Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
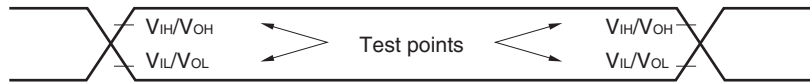
       m: Unit number (m = 0) n: Channel number (n = 0 to 7))

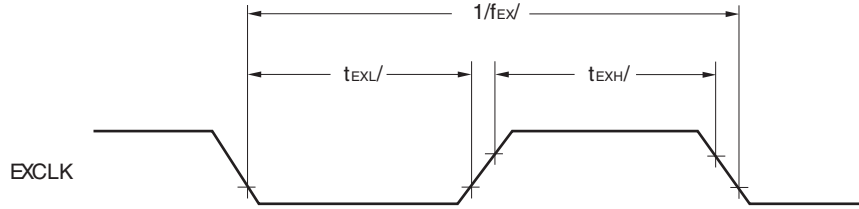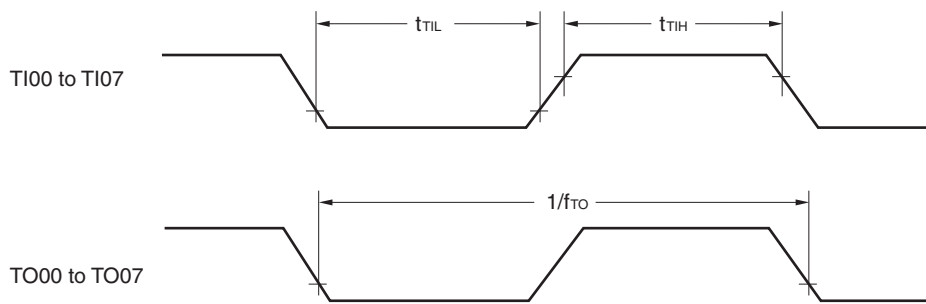**Minimum Instruction Execution Time during Main System Clock Operation**

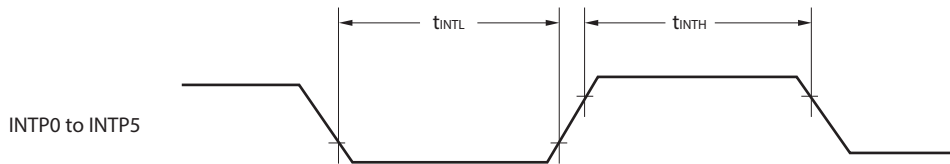T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)

When the high-speed on-chip oscillator clock is selected
During self programming
When high-speed system clock is selected

Supply voltage V$_{DD}$ [V]

T$_{CY}$ vs V$_{DD}$ (LS (low-speed main) mode)

When the high-speed on-chip oscillator clock is selected
During self programming
When high-speed system clock is selected

Supply voltage V$_{DD}$ [V]

T_{CY} vs V_{DD} (LV (low-voltage main) mode)

— When the high-speed on-chip oscillator clock is selected
--- During self programming
-·-· When high-speed system clock is selected

AC Timing Test Points

External System Clock Timing

TI/TO Timing

Interrupt Request Input Timing

$\overline{\text{RESET}}$ Input Timing
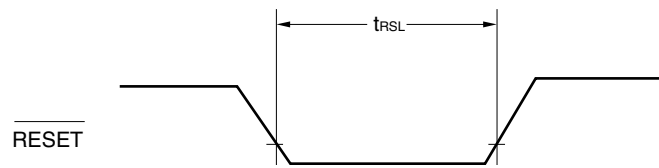
25.5 Peripheral Functions Characteristics

AC Timing Test Points
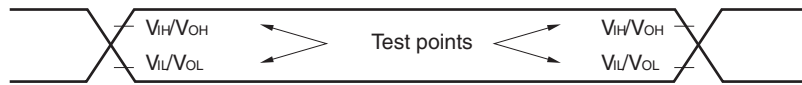
25.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T$_A$ = –40 to +85°C, 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate [Note 1]		2.4 V$\leq$ V$_{DD}$ $\leq$ 5.5 V			f$_{MCK}$/6		f$_{MCK}$/6		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 2]		5.3		1.3		0.6	Mbps
		1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			f$_{MCK}$/6		f$_{MCK}$/6		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 2]		5.3		1.3		0.6	Mbps
		1.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			f$_{MCK}$/6		f$_{MCK}$/6		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 2]		5.3		1.3		0.6	Mbps
		1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			—		f$_{MCK}$/6		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 2]		—		1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

  2. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

  HS (high-speed main) mode: 32 MHz (2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V)

                  16 MHz (2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V)

  LS (low-speed main) mode: 8 MHz (1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V)

  LV (low-voltage main) mode: 4 MHz (1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V)

Caution   Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)
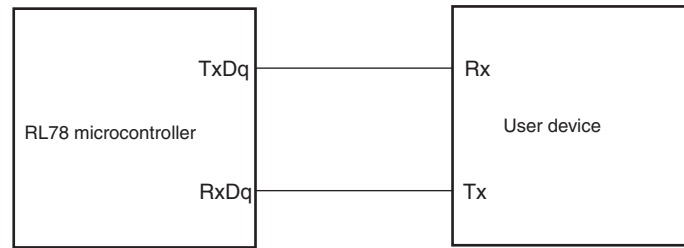
UART mode bit width (during communication at same potential) (reference)
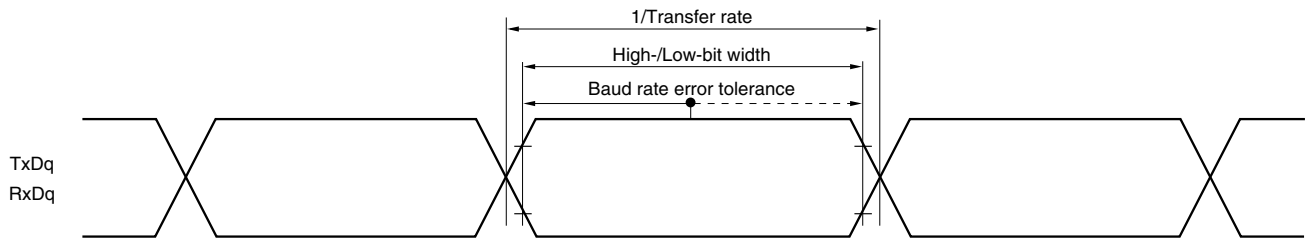
Remarks 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

    2. f_{MCK}: Serial array unit operation clock frequency

      (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

      n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	62.5		250		500		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		23		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		33		110		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4			10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remarks 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

    2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
         g: PIM and POM numbers (g = 1)

    3. f_{MCK}: Serial array unit operation clock frequency

    (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

    n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ =0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 4/f$_{CLK}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ V$_{DD}$ ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2 – 12		t$_{KCY1}$/2 – 50		t$_{KCY1}$/2 – 50		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2 – 18		t$_{KCY1}$/2 – 50		t$_{KCY1}$/2 – 50		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2 – 38		t$_{KCY1}$/2 – 50		t$_{KCY1}$/2 – 50		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2 – 50		t$_{KCY1}$/2 – 50		t$_{KCY1}$/2 – 50		ns
		1.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2 – 100		t$_{KCY1}$/2 – 100		t$_{KCY1}$/2 – 100		ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		t$_{KCY1}$/2 – 100		t$_{KCY1}$/2 – 100		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ V$_{DD}$ ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		220		220		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	1.7 V ≤ V$_{DD}$ ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	1.7 V ≤ V$_{DD}$ ≤ 5.5 V C = 30 pF Note 4			25		25		25	ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V C = 30 pF Note 4			—		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remarks 1. p: CSI number (p = 00, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1, 5)

2. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10, 11))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)
**(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t$_{KCY2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		ns
		1.7 V ≤ V$_{DD}$ ≤ 5.5 V		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		ns
		1.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)
(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) [Note 1]	t$_{SIK2}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$+20		1/f$_{MCK}$+30		1/f$_{MCK}$+30		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$+30		1/f$_{MCK}$+30		1/f$_{MCK}$+30		ns
		1.7 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$+40		1/f$_{MCK}$+40		1/f$_{MCK}$+40		ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		1/f$_{MCK}$+40		1/f$_{MCK}$+40		ns
Slp hold time (from SCKp↑) [Note 2]	t$_{KSI2}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$+31		1/f$_{MCK}$+31		1/f$_{MCK}$+31		ns
		1.7 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$+250		1/f$_{MCK}$+250		1/f$_{MCK}$+250		ns
		1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		1/f$_{MCK}$+250		1/f$_{MCK}$+250		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO2}$	C = 30 pF [Note 4]	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$+44		2/f$_{MCK}$+110		2/f$_{MCK}$+110	ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$+75		2/f$_{MCK}$+110		2/f$_{MCK}$+110	ns
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$+110		2/f$_{MCK}$+110		2/f$_{MCK}$+110	ns
			1.7 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$+220		2/f$_{MCK}$+220		2/f$_{MCK}$+220	ns
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V		—		2/f$_{MCK}$+220		2/f$_{MCK}$+220	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution   Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 11, 20), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 5)

2. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
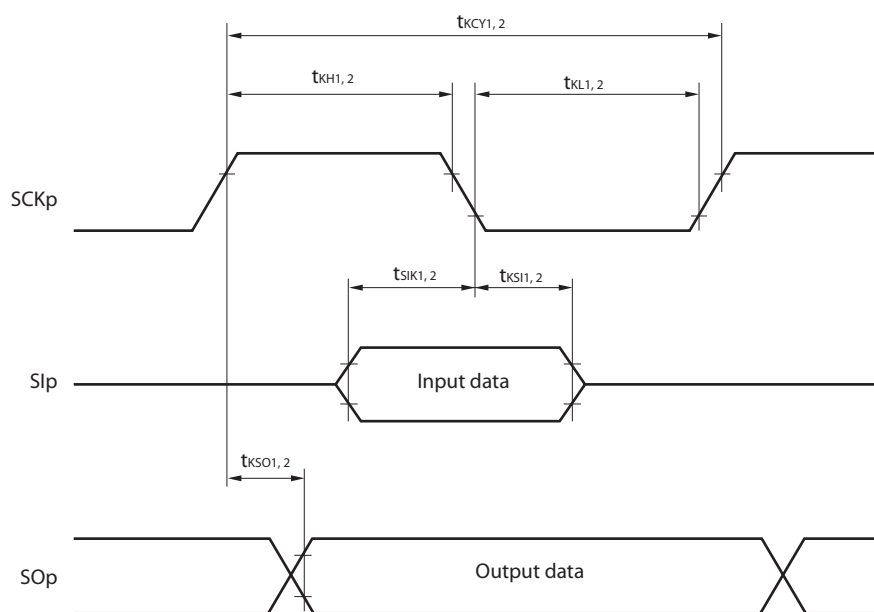
n: Channel number (mn = 00 to 03, 10, 11))

CSI mode connection diagram (during communication at same potential)
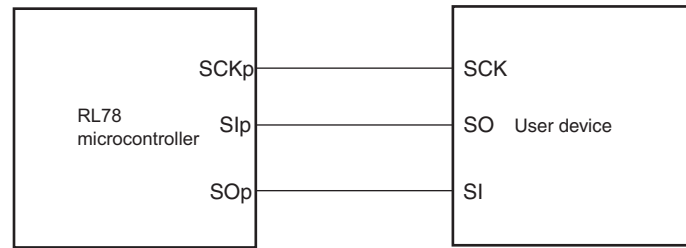
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
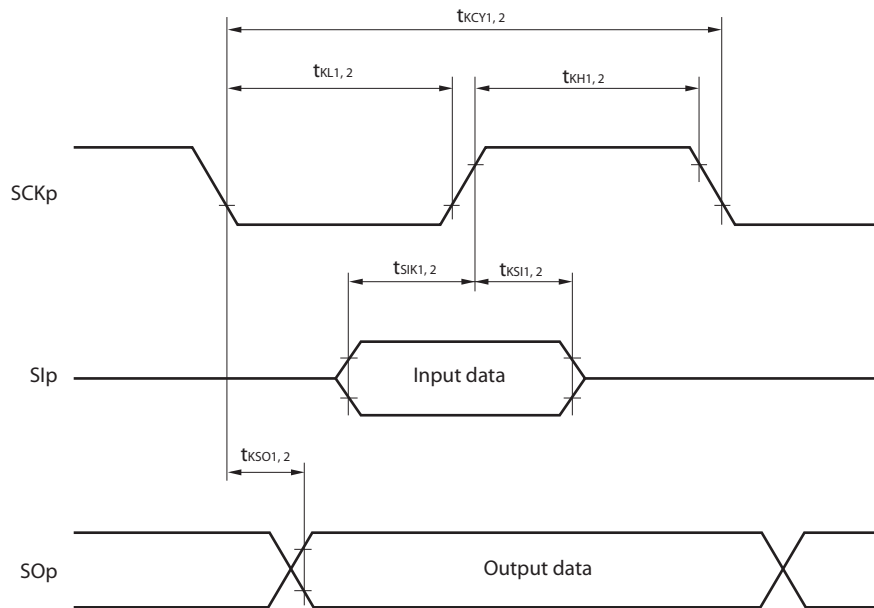
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks 1. p: CSI number (p = 00, 11, 20)

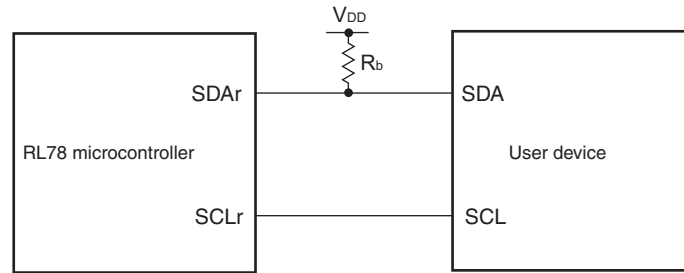   **2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) During communication at same potential (simplified I²C mode) (1/2)

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t$_{LOW}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t$_{HIGH}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		1850		1850		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)
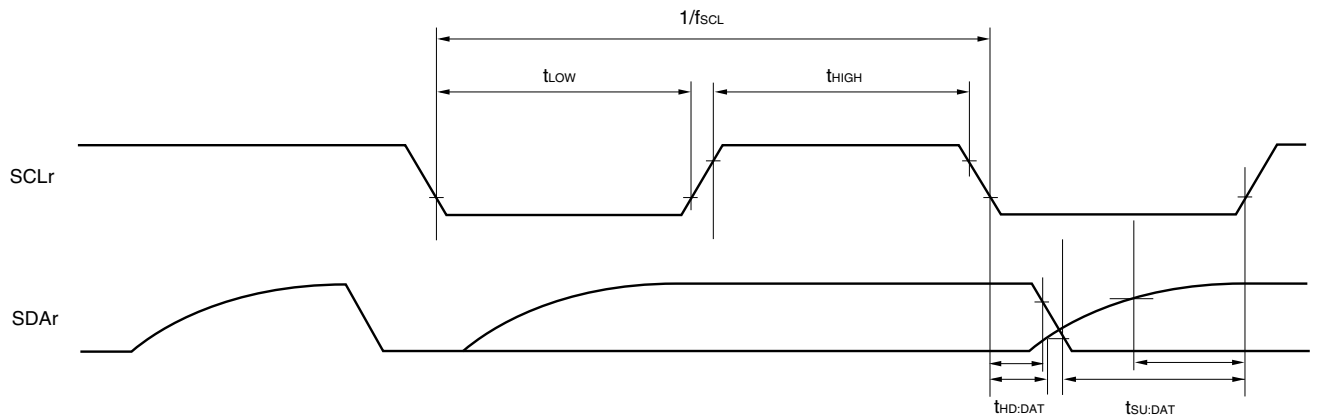
(5) During communication at same potential (simplified I^{2}C mode) (2/2)

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 85 Note2		1/f$_{MCK}$ + 145 Note2		1/f$_{MCK}$ + 145 Note2		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 145 Note2		1/f$_{MCK}$ + 145 Note2		1/f$_{MCK}$ + 145 Note2		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1/f$_{MCK}$ + 230 Note2		1/f$_{MCK}$ + 230 Note2		1/f$_{MCK}$ + 230 Note2		ns
		1.7 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1/f$_{MCK}$ + 290 Note2		1/f$_{MCK}$ + 290 Note2		1/f$_{MCK}$ + 290 Note2		ns
		1.6 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		1/f$_{MCK}$ + 290 Note2		1/f$_{MCK}$ + 290 Note2		ns
Data hold time (transmission)	t$_{HD:DAT}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ V$_{DD}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		0	405	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

   2. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

Simplified I^{2}C mode mode connection diagram (during communication at same potential)

Simplified I^{2}C mode serial transfer timing (during communication at same potential)

Remarks 1. R$_b$[Ω]:Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

    2. r: IIC number (r = 00, 11, 20), g: PIM number (g = 0, 1, 5),
        h: POM number (g = 0, 1, 5)

    3. f$_{MCK}$: Serial array unit operation clock frequency

    (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 3**		5.3		1.3		0.6	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 3**		5.3		1.3		0.6	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			$f_{MCK}/6$ **Notes 1, 2**		$f_{MCK}/6$ **Notes 1, 2**		$f_{MCK}/6$ **Notes 1, 2**	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 3**		5.3		1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

   2. Use it with $V_{DD} \geq V_b$.

   3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

   HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

   16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

   LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

   LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

   2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

   3. f_{MCK}: Serial array unit operation clock frequency

   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

   n: Channel number (mn = 00 to 03, 10, 11)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +85°C, 1.8 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V $\leq$ V_{DD} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V $\leq$ V_{DD} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V $\leq$ V_{DD} $\leq$ 5.5 V and 2.7 V $\leq$ V_b $\leq$ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ V$_{DD}$ < 4.0 V and 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$
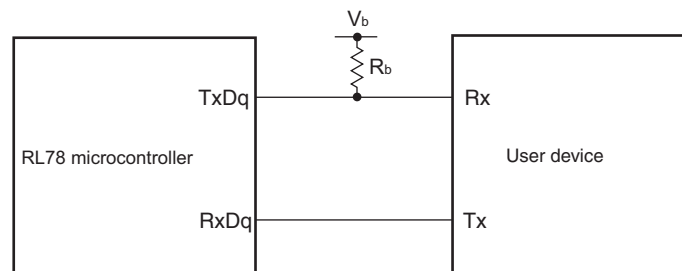
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$
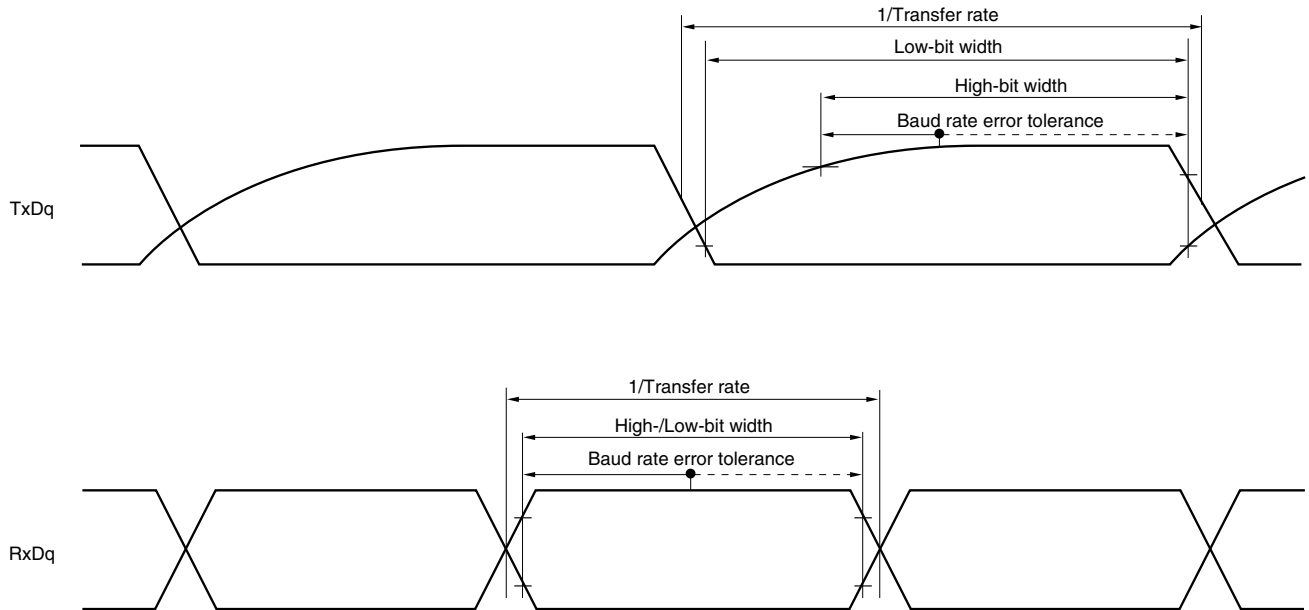
* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with V$_{DD}$ $\geq$ V$_b$.

6. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V $\leq$ V$_{DD}$ < 3.3 V and 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)

UART mode bit width (during communication at different potential) (reference)

TxDq

```
1/Transfer rate
Low-bit width
High-bit width
Baud rate error tolerance
```

RxDq

```
1/Transfer rate
High-/Low-bit width
Baud rate error tolerance
```

Remarks 1. R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		1150		1150		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ − 120		$t_{KCY1}/2$ − 120		$t_{KCY1}/2$ − 120		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ − 7		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ − 10		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		ns
SIp setup time (to SCKp↑) [Note 1]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output [Note 1]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns

(**Notes, Caution,** and **Remarks** are listed on the next page.)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)

(T$_A$ = −40 to +85°C, 2.7 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 2	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	23		110		110		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	33		110		110		ns
SIp hold time (from SCKp↓) Note 2	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
     2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution   Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

Remarks 1. R$_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage
     2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)
     3. f$_{MCK}$: Serial array unit operation clock frequency
      (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
     4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 4/f$_{CLK}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t$_{KH1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 75		t$_{KCY1}$/2 − 75		t$_{KCY1}$/2 − 75		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 170		t$_{KCY1}$/2 − 170		t$_{KCY1}$/2 − 170		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		t$_{KCY1}$/2 − 458		t$_{KCY1}$/2 − 458		t$_{KCY1}$/2 − 458		ns
SCKp low-level width	t$_{KL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 12		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 18		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns

Note   Use it with V$_{DD}$ ≥ V$_b$.

Caution   Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

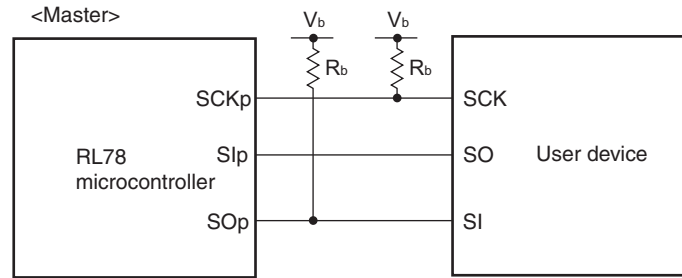**(Remarks** are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) [Note 1]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output [Note 1]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

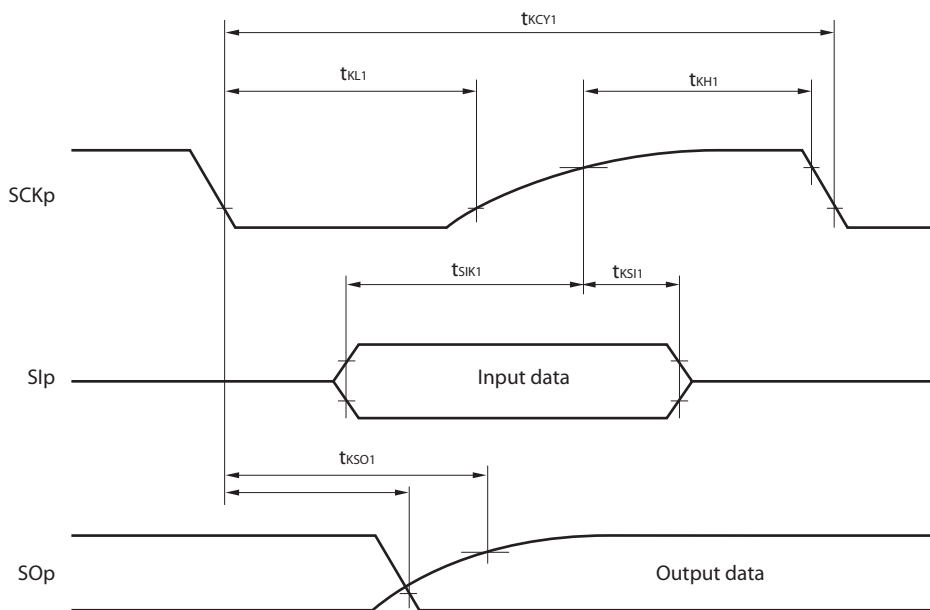   **2.** Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) [Note 1]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) [Note 1]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output [Note 1]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

Notes   **1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

           2. Use it with V_{DD} ≥ V_b.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**
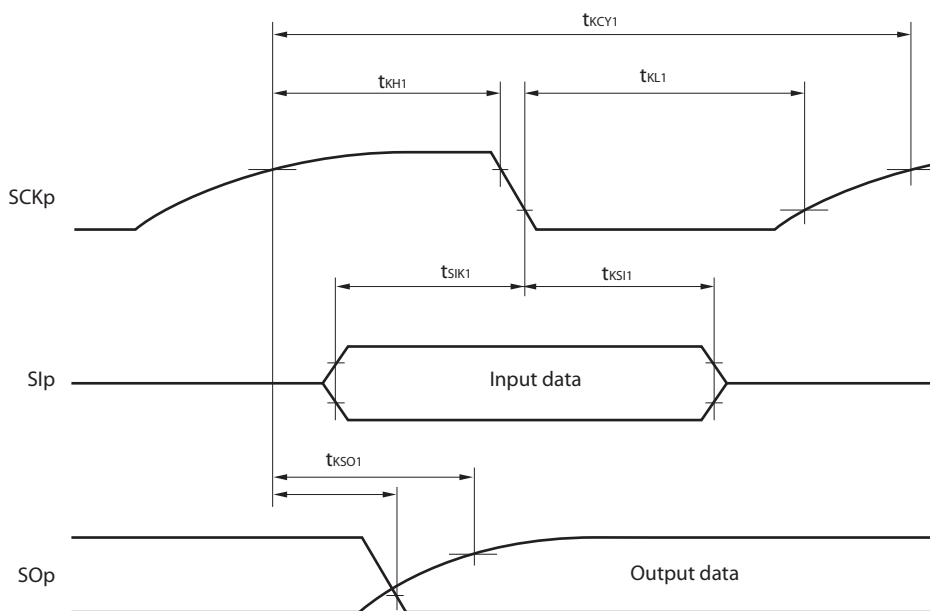
(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

Remarks **1.** R$_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number , n: Channel number (mn = 00, 10), g: PIM and POM number (g = 1)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 10))

4. CSI11 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks 1. p: CSI number (p = 00, 20), m: Unit number , n: Channel number (mn = 00, 10), g: PIM and POM number (g = 1)

2. CSI11 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V)　(CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	14/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	12/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	10/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	20/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	16/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	14/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	24 MHz < f$_{MCK}$	48/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	36/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	32/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	26/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	10/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	t$_{KCY2}$/2 − 12		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
SIp setup time (to SCKp↑) [Note 3]	t$_{SIK2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
SIp hold time (from SCKp↑) [Note 4]	t$_{KSI2}$		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
Delay time from SCKp↓ to SOp output [Note 5]	t$_{KSO2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		2/f$_{MCK}$ + 120		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		2/f$_{MCK}$ + 214		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573	ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

    2. Use it with V$_{DD}$ ≥ V$_b$.

    3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
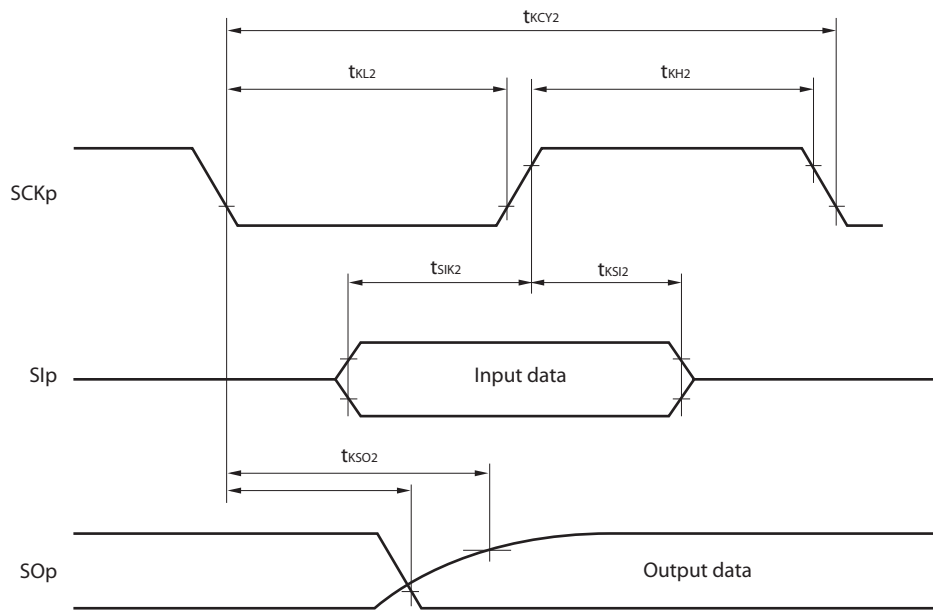
Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**
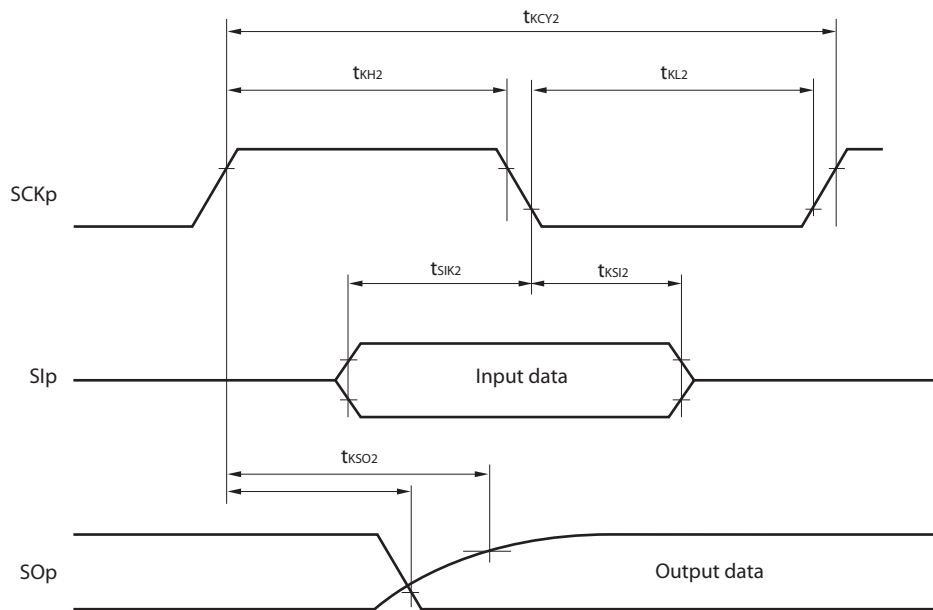
(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)
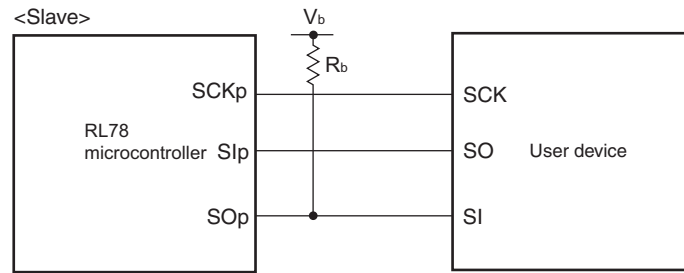
Remarks **1.** R$_b$[Ω]:Communication line (SOp) pull-up resistance, C$_b$[F]: Communication line (SOp) load capacitance, V$_b$[V]: Communication line voltage

     2. p: CSI number (p = 00, 20), m: Unit number, n: Channel number (mn = 00, 10), g: PIM and POM number (g = 1)

     3. f$_{MCK}$: Serial array unit operation clock frequency

     (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

     m: Unit number, n: Channel number (mn = 00, 10))

    4. CSI11 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks 1. p: CSI number (p = 00, 20), m: Unit number,

n: Channel number (mn = 00, 10), g: PIM and POM number (g = 1)

2. CSI11 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

| Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		400 Note 1		300 Note 1		300 ote 1	kHz
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	610		610		610		ns

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (2/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V **Note 2**, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
Data hold time (transmission)	t$_{HD:DAT}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V **Note 2**, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1.　The value must also be equal to or less than f$_{MCK}$/4.

　　　 2.　Use it with V$_{DD}$ ≥ V$_b$.

　　　 3.　Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution　Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I^{2}C mode connection diagram (during communication at different potential)
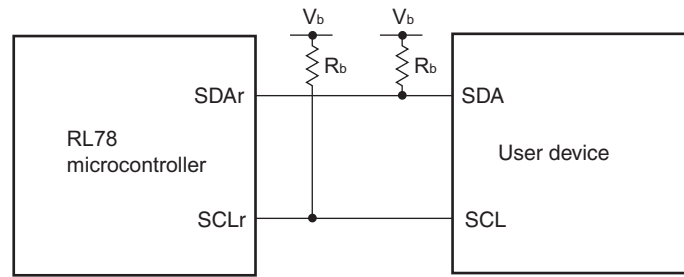
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
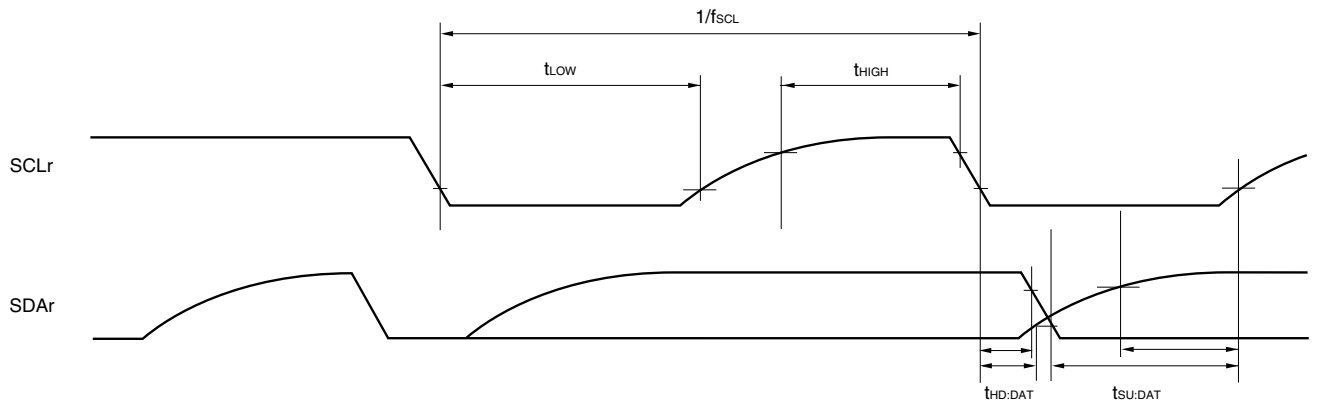
Remarks 1. R$_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

2. r: IIC number (r = 00, 20), g: PIM, POM number (g = 1)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00, 10)

25.6 Analog Characteristics

25.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI3	Refer to **25.6.1 (1)**.	Refer to **25.6.1 (3)**.	Refer to **25.6.1 (4)**.
ANI16 to ANI19	Refer to **25.6.1 (2)**.		
Internal reference voltage	Refer to **25.6.1 (1)**.		−

(1) When reference voltage (+)= AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2, ANI3, internal reference voltage

(T$_A$ = −40 to +85°C, 1.6 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]		1.2	±7.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±0.50	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±0.50	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±5.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI2, ANI3		0		AV$_{REFP}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$[Note 5]		V

(**Notes** are listed on the next page.)

Notes 1. Excludes quantization error ($\pm$1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.

Overall error: Add $\pm$1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Zero-scale error/Full-scale error: Add $\pm$0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Integral linearity error/ Differential linearity error: Add $\pm$0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

5. Refer to **25.6.2 Internal reference voltage characteristics**.

(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), target pin : ANI16 to ANI19

(TA = –40 to +85°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP,

Reference voltage (–) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution VDD = AVREFP = VDD [Notes 3, 4]	1.8 V ≤ AVREFP ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V [Note 5]		1.2	±8.5	LSB
Conversion time	tCONV	10-bit resolution Target ANI pin : ANI16 to ANI19	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ VDD ≤ 5.5 V	17		39	μs
			1.6 V ≤ VDD ≤ 5.5 V	57		95	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution VDD = AVREFP = VDD [Notes 3, 4]	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V [Note 5]			±0.60	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution VDD = AVREFP = VDD [Notes 3, 4]	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V [Note 5]			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution VDD = AVREFP = VDD [Notes 3, 4]	1.8 V ≤ AVREFP ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V [Note 5]			±6.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution VDD = AVREFP = VDD [Notes 3, 4]	1.8 V ≤ AVREFP ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V [Note 5]			±2.5	LSB
Analog input voltage	VAIN	ANI16 to ANI19		0		AVREFP and VDD	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

4. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.

5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V$_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI3, ANI16 to ANI19, internal reference voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (–) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]		1.2	±10.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI19	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
Conversion time	t$_{CONV}$	10-bit resolution Target pin: Internal reference voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±6.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±2.5	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI3		0		V$_{DD}$	V
		ANI16 to ANI19		0		V$_{DD}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{BGR}$ [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to **25.6.2 Internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2, ANI3, ANI16 to ANI19

(T$_A$ = –40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ =0 V, Reference voltage (+) = V$_{BGR}$[Note 3], Reference voltage (–) = AV$_{REFM}$ = 0 V[Note 4], HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$[Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

    2. This value is indicated as a ratio (%FSR) to the full-scale value.

    3. Refer to **25.6.2 Internal reference voltage characteristics**.

    4. When reference voltage (–) = V$_{SS}$, the MAX. values are as follows.

     Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV$_{REFM}$.

     Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

     Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

25.6.2 Internal reference voltage characteristics

(T$_A$ = –40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Operation stabilization wait time	t$_{AMP}$		5			μs

25.6.3 POR circuit characteristics

(T$_A$ = –40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.47	1.51	1.55	V
	V$_{PDR}$	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width**Note**	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time
required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is
entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock
operation status control register (CSC).
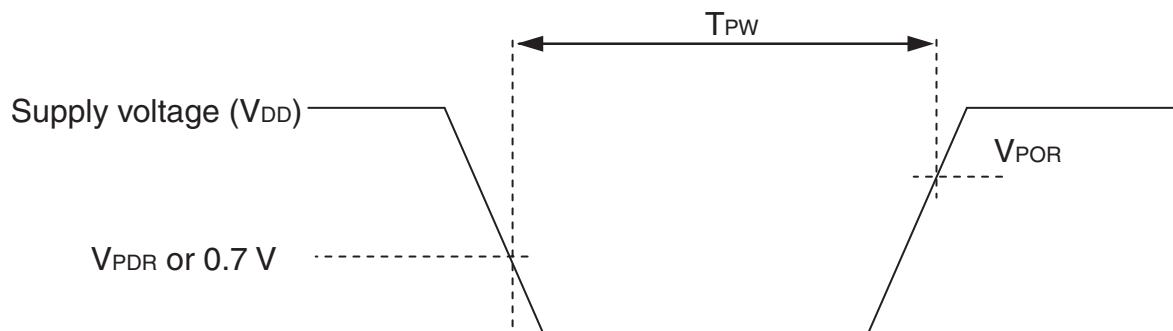
25.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T$_A$ = –40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V$_{LVD0}$	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V$_{LVD1}$	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V$_{LVD2}$	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V$_{LVD3}$	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V$_{LVD4}$	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V$_{LVD5}$	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V$_{LVD6}$	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V$_{LVD7}$	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V$_{LVD8}$	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V$_{LVD9}$	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V$_{LVD10}$	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V$_{LVD11}$	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V$_{LVD12}$	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V$_{LVD13}$	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t$_{LW}$		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T$_A$ = –40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V$_{LVDA0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V$_{LVDA1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		1.74	1.77	1.81	V
			Falling interrupt voltage		1.70	1.73	1.77	V
	V$_{LVDA2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		1.84	1.88	1.91	V
			Falling interrupt voltage		1.80	1.84	1.87	V
	V$_{LVDA3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		2.86	2.92	2.97	V
			Falling interrupt voltage		2.80	2.86	2.91	V
	V$_{LVDB0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V$_{LVDB1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		1.94	1.98	2.02	V
			Falling interrupt voltage		1.90	1.94	1.98	V
	V$_{LVDB2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		2.05	2.09	2.13	V
			Falling interrupt voltage		2.00	2.04	2.08	V
	V$_{LVDB3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		3.07	3.13	3.19	V
			Falling interrupt voltage		3.00	3.06	3.12	V
	V$_{LVDC0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V$_{LVDC1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		2.56	2.61	2.66	V
			Falling interrupt voltage		2.50	2.55	2.60	V
	V$_{LVDC2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		2.66	2.71	2.76	V
			Falling interrupt voltage		2.60	2.65	2.70	V
	V$_{LVDC3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		3.68	3.75	3.82	V
			Falling interrupt voltage		3.60	3.67	3.74	V
	V$_{LVDD0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V$_{LVDD1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		2.86	2.92	2.97	V
			Falling interrupt voltage		2.80	2.86	2.91	V
	V$_{LVDD2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		2.96	3.02	3.08	V
			Falling interrupt voltage		2.90	2.96	3.02	V
	V$_{LVDD3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		3.98	4.06	4.14	V
			Falling interrupt voltage		3.90	3.98	4.06	V

25.6.5 Power supply voltage rising slope characteristics

(T$_A$ = –40 to +85°C, V$_{SS}$ = 0 V)

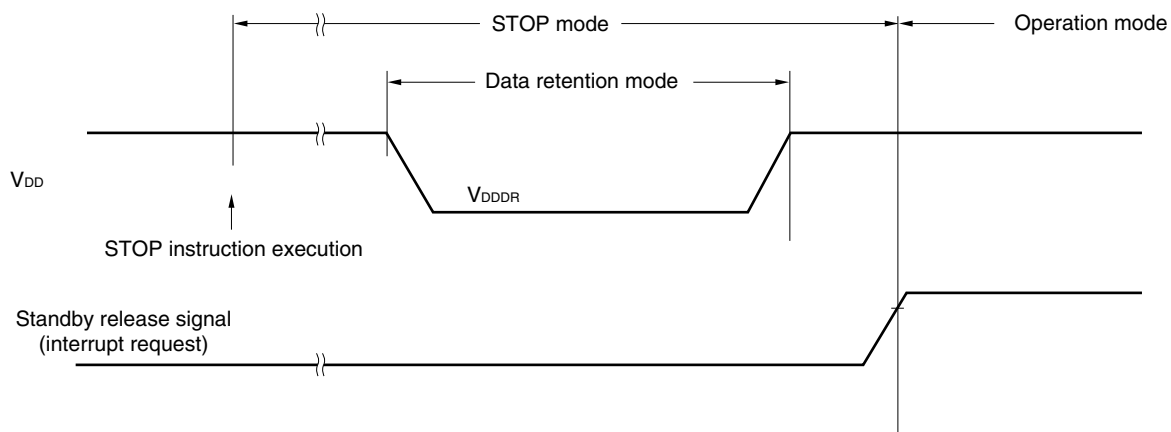| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S$_{VDD}$				54	V/ms

Caution   Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 25.4 AC Characteristics.

25.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T$_A$ = –40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.46[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.

25.8 Flash Memory Programming Characteristics

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f$_{CLK}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V		1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C$_{erwr}$	Retained for 20 years	T$_A$ = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years	T$_A$ = 25°C		1,000,000		
		Retained for 5 years	T$_A$ = 85°C	100,000			
		Retained for 20 years	T$_A$ = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

   The retaining years are until next rewrite after the rewrite.

   2. When using flash memory programmer and Renesas Electronics self programming library

   3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 25.9 Dedicated Flash Memory Programmer Communication (UART)

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

25.10 Timing Specs for Switching Flash Memory Programming Modes
(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must be released before the external reset is released.	1			ms
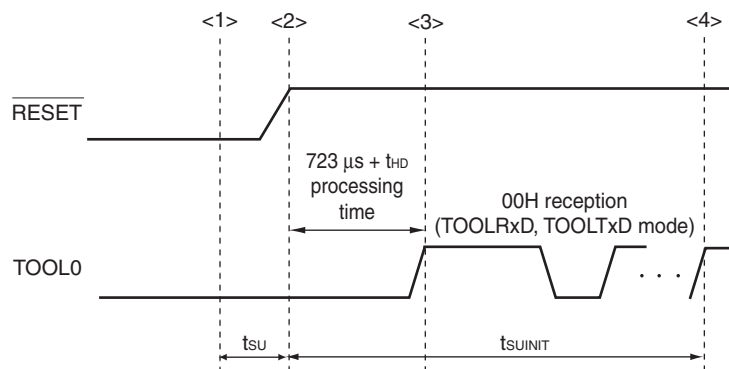
<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t$_{SU}$:   Time to release the external reset after the TOOL0 pin is set to the low level

t$_{HD}$:   Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

26. PACKAGE DRAWINGS

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN32-5x5-0.50	PWQN0032KD-A	————	0.06g

Index area

Detail F
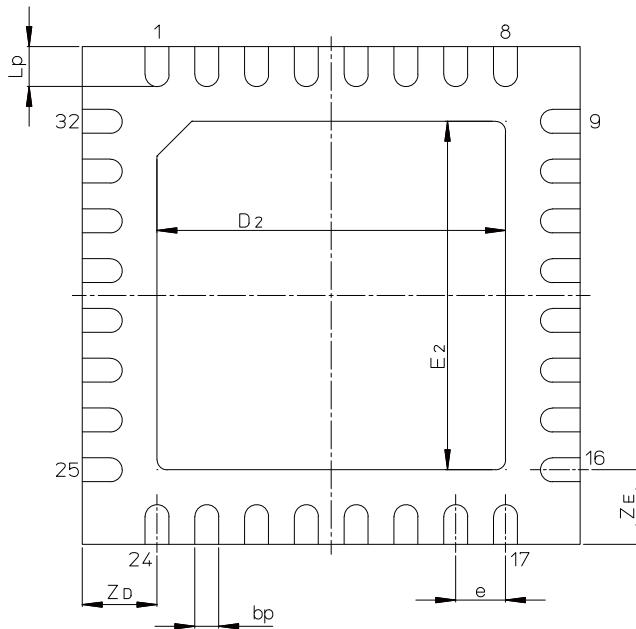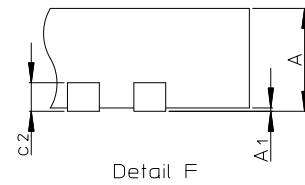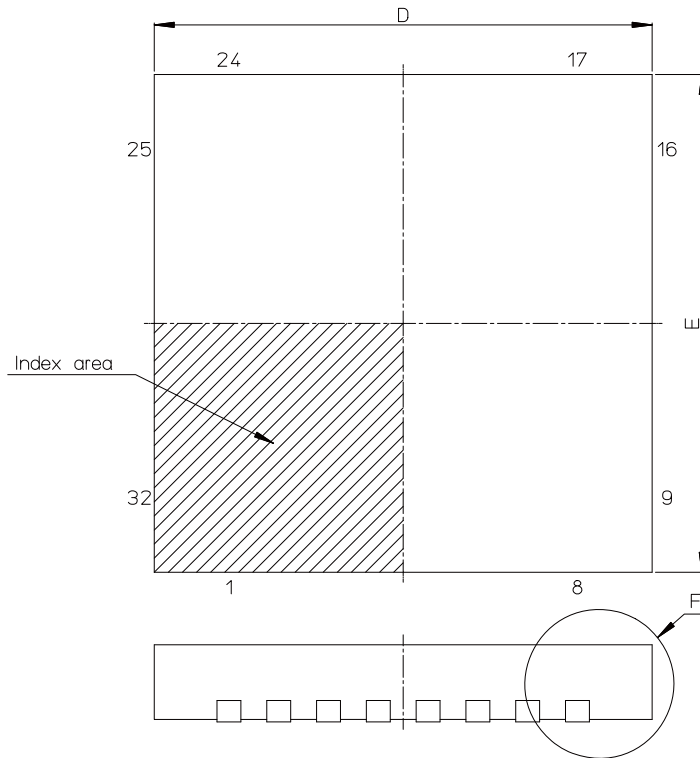
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	——	5.1
E	4.9	——	5.1
A	——	——	0.8
A1	0	——	——
bp	0.18	——	0.30
c2	0.18	——	0.25
e	——	0.5	——
Lp	0.35	——	0.45
ZD	——	0.75	——
ZE	——	0.75	——
D2	3.4	——	3.6
E2	3.4	——	3.6

Rev.	Date	Description	
		Page	**Summary**
1.00	Jun 24, 2014	-	First Edition issued

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction.   If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction.   Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction.   If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction.   CMOS devices behave differently than Bipolar or NMOS devices.   Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry.   Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin.   All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation.   Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate.   When it is dry, a humidifier should be used.   It is recommended to avoid using insulators that easily build up static electricity.   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material.   All test and measurement tools including work benches and floors should be grounded.   The operator should be grounded using a wrist strap.   Semiconductor devices must not be touched with bare hands.   Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device.   Immediately after the power source is turned ON, devices with reset functions have not yet been initialized.   Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers.   A device is not initialized until the reset signal is received.   A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply.   When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply.   Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.   The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE :   Do not input signals or an I/O pull-up power supply while the device is not powered.   The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.   Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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