SLAS319 – MAY 2001

CCD SIGNAL PROCESSOR FOR DIGITAL CAMERAS

FEATURES

- **CCD Signal Processing**
  - **Correlated Double Sampling (CDS)**
  - **Programmable Black Level Clamping**
- **Programmable Gain Amplifier (PGA)**
  - **–6-dB to 42-dB Gain Ranging**
- **10-Bit Digital Data Output**
  - **Up to 36-MHz Conversion Rate**
  - **No Missing Codes**
- **76-dB Signal-to-Noise Ratio**
- **Portable Operation**
  - **Low Voltage: 2.7 V to 3.6 V**
  - **Low Power: 120 mW (typ) at 3.0 V**
  - **Standby Mode: 6 mW**

DESCRIPTION

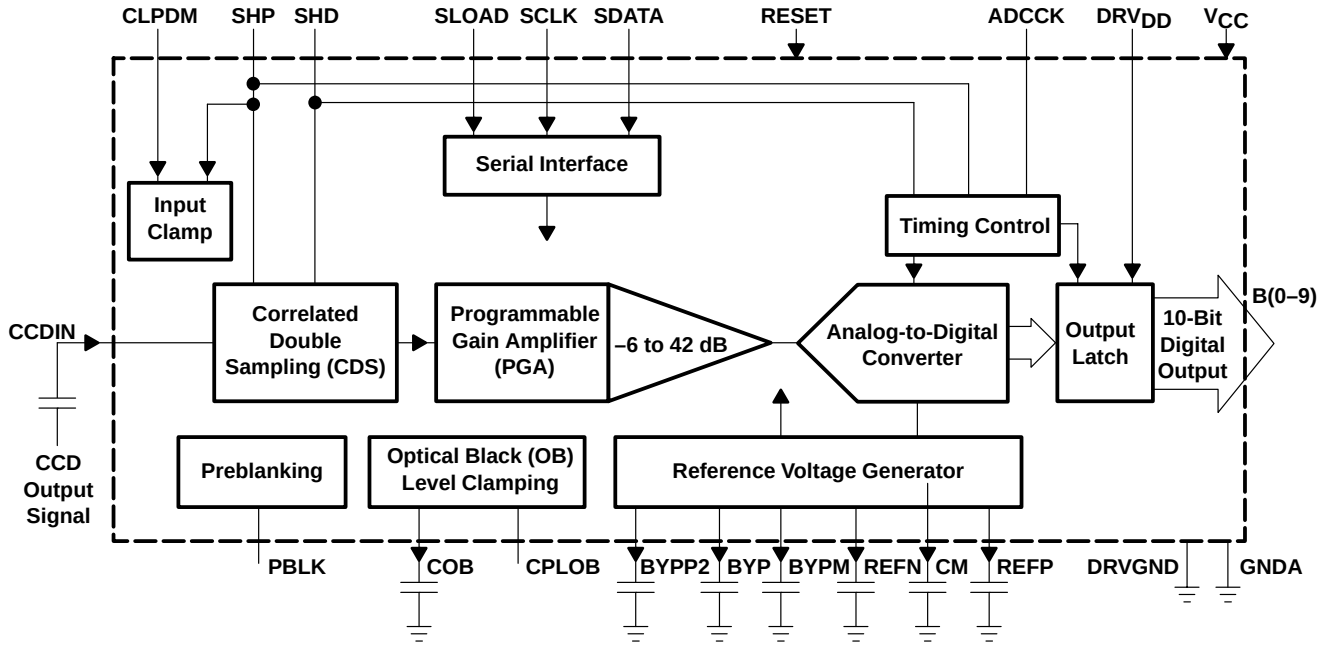
The VSP2230 is a complete mixed-signal processing IC for digital cameras that provides signal conditioning and analog-to-digital conversion for the output of a CCD array. The primary CCD channel provides correlated double sampling (CDS) to extract the video information from the pixels, a –6-dB to 42-dB gain with digital control for varying illumination conditions, and black level clamping for an accurate black level reference.

Input signal clamping and offset correction of the input CDS is also performed. The stable gain control is linear in dB. Additionally, the black level is quickly recovered after gain change.

The VSP2230Y is pin-to-pin compatible with the VSP2260Y (10 bit, 20 MHz) one-chip product.

The VSP2230Y is available in a 48-pin LQFP package and operates from a single 3-V/3.3-V supply.

VSP2230 block diagram



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PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE OUTLINE NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER†	TRANSPORT MEDIA
VSP2230Y	48-pin LQFP	ZZ340	0°C to 85°C	VSP2230Y	VSP2230Y	250 pcs. Tray
VSP2230Y	48-pin LQFP	ZZ340	0°C to 85°C	VSP2230Y	VSP2230Y/2K	Tape and Reel

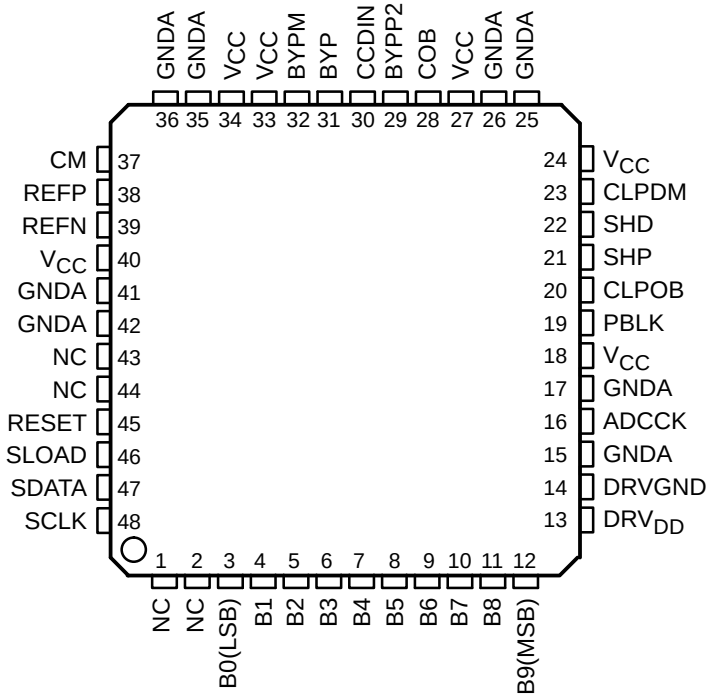
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., VSP2230CDR).

DEMO BOARD ORDERING INFORMATION

PRODUCT	ORDERING NUMBER
VSP2230Y	DEM-VSP2230Y

pin assignments

48-PIN LQFP PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
ADCCK	16	DI	Master clock, See Note 1
B0(LSB)	3	DO	A/D converter output, Bit 0 (LSB)
B1	4	DO	A/D converter output, Bit 1
B2	5	DO	A/D converter output, Bit 2
B3	6	DO	A/D converter output, Bit 3
B4	7	DO	A/D converter output, Bit 4
B5	8	DO	A/D converter output, Bit 5
B6	9	DO	A/D converter output, Bit 6
B7	10	DO	A/D converter output, Bit 7
B8	11	DO	A/D converter output, Bit 8
B9(MSB)	12	DO	A/D converter output, Bit 9 (MSB)
BYP	31	AO	Internal reference C (bypass to ground), See Note 2
BYPM	32	AO	Internal reference N (bypass to ground), See Note 3
BYPP2	29	AO	Internal reference P (bypass to ground), See Note 3
CCDIN	30	AI	CCD signal input
CLPDM	23	DI	Dummy pixel clamp pulse (Default = Active Low), See Note 4
CLPOB	20	DI	Optical black clamp pulse (Default = Active Low), See Note 4
CM	37	AO	A/D converter common mode voltage (bypass to ground), See Note 2
COB	28	AO	Optical black clamp loop reference (bypass to ground), See Note 5
DRV_{DD}	13	P	Power supply. Exclusively for digital output
DRVGND	14	P	Digital ground. Exclusively for digital output
GNDA	15, 17, 25, 26, 35, 36, 41, 42	P	Analog ground
NC	1, 2, 43, 44		Should be left open
PBLK	19	DI	Preblanking High = Normal operation mode Low = Preblanking mode: digital output all zero
REFN	39	AO	A/D converter negative reference (bypass to ground), See Note 2
REFP	38	AO	A/D converter positive reference (bypass to ground), See Note 2
RESET	45	DI	Asynchronous system reset (active low)
SCLK	48	DI	Clock for serial data shift (triggered at the rising edge)
SDATA	47	DI	Serial data input
SHP	21	DI	CDS reference level sampling pulse (Default = Active Low), See Note 4
SHD	22	DI	CDS Data level sampling pulse (Default = Active Low), See Note 4
SLOAD	46	DI	Serial data latch signal (triggered at the rising edge)
V_{CC}	18, 24, 27, 33, 34, 40	P	Analog power supply

† Designators in TYPE: P: power supply and ground, DI: digital input, DO: digital output, AI: analog input, AO: analog output

NOTES:
1. There are two options to drive the A/D converter:
   a). External drive mode. The master clock (ADCCK) drives A/D converter directly.
   b). Internal drive mode. The clock internally generated by on-chip timing control circuit using SHP and SHD signals drives A/D converter.
2. BYP, CM, REFN, and REFP should be connected to ground using a bypass capacitor (0.1 μF). Refer to v*oltage reference* for details.
3. BYPM, BYPP2 should be connected to ground using a bypass capacitor with a recommend value of 200 pF to 600 pF. However, this depends on the application environment. Refer to *voltage reference* for details.
4. Refer to *serial interface* for details.
5. COB should be connected to ground using a bypass capacitor with a recommend value of 0.1 μF to 0.22 μF. However, this depends on the application environment. Refer to *optical black level clamp loop* for details.

detailed description

introduction

The VSP2230 is a complete mixed-signal IC that contains all of the key features associated with the processing of the CCD imager output signal in a video camera, a digital still camera, a security camera, or similar applications. A simplified block diagram is shown on the front page of this data sheet. The VSP2230 includes a correlated double sampler (CDS), a programmable gain amplifier (PGA), an analog-to-digital converter (ADC), an input clamp, an optical black (OB) level clamp loop, a serial interface, a timing control, and a reference voltage generator. We recommend an off-chip emitter follower buffer between the CCD output and the VSP2230 CCDIN input. The PGA gain control, the clock polarity setting, and the operation mode choosing can be made through the serial interface. All parameters are reset to the default value when the RESET pin goes to low asynchronously from the clocks.

correlated double sampler (CDS)

The output signal of a CCD imager is sampled twice during one pixel period, one at the reference interval and the other at the data interval.

Subtracting these two samples, extracts the video information of the pixel as well as removes any noise that is common—or correlated—to both the intervals.

Thus, a CDS is very important to reduce the reset noise and the low frequency noises that are present on the CCD output signal. Figure 1 shows the simplified block diagram of the CDS and input clamp.

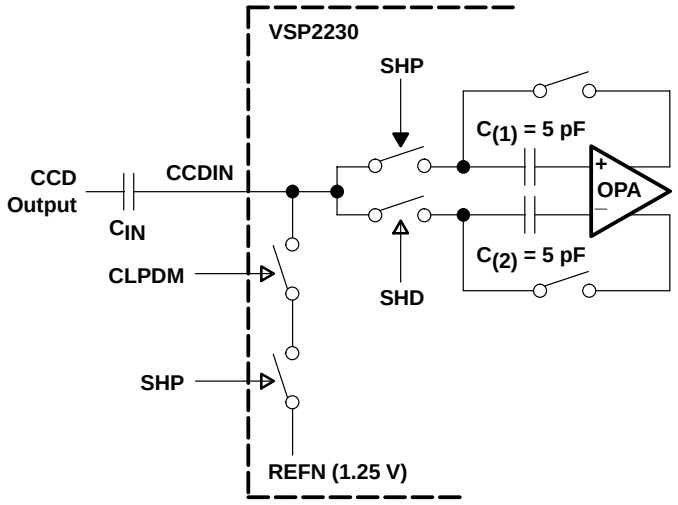


Figure 1. Simplified Block Diagram of the CDS and Input Clamp

The CDS is driven through an off-chip coupling capacitor (C_{IN}). AC coupling is strongly recommended because the DC level of the CCD output signal is usually too high (several volts) for the CDS to work properly. A 0.1-µF capacitor is recommended for C_{IN}, however, it depends on the application environment.

Also, an off-chip emitter follower buffer is recommended that can drive more than 10 pF, because the 5 pF of the sampling capacitor and a few pF of stray capacitance can be seen at the input pin. The analog input signal range at the CCDIN pin is 1 $V_{P–P}$, and the appropriate common mode voltage for the CDS is around 0.5 V to 1.5 V.

The reference level is sampled during SHP active period, and the voltage level is held on the sampling capacitor $C_{(1)}$ at the trailing edge of SHP. The data level is sampled during SHD active period, and the voltage level is held on the sampling capacitor $C_{(2)}$ at the trailing edge of SHD. Then, the switched-capacitor amplifier performs the subtraction of these two levels.

correlated double sampler (CDS) (continued)

The active polarity of SHP/SHD (active high or active low) can be chosen through the serial interface, refer to *serial interface* for details. The default value of SHP/SHD is active low. However, right after power on, this value is unknown. For this reason, it must be set to the appropriate value by using the serial interface, or reset to the default value by the RESET pin. The description and the timing diagrams in this data sheet are all based on the polarity of active low (default value).

input clamp and dummy pixel clamp

The buffered CCD output is capacitively coupled to the VSP2230. The purpose of the input clamp is to restore the dc component of the input signal that was lost with the ac-coupling and establish the desired dc bias point for the CDS. Figure 1 shows the simplified block diagram of the input clamp. The input level is clamped to the internal reference voltage REFN (1.25 V) during the dummy pixel interval. More specifically, when both CLPDM and SHP are active, then the dummy clamp function becomes active. If the dummy pixels and/or the CLPDM pulse are not available in your system, the CLPOB pulse can be used in place of CLPDM as long as the clamping takes place during black pixels. In this case, both CPLDM pin (actives as same timing as CLPOB) and SHP become active during the optical black pixel interval, then the dummy clamp function becomes active.

The active polarity of CLPDM and SHP (active high or active low) can be chosen through the serial interface, refer to *serial interface* for details. The default value of CLPDM and SHP is active low. However, right after power on, this value is unknown. For this reason, it must be set to the appropriate value by using the serial interface, or reset to the default value by the RESET pin. The description and timing diagrams in this data sheet are all based on the polarity of active low (default value).

high performance analog-to-digital converter (ADC)

The analog-to-digital converter (ADC) utilizes a fully differential and pipelined architecture. This ADC is well suited for low voltage operation, low power consumption requirement, and high-speed applications. It assures 10-bit resolution of the output data with no missing code. The VSP2230 includes the reference voltage generator for the ADC. REFP (positive reference, pin 38), REFN (negative reference, pin 39), and CM (common-mode voltage, pin 37) should be bypassed to the ground with a 0.1-μF ceramic capacitor. Do not use this voltage anywhere else in the system because it affects the stability of these reference levels, and then causes ADC performance degradation. These are analog output pins, so do not apply voltage from the outside.

programmable gain amplifier (PGA)

Figure 2 shows the characteristics of the PGA gain. The PGA provides a gain range of –6 dB to 42 dB, which is linear in dB. The gain is controlled by a digital code with 10-bit resolution, and it can be settle through the serial interface, refer to the *serial interface* section for details. The default value of the gain control code is 128 (PGA gain = 0 dB). However, right after power on, this value is unknown. For this reason, it must be set to the appropriate value by using the serial interface, or reset to the default value by the RESET pin.

programmable gain amplifier (PGA) (continued)

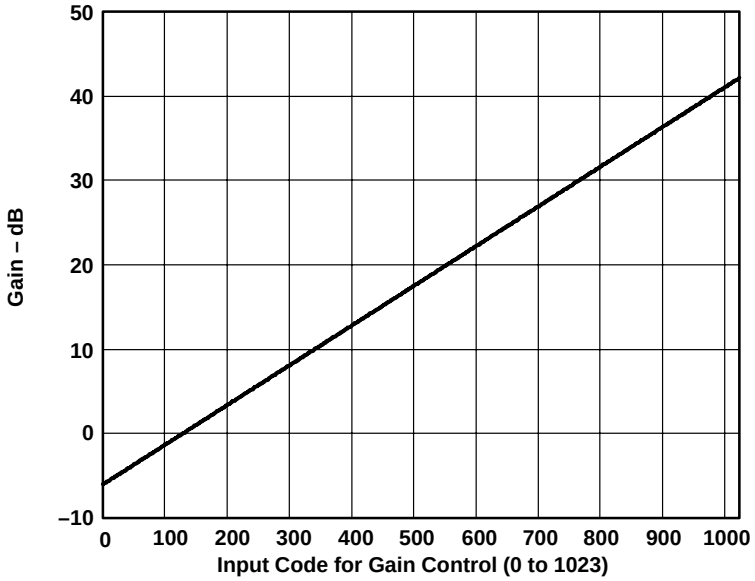


Figure 2. Characteristics of PGA Gain

optical black (OB) level clamp loop

To extract the video information correctly, the CCD signal must be referenced to a well-established optical black (OB) level. The VSP2230 has an autocalibration loop to establish the OB level using the optical black pixel output from the CCD imager. The input signal level of the OB pixels is identified as the real OB level and the loop should be closed during this period while CLPOB is active. During the effective pixel interval, the reference level of the CCD output signal is clamped to the OB level by the OB level clamp loop. To determine the loop-time constant, an off-chip capacitor is required, and should be connected to the COB (pin 28). The time constant T is given in equation 1.

$$T = \frac{C}{\left(16384 \times I_{(min)}\right)} \quad (1)$$

Where:

C is the capacitor value connected to COB, $I_{(min)}$ is the minimum current (0.15 μA) of the control DAC in the OB level clamp loop, and 0.15 μA is equivalent to 1 LSB of the DAC output current. When C is 0.1 μF, then the time constant T is 40.7 μs. Also, the slew rate (SR) is given in equation 2.

$$SR = \frac{I_{(max)}}{C} \quad (2)$$

Where:

C is the capacitor value connected to COB. $I_{(max)}$ is the maximum current (153 μA) of the control DAC in the OB level clamp loop, and 153 μA is equivalent to 1023 LSB of the DAC output current.

Generally, the OB level clamping at high-speed causes clamp noise (or white streak noise). However, the noise will decrease by increasing the capacitor size. On the other hand, a larger capacitor requires a much longer time to restore from the standby mode, or right after the power goes on. Therefore, we recommend a 0.1-μF to 0.22-μF capcitor. However, it depends on the application environment, and making careful adjustments using the cut-and-try method is recommended.

optical black (OB) level clamp loop (continued)

The OB clamp level (the pedestal level) is programmable through the serial interface, refer to *serial interface* for details. Table 1 shows the relationship between the input code and the OB clamp level.

The active polarity of CLPOB (active high or active low) can be chosen through the serial interface, refer to *serial interface* for details. The default value of CLPOB is active low.

However, right after power on, this value is unknown. For this reason, it must be set to the appropriate value by using the serial interface, or reset to the default value by the RESET pin. The description and the timing diagrams in this data sheet are all based on the polarity of active low (default value).

Table 1. Programmable OB Clamp Level

INPUT CODE	OB CLAMP LEVEL, LSBs of 10-Bits
0000	0 LSB
0001	4 LSB
0010	8 LSB
0011	12 LSB
0100	16 LSB
0101	20 LSB
0110	24 LSB
0111	28 LSB
1000 (Default)	**32 LSB**
1001	36 LSB
1010	40 LSB
1011	44 LSB
1100	48 LSB
1101	52 LSB
1110	56 LSB
1111	60 LSB

preblanking and data latency

Some CCDs have large transient output signals during blanking intervals. Such signals may exceed the VSP2230's 1-V_{P_P} input signal range and would overdrive the VSP2230 into saturation. Recovery time from the saturation could be substantial. To avoid this, the VSP2230 has an input blanking (or preblanking) function. When PBLK goes to low, the CCDIN input is disconnected from the internal CDS stage and large transients are prevented from passing through. The VSP2230's digital outputs will go to all zeros at the 11th rising edge of ADCCK from just after PBLK set to low to accommodate the clock latency of the VSP2230. In this mode, the digital output data comes out at the rising edge of ADCCK with a delay of 11 clock cycles (data latency is 11). In the normal operation mode, it is different from the preblanking mode. The digital output data comes out at the rising edge of ADCCK with a delay of nine clock cycles (data latency is 9).

In order to keep stable and accurate OB clamp level, CLPOB should not be activated during PBLK active period. Since CCDIN input is disconnected from the internal circuit, even if the autocalibration loop should be closed while CLPOB is active. Then the OB clamp level is different from the actual OB level established by the CCD imager output. The missed OB clamp level would affect the picture quality.

If the input voltage is higher than the supply rail by 0.3 V or lower than the ground rail by 0.3 V, the protection diodes will be turned on to prevent the input voltage from going further. Such a high swing signal may cause a device damage to the VSP2230 and should be avoided.

detailed description (continued)

standby mode

For the purpose of power saving, the VSP2230 can be set into the standby mode (or power down mode) through the serial interface when the VSP2230 is not in use. Refer to *serial interface* for details. In this mode, all the function blocks are disabled and the digital outputs will go to all zeros. The consumption current will drop to 2 mA. As all the bypass capacitors will discharge during this mode, a substantial time (usually of the order of 200 ms to 300 ms) is required to restore from the standby mode.

voltage reference

All the reference voltages and bias currents needed in the VSP2230 are generated by its internal bandgap circuitry. The CDS and the ADC use three reference voltages, REFP (positive reference, pin 38), REFN (negative reference, pin 39), and CM (common-mode voltage, pin 37). All of REFP, REFN, and CM should be heavily decoupled with appropriate capacitors (for example: 0.1-μF ceramic capacitor). Do not use these voltages anywhere else in the system because it affects the stability of these reference levels, and causes ADC performance degradation. These are analog output pins, so do not apply the voltage from the outside.

BYPP2 (pin 29), BYP (pin 31), and BYPM (pin 32) are also reference voltages to be used in the analog circuit. BYP should be connected to the ground with a 0.1-μF ceramic capacitor. The capacitor value for BYPP2 and BYPM affects the step response. We consider, for many applications, 200 pF to 600 pF is the reasonable value. However, it depends on the application environment, and making careful adjustments using the cut-and-try method is recommended. BYPP2, BYP, and BYPM should be heavily decoupled with the appropriate capacitors. Do not use these voltages anywhere else in the system because it affects the stability of these reference levels, and causes the performance degradation. These are analog output pins, so do not apply the voltage from the outside.

additional output delay control

The VSP2260 can control delay time of the output data by register setting through the serial interface. In some cases, the transition of the output data affects analog performance. Generally, it is avoided by adjusting the timing of the ADCCK. In case ADCCK timing cannot be adjusted, this output delay control is effective to reduce the influence of transient noise. Refer to *serial interface* for details.

serial interface

The serial interface has a 2-byte shift register and various parallel registers to control all the digitally programmable features of the VSP2230. Writing to these registers is controlled by four signals (SLOAD, SCLK, SDATA, and RESET). To enable the shift register, SLOAD must be pulled low. SDATA is the serial data input and the SCLK is the shift clock. The data at SDATA is taken into the shift register at the rising edge of SCLK. The data length should be 2 bytes. After the 2-byte shift operation, the data in the shift register will be transferred to the parallel latch at the rising edge of SLOAD. In addition to the parallel latch, there are several registers dedicated to the specific features of the device and they are synchronized with the ADCCK clock. It takes five or six clock cycles for the data in the parallel latch to be written to those registers. Thus, to complete the data updates, it has to wait five or six clock cycles after the parallel latching by the rising edge of SLOAD.

The serial interface data format is shown in Table 2. TEST is the flag for the test mode (Burr-Brown proprietary only), A0 to A2 is the address for the various registers, and D0 to D11 is the data or the operand field.

Table 2. Serial Interface Data Format

	MSB															LSB
REGISTERS	**TEST**	**A2**	**A1**	**A0**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Configuration	0	0	0	0	0	0	0	C8	0	0	0	0	0	0	0	C0
PGA gain	0	0	0	1	0	0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
OB clamp level	0	0	1	0	0	0	0	0	0	0	0	0	O3	O2	O1	O0
Clock polarity	0	0	1	1	0	0	0	0	0	0	0	0	0	P2	P1	P0
Output delay	0	1	0	0	0	0	0	0	0	0	0	0	0	0	J1	J0
Reserved	0	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x
Reserved	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x
Reserved	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x
Reserved	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x = Don't care

C0 : Operation Mode, Normal/Standby
Serial interface and registers are always active, independently from the operation mode
C0 = 0 Normal operation, C0 = 1 Standby

C8 : A/D Converter Drive Mode, Internal/External
Internal drive mode: The clock is internally generated by SHP and SHP drives the A/D converter
External drive mode: The master clock (ADCCK) drives the A/D converter
C8 = 0 Internal drive mode, C8 = 1 External drive mode

G[9:0] : Characteristics of PGA Gain (see Figure 2)

J[1:0] : Additional Output Delay Control
Controls additional output data delay time

J1 = 0, J0 = 0	Additional Delay = 0 ns
J1 = 0, J0 = 1	Additional Delay = 5 ns (typ)
J1 = 1, J0 = 0	Additional Delay = 10 ns (typ)
J1 = 1, J0 = 1	Additional Delay = 13 ns (typ)

O[3:0] : Programmable OB Clamp Level (see Table 1)

P[2:0] : Clock Polarity

P0 = Polarity for CLPDM	(P0 = 0 active low, P0 = 1 active high)
P1 = for CLPOB	(P0 = 0 active low, P0 = 1 active high)
P2 = for SHP/SHD	(P0 = 0 active low, P0 = 1 active high)

Right after power on, these values are unknown. They must be set to the appropriate value using the serial interface, or reset to the default value by the RESET pin.

Default values are:

C0 = 0	:	Normal operation mode
C8 = 0	:	A/D converter internal drive mode
G[9:0] = 0010000000	:	PGA gain = 0 dB
J[1:0] = 00	:	Additional output delay = 0 ns
O[3:0] = 1000	:	OB clamp level = 32 LSB
P[2:0] = 000	:	CLPDM, CLPOB, SHP/SHD are all active low (see Note 6)

NOTE 6: The description and the timing diagrams in this data sheet are all based on the polarity of active low (default value).

timing

VSP2230 has two options to drive the on-chip A/D converter. The internal drive mode and the external drive mode can be selected by accessing the configuration register via the serial interface. The internal drive mode, the drive clock for the A/D converter, is generated by the on-chip timing control circuit automatically, based on the SHP and SHD signals. The external drive mode is the master clock (ADCCK) and drives the on-chip A/D converter directly. The digital data output is synchronized with the master clock (ADCCK) and it is independent from the drive mode.

The CDS and the ADC are operated by SHP/SHD and their derivative timing clocks generated by the on-chip timing generator. The digital output data is synchronized with ADCCK. The timing relationship among the CCD signal, SHP/SHD, ADCCK, and the output data is shown in the VSP2230 CDS timing specifications. CLPOB is used to activate the black-level clamp loop during the OB pixel interval, and CLPDM is used to activate the input clamping during the dummy pixel interval. If the CLPDM pulse is not available in your system, the CLPOB pulse can be used in place of CLPDM as long as the clamping takes place during black pixels, refer to *input clamp and dummy pixel clamp* for details. The clock polarities of SHP/SHD, CLPOB, and CLPDM can be independently set through the serial interface, refer to *serial interface section* for details. The description and the timing diagrams in this data sheet are all based on the polarity of active low (default value). In order to keep a stable and accurate OB clamp level, it is recommended that CLPOB should not be activated during the PBLK active period. Refer to *preblanking and data latency* for details. In the standby mode, ADCCK, SHP, SHD, CLPOB, and CLPDM are internally masked and pulled high.

power supply, grounding, and device decoupling recommendations

The VSP2230 incorporates a very high-precision and high-speed analog-to-digital converter and analog circuitry that are vulnerable to any extraneous noise from the rails or elsewhere. For this reason, although the VSP2230 has analog and digital supply pins, it should be treated as an analog component and all supply pins except for DRV_{DD} should be powered by only the analog supply of the system. This will ensure the most consistent results, since digital power lines often carry high levels of wide band noise that would otherwise be coupled into the device and degrade the achievable performance.

Proper grounding, short lead length, and the use of ground planes are also very important for high frequency designs. Multilayer PC boards are recommended for the best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. It is highly recommended that the analog and digital ground pins of the VSP2230 be joined together at the IC and be connected only to the analog ground of the system. The driver stage of the digital outputs (B[9:0]) is supplied through a dedicated supply pin (DRV_{DD}) and should be separated from the other supply pins completely, or at least with a ferrite bead. It is also recommended to keep the capacitive loading on the output data lines as low as possible (typically less than 15 pF). Larger capacitive loads demand higher charging current due to surges that can feed back into the analog portion of the VSP2230 and affect the performance.

If possible, external buffers or latches should be used which provide the added benefit of isolating the VSP2230 from any digital noise activities on the data lines. In addition, resistors in series with each data line may help in minimizing the surge current. Values in the range of 100 Ω to 200 Ω will limit the instantaneous current to the output stage and has to provide for recharging the parasitic capacitance's as the output levels change from low-to-high or high-to-low. Because of the high operation speed, the converter also generates high frequency current transients and noises that are fed back into the supply and reference lines. This requires the supply and reference pins to be sufficiently bypassed. In most cases, a 0.1-μF ceramic-chip capacitor is adequate to decouple the reference pins. Supply pins should be decoupled to the ground plane with a parallel combination of tantalum (1 μF to 22 μF) and ceramic (0.1 μF) capacitors. The effectiveness of the decoupling largely depends on the proximity to the individual pin. DRV_{DD} should be decoupled to the proximity of DRVGND. Special attention must be paid to the bypassing of COB, BYPP2, and BYPM since these capacitor values determine important analog performance of the device.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (V_{CC}, DRV_{DD}) . . . . . ±0.1 V
Supply voltage differences (among V_{CC}) . . . . . ±0.1 V
Ground voltage differences (among GNDA) . . . . . 0.3 V to 5.3 V
Digital input voltage . . . . . –0.3 V to 5.3 V
Analog input voltage . . . . . –0.3 V to V_{CC} + 0.3 V
Input current (any pins except supplies) . . . . . ±10 mA
Operating temperature, T_A . . . . . –25°C to 85°C
Storage temperature, T_{stg} . . . . . –55°C to 125°C
Junction temperature, T_J . . . . . 150°C
Lead temperature (soldering) . . . . . 260°C, 5 sec
Package temperature (IR Reflow, Peak) . . . . . 235°C, 10 sec

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = DRV_{DD} = 3 V, conversion rate $f_{(ADCCK)}$ = 36 MHz, no load unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10		Bits
	Max conversion rate		36			MHz
	Digital inputs					
	Logic family			TTL		
V_{IT-}	Low-to-high threshold voltage			1.9		V
V_{IT+}	High-to-low threshold voltage			0.9		V
I_{IH}	High-level input current	V_{IN} = 3 V			±20	µA
I_{IL}	Low-level input current	V_{IN} = 0 V			±20	
	ADCCK clock duty cycle			50%		
	Input capacitance			5		pF
	Max input voltage		–0.3		5.3	V
	Digital inputs					
	Logic family			CMOS		
	Logic coding			Straight binary		
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	
	Additional output data delay	J[1:0] = 00		0		ns
		J[1:0] = 01		5		ns
		J[1:0] = 10		10		ns
		J[1:0] = 11		13		ns

reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive reference voltage			1.75		V
Negative reference voltage			1.25		V

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = DRV_{DD} = 3 V, conversion rate $f_{(ADCCK)}$ = 36 MHz, no load unless otherwise noted (continued)

power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage, DRV_{DD}		2.7	3	3.6	V
P_D	Power dissipation	Normal operation mode: V_{CC} = DRV_{DD} = 2.7 V, f_{ADCCK} = 36 MHz, No Load		130		mW
		Standby mode: $f_{(ADCCK)}$ = Not applied		6		

temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A	Operation temperature		–25		85	°C
T_{stg}	Storage temperature		–55		125	°C
	Thermal resistance θ_{JA}	48-pin LQFP		100		°C/W

analog input (CCDIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input signal level for full-scale out	PGA gain = 0 dB	900			mV
Input capacitance			15		pF
Input limit		–0.3		3.3	V

transfer characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNL	Differential nonlinearity	PGA gain = 0 dB		±0.5		LSB
INL	Integral nonlinearity	PGA gain = 0 dB		±1		LSB
	No missing codes			Assured		
	Step response settling time	Full-scale step input		1		pixel
	Overload recovery time	Step input from 1.8 V to 0 V		2		pixels
	Data latency			9(fixed)		Clock cycles
SNR	Signal-to-noise ratio (see Note 7)	Grounded input cap, PGA gain = 0 dB		76		dB
		Grounded input cap, Gain = 24 dB		52		
	CCD offset correction range		–180		200	mV

NOTE 7: SNR = 20 log (full-scale voltage/rms noise)

CDS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference sample settling time	Within 1 LSB, driver impedance = 50 Ω		6.9		ns
Data sample settling time			6.9		

input clamp

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clamp-on resistance			400		Ω
Clamp level			1.25		V

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = DRV_{DD} = 3 V, conversion rate (fADCCK) = 36 MHz, no load unless otherwise noted (continued)

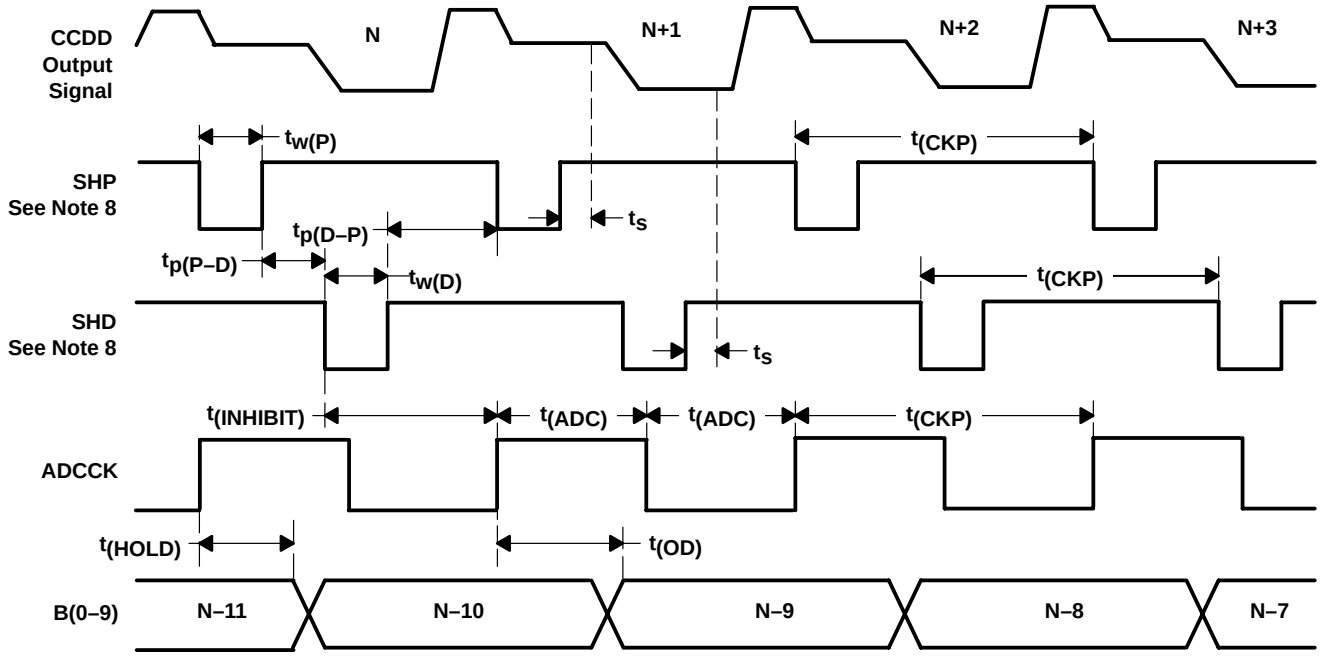
programmable gain amplifier (PGA)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain control resolution			10		Bits
Maximum gain	Gain code = 1111111111		42		dB
High gain	Gain code = 1101001000		34		dB
Medium gain	Gain code = 1000100000		20		dB
Low gain	Gain code = 0010000000		0		dB
Minimum gain	Gain code = 0000000000		–6		dB
Gain control error			±0.5		dB

optical black clamp loop

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Control DAC resolution			10		Bits
	Optical black clamp level	Programmable range of clamp level	0		60	LSB
		OBCLP level at CODE = 1000		32		LSB
	Minimum output current for control DAC	COB pin		±0.15		µA
	Maximum output current for control DAC			±153		
	Loop time constant	$C_{(COB)}$ = 0.1 µF		40.7		µs
SR	Slew rate	$C_{(COB)}$ = 0.1 µF, Output current from control DAC is saturated		1530		V/s

timing specifications



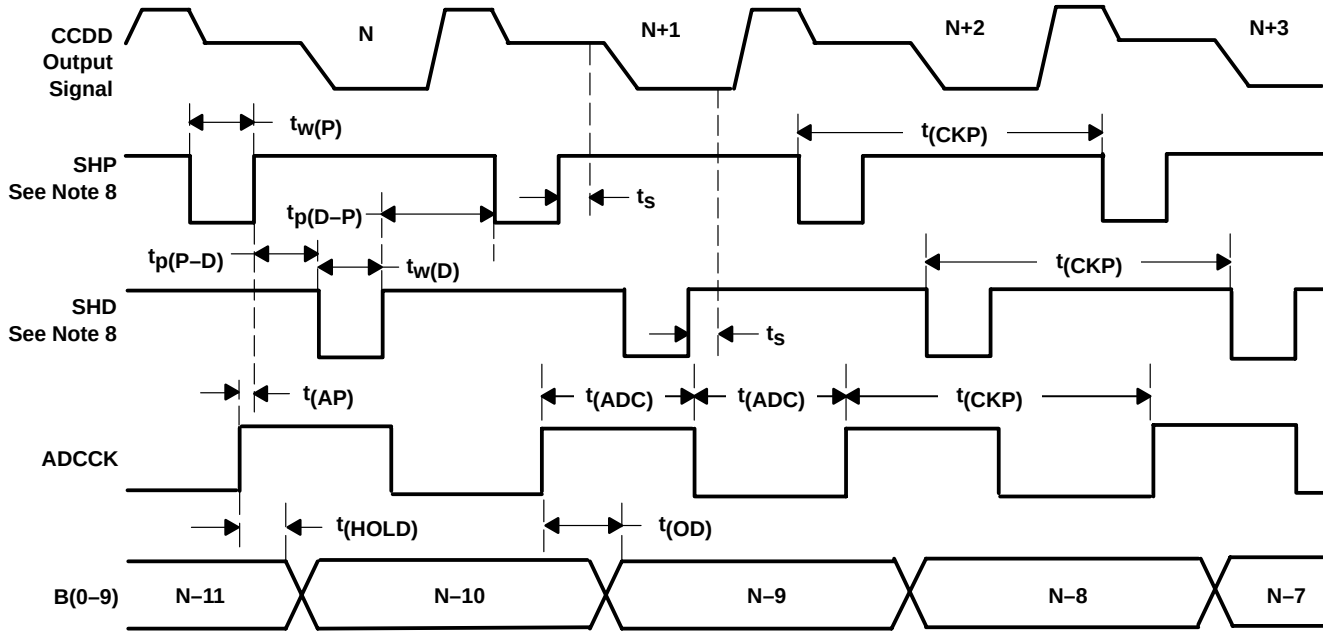
PARAMETER		MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	27.7			ns
$t_{(ADC)}$	ADCCK high/low pulse width		13.8		ns
$t_{w(P)}$	SHP pulse width		6.9		ns
$t_{w(D)}$	SHD pulse width		6.9		ns
$t_{p(P–D)}$	SHP trailing edge to SHD leading edge (see Note 8)	4			ns
$t_{p(D–P)}$	SHD trailing edge to SHP leading edge (see Note 8)	8			ns
t_S	Sampling delay		3		ns
$t_{(Inhibit)}$	Inhibited clock period	12			ns
$t_{(Hold)}$	Output hold time (see Note 9)	2			ns
$t_{(OD)}$	Output delay			27.7	ns
DL	Data latency, normal operation mode		9 (fixed)		Clock cycles

NOTES: 8. The description and the timing diagrams in this data sheet are all based on the polarity of active low (default value). The active polarity (active low or active high) can be chosen through the serial interface, refer to *serial interface* for details.

9. Output hold time is specified at additonal output delay = 0 ns. Refer to *serial interface* section for detail.

Figure 3. VSP2230 CDS Timing Specifications—A/D Converter Internal Drive Mode

timing specifications (continued)



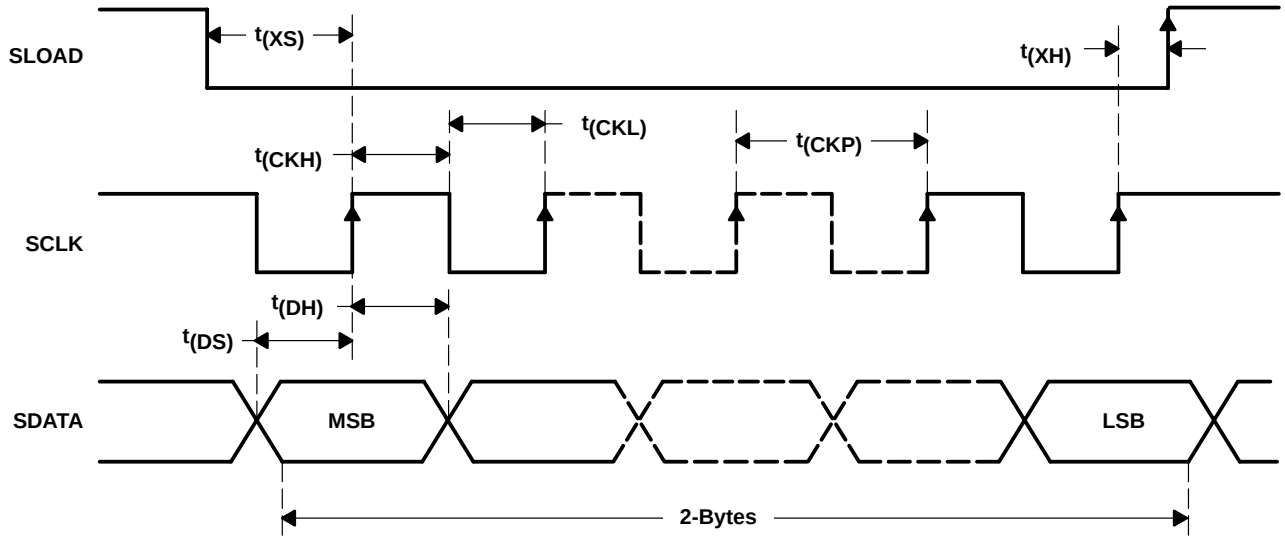
PARAMETER		MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	27.7			ns
$t_{(ADC)}$	ADCCK pulse duty rate	45%	50%	55%	
$t_{w(P)}$	SHP pulse width		6.9		ns
$t_{w(D)}$	SHD pulse width		6.9		ns
$t_{p(P–D)}$	SHP trailing edge to SHD leading edge (see Note 8)	1			ns
$t_{p(D–P)}$	SHD trailing edge to SHP leading edge (see Note 8)	6			ns
t_S	Sampling delay		3		ns
$t_{(AP)}$	ADCCK leading edge to SHP trailing edge	0	1.5		ns
$t_{(Hold)}$	Output hold time (see Note 9)	2			ns
$t_{(OD)}$	Output delay			27.7	ns
DL	Data latency, normal operation mode		9 (fixed)		Clock cycles

NOTES: 8: The description and the timing diagrams in this data sheet are all based on the polarity of active low (default value). The active polarity (active low or active high) can be chosen through the serial interface, refer to *serial interface* for details.

9. Output hold time is specified at additonal output delay = 0 ns. Refer to serial interface section for detail.

Figure 4. VSP2230 CDS Timing Specifications—A/D Converter External Drive Mode

timing specifications (continued)



PARAMETER		MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	100			ns
$t_{(CKH)}$	Clock high pulse width	40			ns
$t_{(CKL)}$	Clock low pulse width	40			ns
t_{su}	Data setup time	30			ns
t_h	Data hold time	30			ns
$t_{(XS)}$	SLOAD to SCLK setup time	30			ns
$t_{(XH)}$	SCLK to SLOAD hold time	30			ns

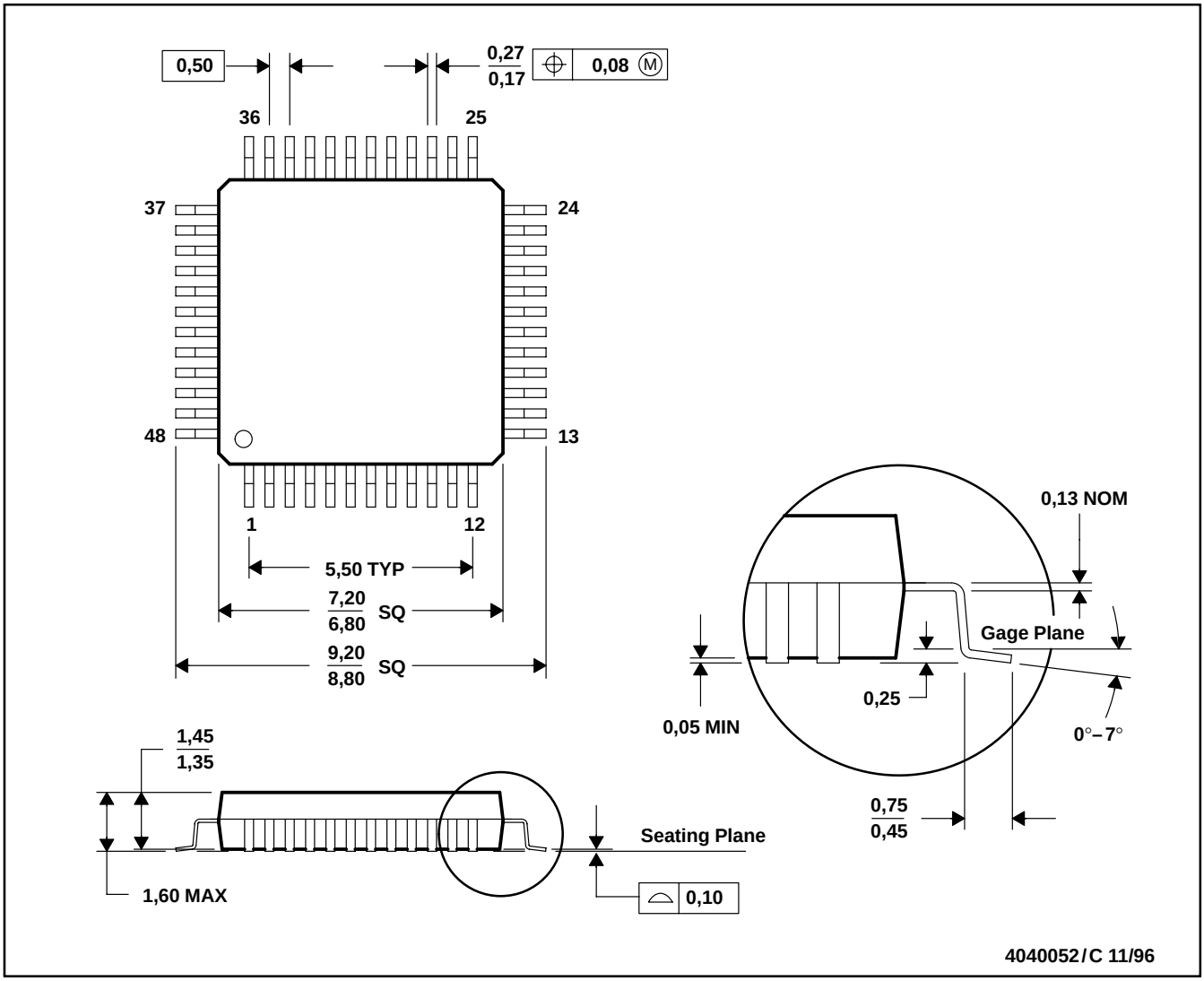
NOTES: 10. It is effective for the data shift operation at the rising edges of SCLK during SLOAD is low period. 2 bytes of data input are loaded to the parallel latch in the VSP2230 at the rising edge of SLOAD.

11. When the input serial data is longer than 2 bytes (16 bits), the last 2 bytes become effective and the former bits are lost.

Figure 5. VSP2230 Serial Interface Timing Specification

MECHANICAL DATA

PT (S-PQFP-G48) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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