

# SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS

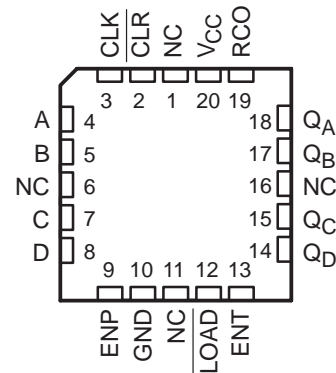
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable

SN54HC161 . . . J OR W PACKAGE  
SN74HC161 . . . D, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC161 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC161 devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC161N	SN74HC161N
	SOIC – D	Tube of 40	SN74HC161D	HC161
		Reel of 2500	SN74HC161DR	
		Reel of 250	SN74HC161DT	
	SOP – NS	Reel of 2000	SN74HC161NSR	HC161
	TSSOP – PW	Tube of 90	SN74HC161PW	HC161
Reel of 2000		SN74HC161PWR		
Reel of 250		SN74HC161PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC161J	SNJ54HC161J
	CFP – W	Tube of 150	SNJ54HC161W	SNJ54HC161W
	LCCC – FK	Tube of 55	SNJ54HC161FK	SNJ54HC161FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
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# SN54HC161, SN74HC161

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### description/ordering information (continued)

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'HC161 devices is asynchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ( $\overline{\text{LOAD}}$ ), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with  $Q_A$  high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.



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## logic diagram (positive logic)



† For simplicity, routing of complementary signals  $\overline{\text{LD}}$  and  $\overline{\text{CK}}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, J, N, NS, PW, and W packages.

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## logic symbol, each D/T flip-flop



## logic diagram, each D/T flip-flop (positive logic)



† The origins of  $\overline{LD}$  and  $\overline{CK}$  are shown in the logic diagram of the overall device.

**typical clear, preset, count, and inhibit sequence**

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		SN54HC161			SN74HC161			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V			0.5	0.5	V	
		$V_{CC} = 4.5$ V			1.35	1.35		
		$V_{CC} = 6$ V			1.8	1.8		
$V_I$	Input voltage	0		$V_{CC}$	0	$V_{CC}$	V	
$V_O$	Output voltage	0		$V_{CC}$	0	$V_{CC}$	V	
$\Delta t/\Delta v$ ‡	Input transition rise/fall time	$V_{CC} = 2$ V			1000	1000	ns	
		$V_{CC} = 4.5$ V			500	500		
		$V_{CC} = 6$ V			400	400		
$T_A$	Operating free-air temperature	–55		125	–40	85	°C	

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from  $V_{ILmax} = 0.5$  V to  $V_{IHmin} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC161		SN74HC161		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC161		SN74HC161		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		6		4.2		5	MHz
		4.5 V		31		21		25	
		6 V		36		25		29	
t <sub>w</sub>	Pulse duration	CLK high or low	2 V	80		120		100	ns
			4.5 V	16		24		20	
			6 V	14		20		17	
	CLR low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t <sub>su</sub>	A, B, C, or D	2 V	150		225		190	ns	
		4.5 V	30		45		38		
		6 V	26		38		32		
		LOAD low	2 V	135		205			170
			4.5 V	27		41			34
			6 V	23		35			29
	ENP, ENT	2 V	170		255		215		
		4.5 V	34		51		43		
		6 V	29		43		37		
	CLR inactive	2 V	125		190		155		
		4.5 V	25		38		31		
		6 V	21		32		26		
t <sub>h</sub>	Hold time, all synchronous inputs after CLK↑	2 V	0		0		0	ns	
		4.5 V	0		0		0		
		6 V	0		0		0		



# SN54HC161, SN74HC161

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

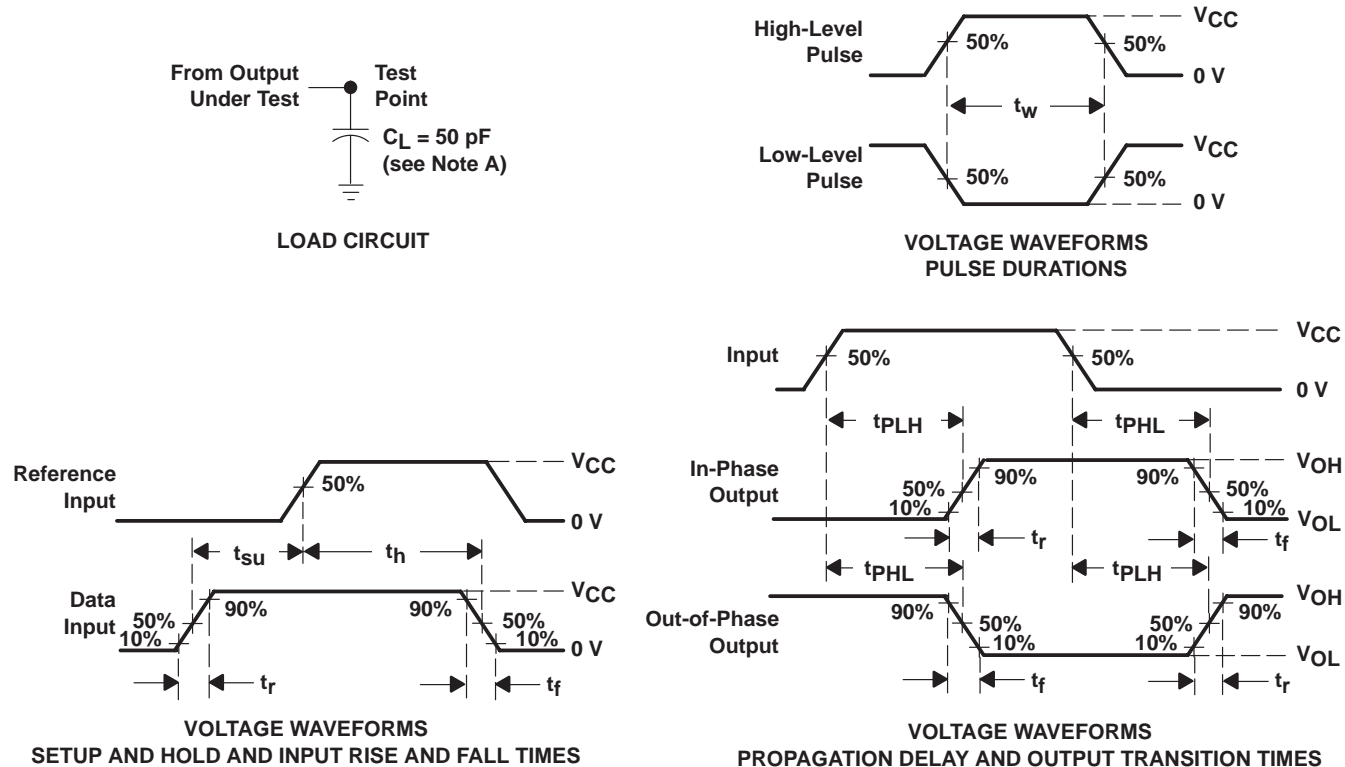
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC161		SN74HC161		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			2 V	6	14		4.2		5	MHz	
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
$t_{pd}$	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
		Any Q	2 V		80	205		310		255	
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
	ENT	RCO	2 V		62	195		295		245	
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
$t_{PHL}$	$\overline{\text{CLR}}$	Any Q	2 V		105	210		315		265	ns
			4.5 V		21	42		63		53	
			6 V		18	36		54		45	
		RCO	2 V		110	220		330		275	
			4.5 V		22	44		66		55	
			6 V		19	37		56		47	
$t_t$		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	60	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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## APPLICATION INFORMATION

### n-bit synchronous counters

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC161 devices count in binary. Virtually any count mode (modulo-N,  $N_1$ -to- $N_2$ ,  $N_1$ -to-maximum) can be used with this fast look-ahead circuit.

The application circuit shown in Figure 2 is not valid for clock frequencies above 18 MHz (at 25°C and 4.5-V  $V_{CC}$ ). The reason for this is that there is a glitch that is produced on the second stage's RCO and every succeeding stage's RCO. This glitch is common to all HC vendors that Texas Instruments has evaluated, in addition to the bipolar equivalents (LS, ALS, AS).

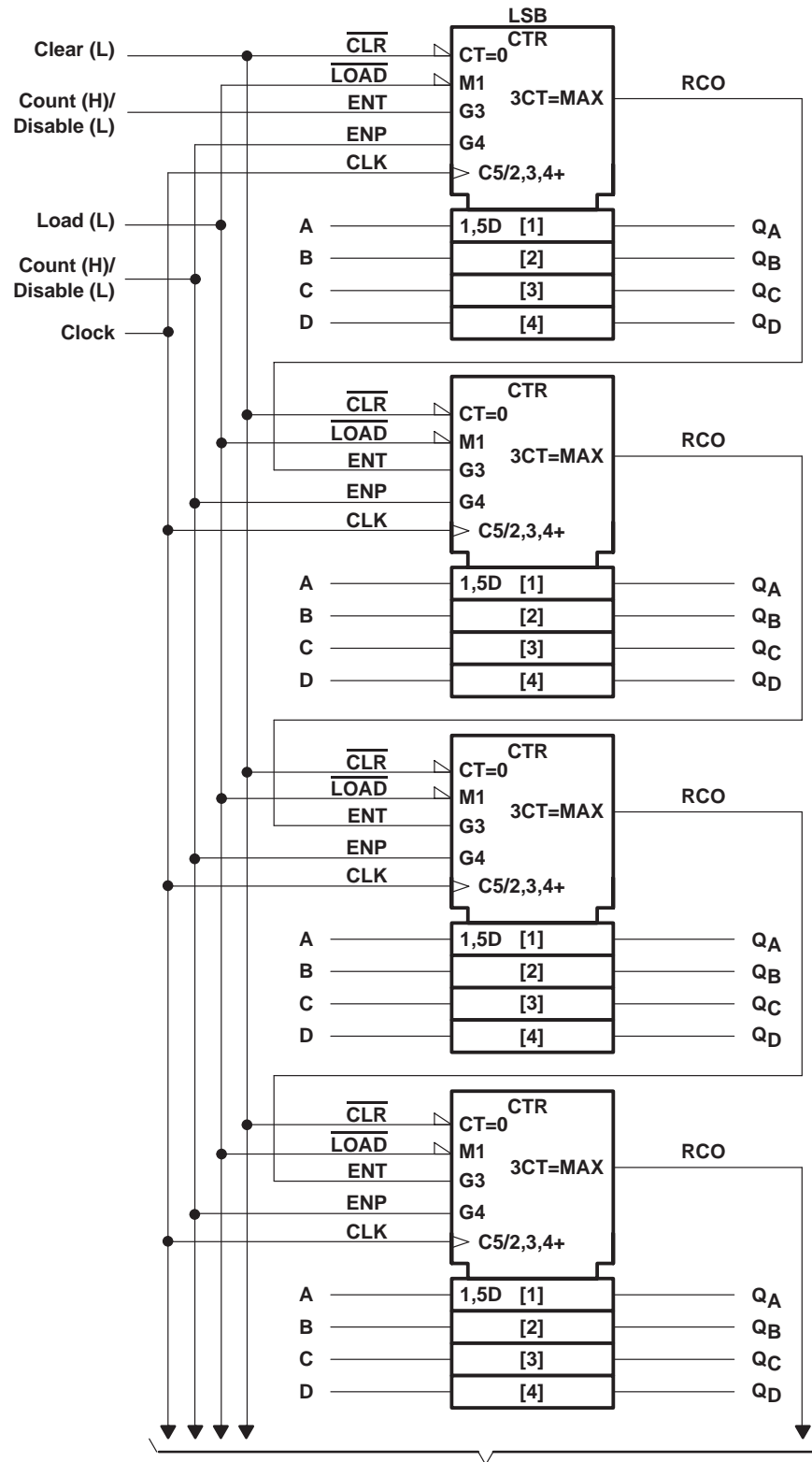


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## APPLICATION INFORMATION



To More-Significant Stages

Figure 2



# SN54HC161, SN74HC161

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### APPLICATION INFORMATION

The glitch on RCO is caused because the propagation delay of the rising edge of  $Q_A$  of the second stage is shorter than the propagation delay of the falling edge of ENT. RCO is the product of ENT,  $Q_A$ ,  $Q_B$ ,  $Q_C$ , and  $Q_D$  ( $ENT \times Q_A \times Q_B \times Q_C \times Q_D$ ). The resulting glitch is about 7–12 ns in duration. Figure 3 shows the condition in which the glitch occurs. For simplicity, only two stages are being considered, but the results can be applied to other stages.  $Q_B$ ,  $Q_C$ , and  $Q_D$  of the first and second stage are at logic one, and  $Q_A$  of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse,  $Q_A$  and RCO of the first stage go high. On the rising edge of the third clock pulse,  $Q_A$  and RCO of the first stage return to a low level, and  $Q_A$  of the second stage goes to a high level. At this time, the glitch on RCO of the second stage appears because of the race condition inside the chip.



Figure 3

The glitch causes a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than the inverse of the sum of the clock-to-RCO propagation delay and the glitch duration ( $t_g$ ). In other words,  $f_{max} = 1/(t_{pd} \text{ CLK-to-RCO} + t_g)$ . For example, at 25°C at 4.5-V  $V_{CC}$ , the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following tables contain the  $f_{clock}$ ,  $t_w$ , and  $f_{max}$  specifications for applications that use more than two 'HC161 devices cascaded together.

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## APPLICATION INFORMATION

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC161		SN74HC161		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub> Clock frequency	2 V		3.6		2.5		2.9	MHz
	4.5 V		18		12		14	
	6 V		21		14		17	
t <sub>w</sub> Pulse duration, CLK high or low	2 V	140		200		170		ns
	4.5 V	28		40		36		
	6 V	24		36		30		

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Note 4)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC161		SN74HC161		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	3.6		2.5		2.9		MHz
			4.5 V	18		12		14		
			6 V	21		14		17		

NOTE 4: These limits apply only to applications that use more than two 'HC161 devices cascaded together.

If the 'HC161 devices are used as a single unit, or only two cascaded together, then the maximum clock frequency that the device can use is not limited because of the glitch. In these situations, the device can be operated at the maximum specifications.

A glitch can appear on RCO of a single 'HC161 device, depending on the relationship of ENT to CLK. Any application that uses RCO to drive any input except an ENT of another cascaded 'HC161 device must take this into consideration.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8407501VEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8407501VE A SNV54HC161J	<a href="#">Samples</a>
84075012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84075012A SNJ54HC 161FK	<a href="#">Samples</a>
8407501EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407501EA SNJ54HC161J	<a href="#">Samples</a>
8407501FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407501FA SNJ54HC161W	<a href="#">Samples</a>
JM38510/66302BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 66302BEA	<a href="#">Samples</a>
M38510/66302BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 66302BEA	<a href="#">Samples</a>
SN54HC161J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC161J	<a href="#">Samples</a>
SN74HC161D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	
SN74HC161DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	<a href="#">Samples</a>
SN74HC161DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	<a href="#">Samples</a>
SN74HC161DT	LIFEBUY	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	
SN74HC161N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC161N	<a href="#">Samples</a>
SN74HC161NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	<a href="#">Samples</a>
SN74HC161PW	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	
SN74HC161PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	<a href="#">Samples</a>
SN74HC161PWT	LIFEBUY	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161	
SNJ54HC161FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84075012A SNJ54HC 161FK	<a href="#">Samples</a>
SNJ54HC161J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407501EA SNJ54HC161J	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54HC161W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407501FA SNJ54HC161W	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC161, SN54HC161-SP, SN74HC161 :**

- Catalog : [SN74HC161](#), [SN54HC161](#)
- Military : [SN54HC161](#)
- Space : [SN54HC161-SP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC161DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC161NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC161PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC161PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC161DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC161NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC161PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC161PWT	TSSOP	PW	16	250	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84075012A	FK	LCCC	20	1	506.98	12.06	2030	NA
8407501FA	W	CFP	16	1	506.98	26.16	6220	NA
SN74HC161D	D	SOIC	16	40	507	8	3940	4.32
SN74HC161N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC161N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC161PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54HC161FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54HC161W	W	CFP	16	1	506.98	26.16	6220	NA



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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