MAX20790

Smart Power-Stage IC with Integrated Current and Temperature Sensors

General Description

The MAX20790 is a feature-rich smart power-stage IC designed to work with Maxim's controllers to implement a high-density multiphase voltage regulator. Multiple smart power-stage ICs plus a controller provide a compact synchronous buck converter that includes accurate individual phase current and temperature reporting through PMBus™. These smart power-stage devices include fault-protection circuits for overtemperature, VX short, and supply undervoltage lockout (UVLO). The MAX20790 immediately shuts down on fault detection, communicating the Fault_ID to the controller.

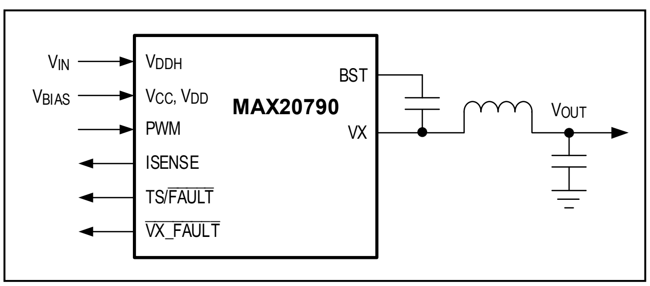
Monolithic integration and advanced packaging technology allow high-switching frequencies with significantly lower losses than conventional implementations. Phase-shedding and discontinuous conduction modes (DCM) optimize efficiency over a wide range of load currents.

The MAX20790 is available in a 12-pin FC2QFN package with an exposed top-side thermal pad (3.25mm x 7.4mm).

Applications

- High-Current Multiphase-Voltage Regulators
  - Networking ASICs
  - AI and Machine Learning ASICs
  - Graphics Processors
- Servers, Workstations, and Enterprise Storage
- Communications and Networking Equipment
- AI and Machine Learning

Typical Operating Circuit



Benefits and Features

- Space-Optimized Solution
  - Monolithic, Smart Power Stage
  - Phase-Current Steering for Thermal Balance
  - Small Footprint: ~24mm^2
- 95.6% Peak Efficiency
  - 6-Phase, 400kHz, 12V V_{IN}, 1.8V V_{OUT}
- 300kHz to 1.3MHz Switching Frequency
- Telemetry and Fault Reporting through Controller IC PMBus
  - Accurate Temperature Monitoring and Reporting
  - Accurate Per-Phase Current Reporting
  - Fault_ID Indicates Type of Fault
- Advanced Self-Protection Features
  - Supply and Boost UVLO Protection
  - Boost Refresh
  - VX Short and Overtemperature Shutdown
  - Fast Overcurrent Protection

Ordering Information appears at end of data sheet.

Electrical and Thermal Ratings

DESCRIPTION	CURRENT RATING* (A)	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)
Electrical Rating**	86	4.5 to 16	0.25 to 2.3V
Thermal Rating T_A = 55°C, 200LFM	52	12	1.8
Thermal Rating T_A = 55°C, 200LFM	60	12	1.0

**T_J = 125°C. For specific operating conditions, see the SOA curves in the Typical Operating Characteristics section.*
*** Maximum-Phase DC current limited by POCP and FASTPOCP_R typical values*

Absolute Maximum Ratings

V_{DDH} to V_{SS}, $\overline{\text{VX\_FAULT}}$ to V_{SS} (Note 1)............-0.3V to +19V
VX to V_{SS} (DC) ....-0.3V to +19V
VX to V_{SS} (AC) (Notes 1, 2) ....-10V to +23V
V_{DDH} to VX (DC)...-0.3V to +19V
V_{DDH} to VX (AC) (Notes 1, 2)................................-10V to +23V
BST to V_{SS} (DC) ....-0.3V to +21.5V
BST to V_{SS} (AC) (Note 2) ....-7V to +25.5V
BST to VX Differential ....-0.3V to +2.5V
BST to V_{CC} Differential (DC) ....-0.3V to +19V
BST to V_{CC} Differential (AC) (Notes 1, 2)............-0.3V to +23V
V_{DD}, V_{CC} to AGND ....-0.3V to +2.5V
PWM, ISENSE, TS/$\overline{\text{FAULT}}$
to AGND ....-0.3V to V_{DD} + 0.3V
V_{SS} to AGND ....-0.3V to +0.3V
Peak VX Current (Note 3) ....-70A to +120A
Junction Temperature (T_J)..+150°C
Storage Temperature Range .... -65°C to +150°C
Peak Reflow Temperature Lead-Free ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 FC2QFN	
Package Code	F123A7F+1
Outline Number	**21-100261**
Land Pattern Number	**90-100099**
THERMAL RESISTANCE	
Junction to Ambient (θ_{JA}) (Note 4)	8°C/W
Junction to Case (θ_{JC_TOP})	0.25°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Input HF capacitors placed not more than 40 mils away from the V_{DDH} pin required to keep inductive voltage spikes within Absolute Maximum limits.
Note 2: AC is limited to 25ns.
Note 3: POCP and FASTPOCP_R limit the application below the peak VX current rating.
Note 4: Applicable only to the MAX16600 EV Kit in free space with no airflow.

Continuous Smart Power-Stage Thermal Design Current (TDC)

T_J = 115°C, 500kHz, V_{DDH} = 12V, no heatsink, PCB temperature is controlled at 95°C.

AIRFLOW	V_{OUT} = 1.0V, NO LL (A) 6-PHASE APPLICATION	
	T_A = 25°C	T_A = 55°C
0LFM	40	39
200LFM	45	42
400LFM	47	45

Electrical Characteristics

(See *Typical Multiphase Application Circuit*, V_{DDH} = 12V, V_{CC} = V_{DD} = 1.8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +32°C. All devices 100% tested at T_A = T_J = +32°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES, SUPPLY CURRENT							
Input-Supply Voltage Range	V_{DDH}			4.5		16	V
Bias-Supply Voltage Range	V_{CC}, V_{DD}			1.71		1.98	V
Input-Supply Current	I_{DDH}	Shutdown (PWM = 0, TS/$\overline{FAULT}$ = 0, ISENSE = 0), T_A = +32°C			1.3	10	µA
		Inactive, no switching (PWM = Hi-Z), T_A = +32°C			650	2000	µA
Bias-Supply Current	I_{CC} + I_{DD}	Shutdown (PWM = 0, TS/$\overline{FAULT}$ = 0, ISENSE = 0), T_A = +32°C			3	6	µA
		Inactive, no switching (PWM = Hi-Z), T_A = +32°C			3	6.5	mA
		Load = 0, duty cycle = 15%, f_{SW} = 600kHz, T_A = +32°C			44		mA
I_{RECON} SPECIFICATIONS							
Current-Sense Gain	A_I	ISENSE/I_{VX}, duty cycle ≤ 20%	0A ≤ I_{VX} ≤ +35A (Note 5)	9.6	10	10.4	µA/A
			+35A < I_{VX} ≤ FASTPOCP_R (Note 6)	9.55	10	10.45	µA/A
Current-Sense Offset		Duty cycle ≤ 20%, no load		-5	0	+5	µA
I_{RECON} Bandwidth		I_{LOAD} = 0A			5		MHz
		I_{LOAD} = 85A			10		MHz

Electrical Characteristics (continued)

(See *Typical Multiphase Application Circuit*, V_{DDH} = 12V, V_{CC} = V_{DD} = 1.8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +32°C. All devices 100% tested at T_A = T_J = +32°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE SENSOR						
Temperature-Sensor Dynamic Range	T_{RANGE}	(Note 7)	-40		+125	°C
Temperature-Sensor Gain	A_{TEMP}	(Note 7), T_J = -40°C to 0°C	2.859	3.163	3.466	mV/°C
		(Note 7), T_J = 0°C to +125°C	2.954	3.0835	3.213	
Temperature-Sensor Voltage	$V_{TS/\overline{FAULT}}$, 0°C	T_J = 0°C (Note 7)	810	821	833	mV
	$V_{TS/\overline{FAULT}}$, 125°C	T_J = +125°C (Note 7)	1190	1206	1224	
Temperature-Sensor Bandwidth	$V_{TS/\overline{FAULT}}$			144		kHz
PROTECTION FEATURES						
V_{DDH} Undervoltage Lockout (Rising)	V_{DDH_UVLO}	Rising V_{DDH}, 200mV hysteresis	4.00	4.17	4.31	V
V_{DD} Undervoltage Lockout	V_{DD_UVLO}	Rising V_{DD}, 60mV hysteresis			1.7	V
		Falling V_{DD}	1.47	1.52	1.57	
BST Undervoltage Lockout (Rising)	V_{BST_UVLO}	Rising V_{BST}, 60mV hysteresis	1.47	1.56	1.62	V
V_{DD} Power on Reset (Falling)	V_{DD_POR}	Falling V_{DD}, 110mV hysteresis		1		V
Positive Current Limit (Rising)	FASTPOCP_R	Per-phase-nonlatched peak current limit	82	88	93	A
Positive Current Limit (Falling)	POCP	Per-phase HS on inhibit level	75	84	92	A
Negative Current Limit	NOCP	Per-phase LS on inhibit level			-50	A
FASTPOCP_ Propagation Delay	$td_{FASTPOCP}$			15		ns
Overtemperature Protection/ Shutdown	T_{SHDN}	Rising threshold		160		°C
HS_VXSHORT Threshold	$V_{HSVXSHRT\_TH}$	HS on and VX shorted to V_{SS}		V_{DDH} - 0.67		V
LS_VXSHORT Threshold	$V_{LSVXSHRT\_TH}$	LS on and VX shorted to V_{DDH}		0.2 x V_{CC}		V
VX Short Fault Detect to $\overline{VX\_FAULT}$ Low Delay	t_{VXFLB_LOW}			25		ns
$\overline{VX\_FAULT}$ PIN						
$\overline{VX\_FAULT}$ Output Low	V_{VXFLB_VOL}	Output logic-low (I = 1mA)			90	mV
$\overline{VX\_FAULT}$ Leakage Current	I_{VXFLB_LK}	$\overline{VX\_FAULT}$ = 12V, T_A = +32°C			1	µA
TS/$\overline{FAULT}$ PIN						
TS/$\overline{FAULT}$ Digital Threshold	V_{TSFB_IH}	Input logic-high	0.69			V
	V_{TSFB_IL}	Input logic-low			0.3	V
	V_{TSFB_HL}	Output logic-high, (I = 1mA)	V_{DD} - 0.33			V
	V_{TSFB_OL}	Output logic-low, (I = 10mA)			0.12	V
Fault Detect to TS/$\overline{FAULT}$ Low Delay	t_{TSFLB_LOW}			535		ns

Electrical Characteristics (continued)

(See *Typical Multiphase Application Circuit*, V_{DDH} = 12V, V_{CC} = V_{DD} = 1.8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +32°C. All devices 100% tested at T_A = T_J = +32°C. Limits over temperature guaranteed by design.)

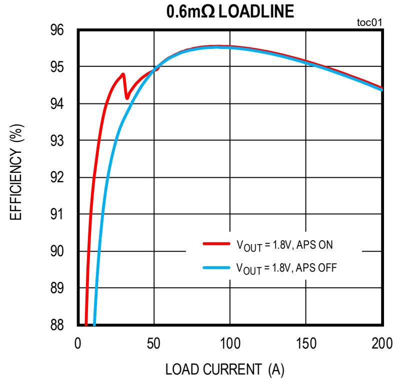
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM AND VX PIN						
PWM Input Levels	V_{PWM_H}	Input logic-high	V_{DD} - 0.23			V
	V_{PWM_L}	Input logic-low			0.24 x V_{DD}	V
	V_{PWM_MID}	PWM input midlevel for VX three-state control		0.68		V
PWM Midlevel Hold Time	$t_{PWM\_MID\_HOLD}$	VX low to Hi-Z transition		50		ns
PWM Input Current	I_{PWM_H}	Input current, PWM high		260		μA
	I_{PWM_L}	Input current, PWM low		-430		μA
Minimum VX On-Time	t_{VX_MIN}			34		ns
ISENSE PINS						
ISENSE Input Levels	V_{ISNS_H}	Input logic-high	0.81			V
	V_{ISNS_L}	Input logic-low			0.43	

Note 5: Replica current tested in production. Actual current-sense gain tolerance validated in application.
Note 6: Guaranteed by design to 4-sigma
Note 7: Not production tested.

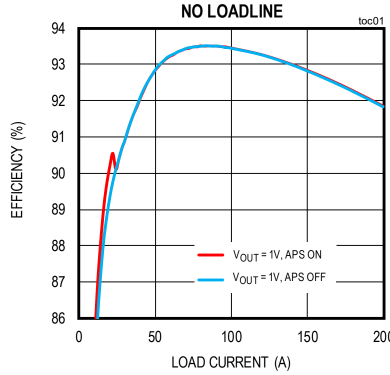
Typical Operating Characteristics

(V_{DDH} = 12V, T_A = +25°C, f_{SW} = 400kHz, 6-phase configuration, inductor = CLH1110-6, unless otherwise noted.)

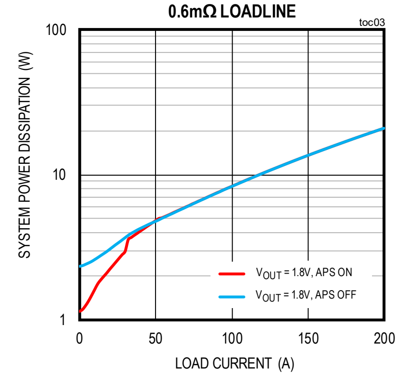
EFFICIENCY vs. LOAD CURRENT
0.6mΩ LOADLINE



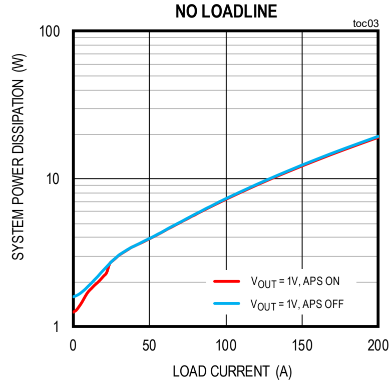
EFFICIENCY vs. LOAD CURRENT
NO LOADLINE



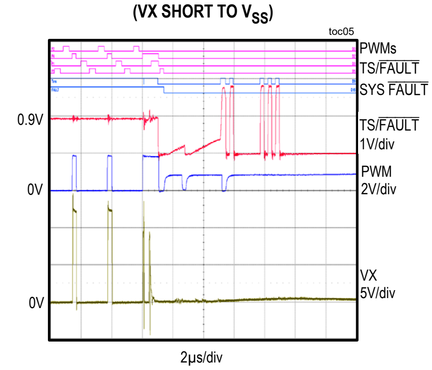
SYSTEM POWER DISSIPATION vs. LOAD CURRENT
0.6mΩ LOADLINE



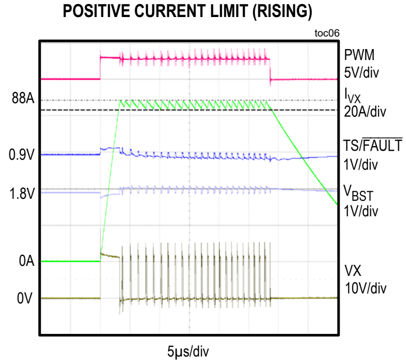
SYSTEM POWER DISSIPATION vs. LOAD CURRENT
NO LOADLINE



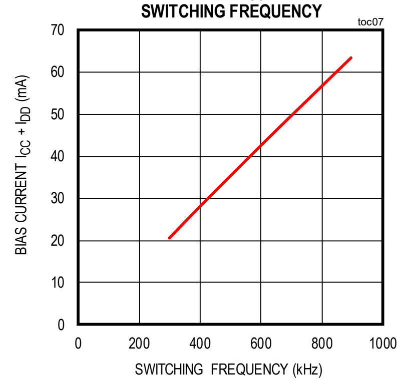
HS_VXSHORT FAULT
(VX SHORT TO V_{SS})



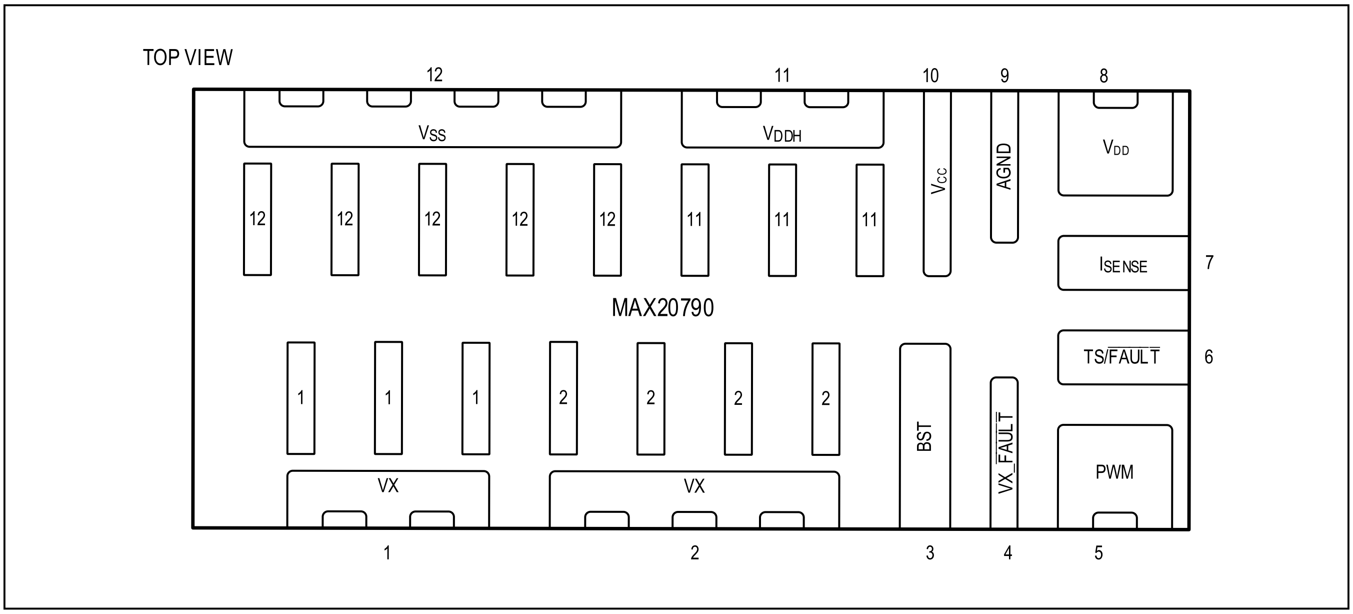
MAX20790 FASTPOCP_R
POSITIVE CURRENT LIMIT (RISING)



BIAS CURRENT I_{CC} + I_{DD} vs.
SWITCHING FREQUENCY



Pin Configurations



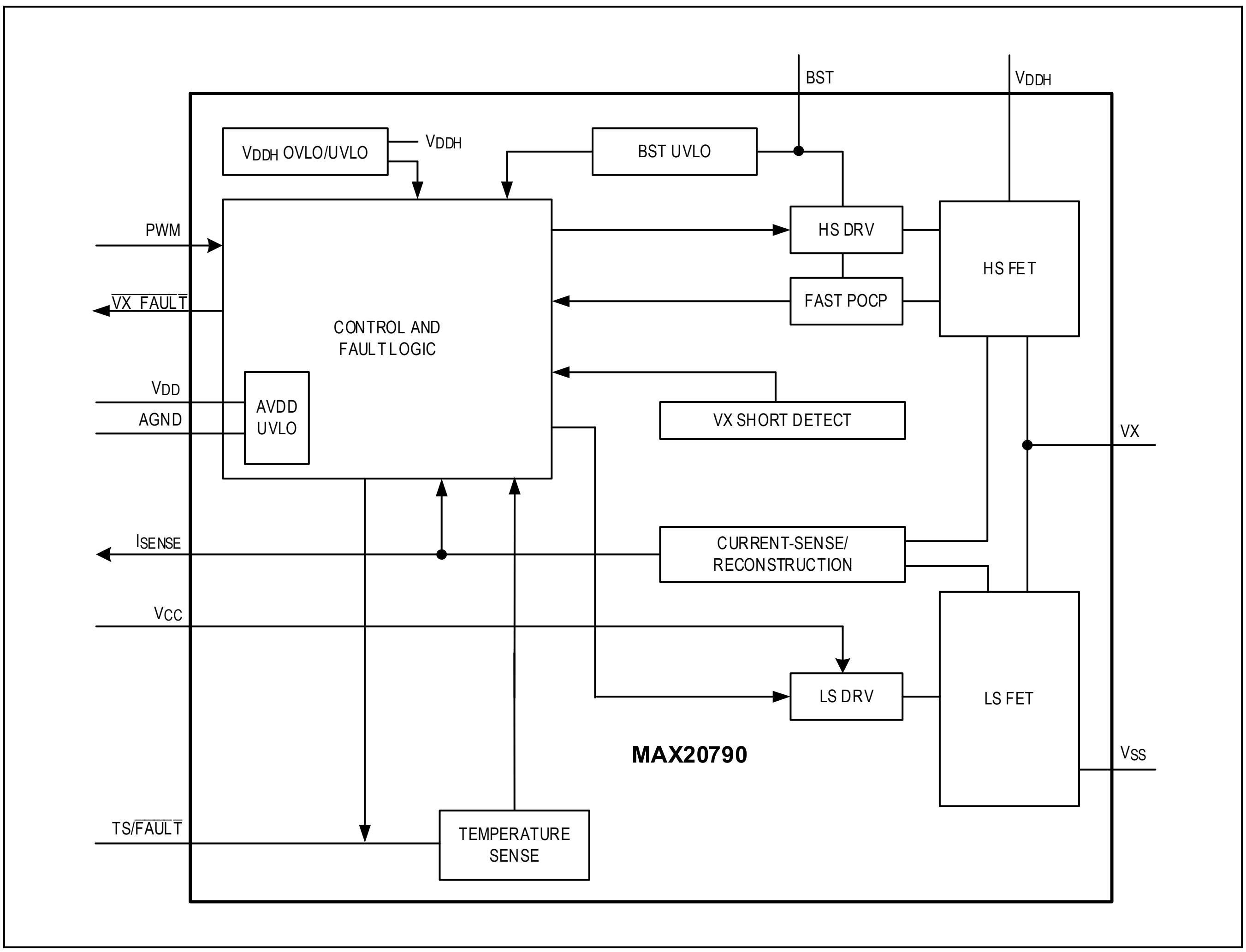
Pin Description

PIN	NAME	FUNCTION
1–2	VX	Switching Node. Connect to the switching node of the output inductor.
3	BST	Boost Supply Input. Connect a 0.68µF ceramic capacitor placed on the same side and 40 mils or closer to the IC between BST and VX.
4	$\overline{\text{VX\_FAULT}}$	VX_FAULT Open-Drain Output. Use this signal to disconnect the V_{DDH} input supply from the IC to prevent exothermic events.
5	PWM	PWM Input. Connect to the appropriate PWM output of the controller. PWM Logic Levels: - High: High-Side (HS) FET on, Low-Side (LS) FET off - Mid: Diode emulation mode; both FETs are off when the current reaches zero - Low: LS FET on, HS FET off
6	TS/$\overline{\text{FAULT}}$	Smart Power-Stage Temperature and Fault Output. This dual-function pin is used to report the junction temperature and to communicate a fault condition to the controller. See the *Fault Detection and Fault_ID Communication* section for the fault communication description. The junction temperature is calculated as shown below: $T_J = (V_{TS/\overline{FAULT}} - V_{TS/\overline{FAULT}, 0°C})/A_{TEMP}$ $= (V_{TS/\overline{FAULT}} - 821mV)/(3.0835mV/°C)$ Connect TS/$\overline{\text{FAULT}}$ to the appropriate TSENSE input of the controller.
7	I_{SENSE}	Current-Sense Output. Connect to the appropriate I_{SENSE} input pin of the controller. The I_{SENSE} current is an attenuated replica of the VX current: $I_{SENSE} = I_{VX} \times 10µA/A$

Pin Description (continued)

PIN	NAME	FUNCTION
8	V_{DD}	Analog Supply Input. Connect to the bias supply provided by the controller or an external 1.8V bias supply. Connect a 0.47μF or higher ceramic capacitor in close proximity to the IC's V_{DD} and AGND pins.
9	AGND	Analog Ground. Connect to the ground plane using a single via placed 40 mils or closer to the IC.
10	V_{CC}	Gate-Drive Supply. Connect to the bias supply provided by the controller or an external 1.8V bias supply. See Table 2 for decoupling requirements.
11	V_{DDH}	Drain of High-Side Power FET. Connect to the 12V input supply. See Table 2 for decoupling requirements.
12	V_{SS}	Power Ground. Connect to the return path of the output load.

Functional Block Diagram



Detailed Description

The MAX20790 smart power-stage IC provides the control logic, drivers, monitoring circuits, and power semiconductors for a synchronous buck converterwith independent fault protection, status monitoring, and accurate lossless current sensing.

Power-Switch Control and Drivers

The smart power-stage ICs operate in conjunction with a Maxim controller. The controller configures the voltage regulator based on the number of phases detected. Switching is controlled by the proprietary command signals on the pulse-width modulation (PWM) control lines. The PWM control signal has three defined levels: high, low, and midlevel. The midlevel is used for phase-shedding and discontinuous-conduction modes (DCM).

Bias Supply Pins

An external boost capacitor is required to supply the voltage for the high-side switch drivers. V_{DD} and V_{CC} are dedicated pins for local decoupling and increased noise immunity for analog circuits.

Current-Sense Output

The integrated lossless current sense (or "current reconstruction") produces a precise ratiometric current-sense signal for both positive and negative currents, which is sent to the controller as an analog current signal. This current-sense technology provides accurate current information over load and temperature that is not affected by tolerances of passive elements such as the output inductor, resistors, and capacitors.

Phase Configuration

The ability of the controller to dynamically disable and re-enable a phase is an integral part of the Maxim controller/power-stage architecture. The controller sets the PWM control signal to midlevel to disable a phase. The same state is used to control DCM operation. When using a coupled inductor, a proprietary mode (coupled-inductor mode) can be set by the controller and communicated to the IC through the PWM control signal to minimize losses due to coupled currents in inactive phases (during operations with reduced phase count).

Low Power I_{DDQ} State

The IC enters a low-power I_{DDQ} state when all the following three signals are held low: TS/$\overline{\text{FAULT}}$, PWM and I_{SENSE}. The controller forces this state when the regulator is in the OFF state. The smart power stage exits the I_{DDQ} state when any one of the required inputs is not held low.

Fault Protection

The IC features independent fault-monitoring and protection features. TS/$\overline{\text{FAULT}}$ is pulled low when a fault occurs. The Fault_ID is subsequently communicated to the controller over the TS/$\overline{\text{FAULT}}$ line to indicate the type of fault.

Overcurrent Protection

The IC incorporates instantaneous overcurrent fault protection using a lossless peak current sense and a reconstructed valley current. This overcurrent protection is separate from the system overcurrent protection, and is intended to operate only in extreme fault conditions to protect the IC and other components. The system overcurrent protection of the controller should be set with sufficient margin below the individual smart power stage's threshold to ensure correct system operation.

For current-sourcing operation, the reconstructed valley current limit prevents the high-side FET from turning on until the current is below the POCP level, while the lossless peak current sense turns off the high-side FET if the instantaneous current exceeds the FASTPOCP_R overcurrent-protection value (see the *Electrical Characteristics* table). The FASTPOCP_R threshold is set to ensure that the maximum allowable peak current is not exceeded when using the recommended inductors. The sourcing current limiting is not considered a hard fault condition for the smart power stage; therefore, TS/$\overline{\text{FAULT}}$ is not asserted. The maximum achievable DC current per phase is given by Equation 1.

Equation 1:

$$\text{Maximum VX DC Phase Current} = \frac{I_{FASTPOCP\_R} + I_{POCP}}{2}$$

In applications where the inductor ripple is lower than the difference between FASTOCP_R and POCP, the ripple current must be considered when calculating the maximum average current per phase, as shown in Equation 2. Note that the clamping is based on a fast current sense independent of the I_{SENSE} signal. Limits shown for FASTPOCP_R and POCP in the *Electrical Characteristics* table reflect expected variations in application conditions and external component characteristics.

Equation 2:

$$\text{Maximum VX DC Phase Current} = I_{POCP} + \frac{I_{RIPPLE}}{2}$$

Note that the controller (i.e., system) overcurrent protection should be set lower than the corresponding smart power stages' maximum operating current.

For current-sinking protection, if the negative overcurrent-protection threshold is reached, the LS FET is turned off, the smart power stage limits the phase current, as shown in Equation 3, and $TS/\overline{FAULT}$ is not asserted.

Equation 3:

$$\text{Maximum VX Negative DC Phase Current} = I_{NOCP} + \frac{I_{RIPPLE}}{2}$$

V_{DD} and V_{BST} Undervoltage Lockout

The IC includes undervoltage-lockout circuits for V_{DD} and BST. For power-sequencing guidelines and operation with separate bias rails for controller and smart power stages, refer to the appropriate controller data sheet. The BST_UVLO circuit is active at all times after the initial system startup. It is not active during the initial system power-on state (before regulation is enabled) and is activated approximately 18µs after the four BST charging cycles of the initial startup sequence. If any of these UVLO circuits is tripped during operation, the MAX20790 stops switching and a fault signal ($TS/\overline{FAULT}$ pulled LOW) is sent to the controller.

V_{DDH} Undervoltage Lockout

The IC includes protection circuits that shut down the smart power stage and assert $TS/\overline{FAULT}$ if V_{DDH} is below the correct operating range. If this circuit is tripped during operation, the smart power stage stops switching and a fault signal ($TS/\overline{FAULT}$ pulled LOW) is sent to the controller.

Temperature Sensing and Overtemperature Protection

Each IC incorporates an accurate die temperature sensor. The temperature-sense signal is sent to the controller as an analog signal through the $TS/\overline{FAULT}$ pin. The actual temperature of each smart power-stage device is then made available through the controller's SMBus or PMBus interface. The junction temperature is calculated as shown in Equation 4:

Equation 4:

$$T_J = \frac{V_{TS/\overline{FAULT}} - V_{TS/\overline{FAULT},\,0°C}}{A_{TEMP}}$$

where $V_{TS/\overline{FAULT}}$ is the measured voltage on the $TS/\overline{FAULT}$ pin, and $V_{TS/\overline{FAULT},\,0°C}$ and A_{TEMP} are taken from the *Electrical Characteristics* table.

The MAX20790 also includes overtemperature protection. If the trip point is reached, the IC immediately shuts down and the fault is reported to the controller through the $TS/\overline{FAULT}$ pin.

VX Short Protection During Operation

The IC includes VX short detection to detect a local short circuit from the VX node to either V_{DDH} or V_{SS} during operation. If such a fault is detected, the smart power stage shuts down and communicates the fault to the controller through the $TS/\overline{FAULT}$ pin. The $\overline{VX\_FAULT}$ signal is also pulled low. This high-voltage open-drain $\overline{VX\_FAULT}$ signal can be used to directly disconnect an input power switch to immediately cut off the supply to V_{DDH} and prevent exothermic events.

Fault Detection and Fault_ID Communication

If a fault is detected, the smart power stage sends a signal to the controller by pulling the $TS/\overline{FAULT}$ pin to ground. Under normal conditions, the voltage on this pin is an accurate analog representation of the power-stage temperature. If a fault is detected, this pin is asserted LOW to indicate that a fault condition was detected by a smart power-stage IC. Table 1 shows the faults that result in asserting this signal. For a latching fault, the fault must be cleared and the V_{DD} power cycled to reenable the IC.

If a nonlatching fault is detected by the smart power stage, it pulls $TS/\overline{FAULT}$ low and stops switching. The smart power stage resumes switching and deasserts $TS/\overline{FAULT}$ around 37µs after the fault condition is removed. Refer to the controller data sheet for controller response to $TS/\overline{FAULT}$ asserted LOW by the smart power-stage device.

Table 1. Fault-Detection and Protection Circuits

FAULT NAME	FAULT DESCRIPTION	FAULT RESPONSE	TS/$\overline{\text{FAULT}}$	FAULT_ID
BST_UVLO	Boost Supply Undervoltage Lockout	Shutdown, Latching	Asserted	2
V_{DD}_UVLO	V_{DD} Undervoltage Lockout	Shutdown, Nonlatching	Asserted	1
V_{DDH_UVLO}	Input Supply Undervoltage Lockout	Shutdown, Nonlatching	Asserted	1
POCP (Sourcing)	Positive Overcurrent: Valley positive current limit that inhibits HS FET turn on	Cycle-by-Cycle Clamp	Not asserted	N/A
NOCP (Sinking)	Negative Overcurrent: Peak negative current threshold that disables the LS FET	Cycle-by-Cycle Clamp	Not asserted	N/A
FASTPOCP_R	Fast Positive OCP Rising: Peak positive VX current limit	Cycle-by-Cycle Clamp	Not asserted	N/A
HS_VXSHORT	HS on and VX to V_{SS} Short	Shutdown, Latching	Asserted	3
LS_VXSHORT	LS on and V_{DDH} to VX Short	Shutdown, Latching	Asserted	4*
OTP	Overtemperature Protection	Shutdown, Latching	Asserted	5

Note: **Note:** *Not reported for power-up short detection.*

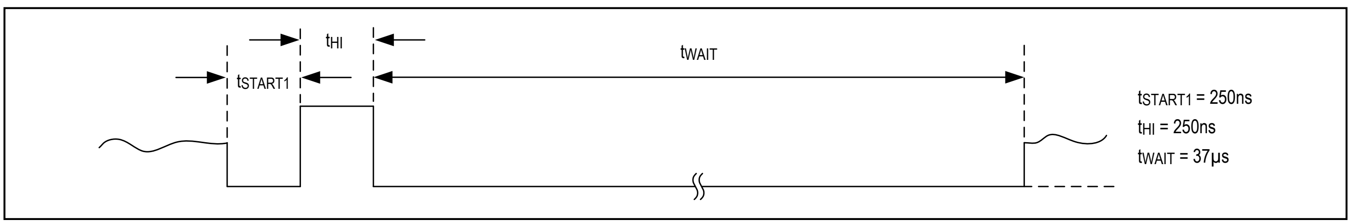


Figure 1. TS/$\overline{\text{FAULT}}$: Nonlatching Fault

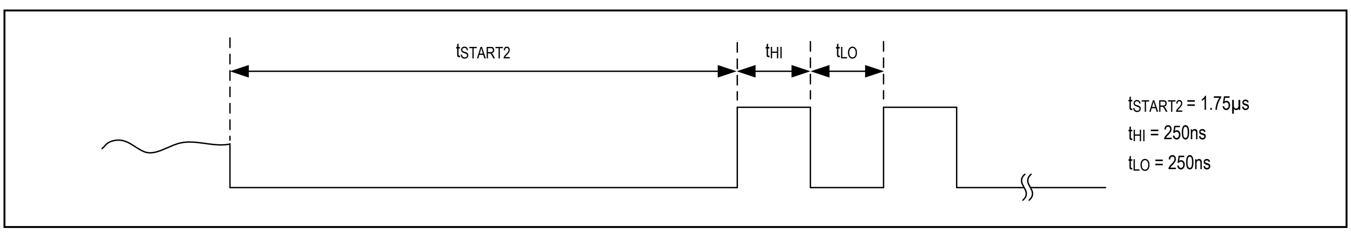


Figure 2. TS/$\overline{\text{FAULT}}$: Latching Fault without VXSHORT

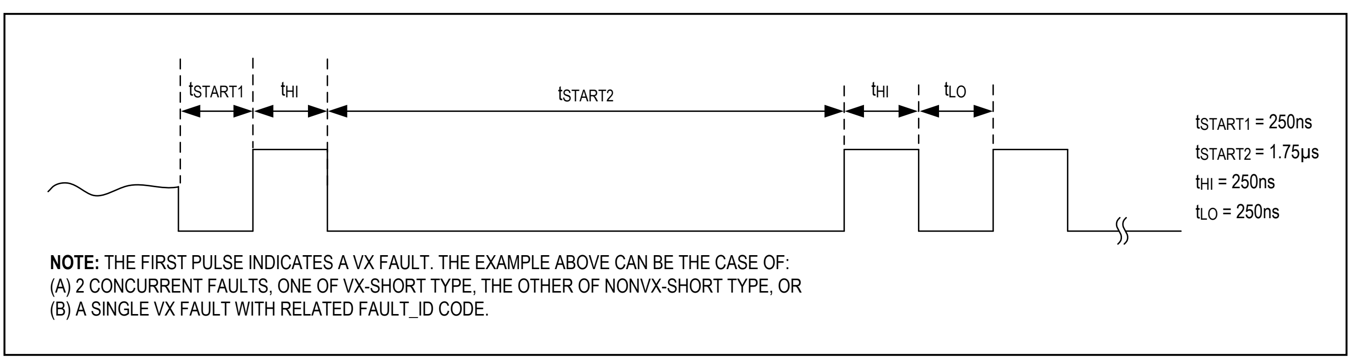


Figure 3. TS/$\overline{\text{FAULT}}$: Latching Fault with VXSHORT

Design Procedure

Phase Current Sharing and Steering Control

Maxim's controller/power-stage chipsets offer options for thermal balancing in applications where one or more phases have different thermal characteristics. The current sense and chipset regulation system offer the potential for current steering, where a percentage of current can be steered away from any phase, allowing that phase to operate at a different current than the other phases. This allows a precise scaling of current in any power stage(s) to achieve proper thermal balance between phases.

Refer to the applicable Maxim controller data sheet for more information on how to program this feature.

Thermal Path and PCB Design

The smart power-stage IC has an exposed pad on the top-side of the package that is designed as an additional thermal path. This pad is electrically connected to AGND/V_{SS}, but is not intended for use as an electrical connection. Since there is normally sufficient airflow above the regulator, conducting heat from the top of the package results in low junction-to-ambient thermal impedance; hence, a lower junction temperature. This method provides an additional thermal path to the heat flow from the die to the PCB to ambient and also reduces the temperature of the PCB. Thermal performance is presented for various thermal conditions and airflow rates in the SOA plots (see the *Typical Operating Characteristics* section).

PCB Layout

PCB layout can significantly affect the performance of the regulator. Careful attention should be paid to the location of the input and BST capacitors and output inductor, which should be placed close to the IC. The VX traces include large voltage swings (greater than 12V) with dV/dt greater than 10V/ns. It is recommended that these traces are not only kept short, but also are shielded with a ground plane immediately beneath.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative. Contact Maxim to obtain FC2QFN layout guidelines for optimal design.

High-frequency capacitors are chosen based on their impedance vs. frequency characteristics. The right capacitor should have low impedance at the VX ringing frequency. Place these on the same side as the IC, 40 mils or closer to the V_{DDH} pin, and not more than 60 mils away. Typical mid-frequency and bulk capacitors provide the required decoupling at mid and low frequencies. These are placed after the HF capacitors, or on the opposite side of the PCB. BST capacitors should be placed on the same side of IC as well, 40 mils or closer to the BST and VX pins, and not more than 60 mils away.

VX Voltage Spike and Derating

Parasitic inductance in the switching power path causes voltage spikes on VX during a low-to-high transition. Close placement of HF capacitors to the IC pins with adequate routing and vias keep the parasitic inductance low. Contact Maxim to obtain FC2QFN layout guidelines for optimal design.

Equation 5:

$$EVS_{SPIKE} = VX(\text{Abs Max}) \times I(\text{Peak VX Current}) \times 25\text{ns}$$

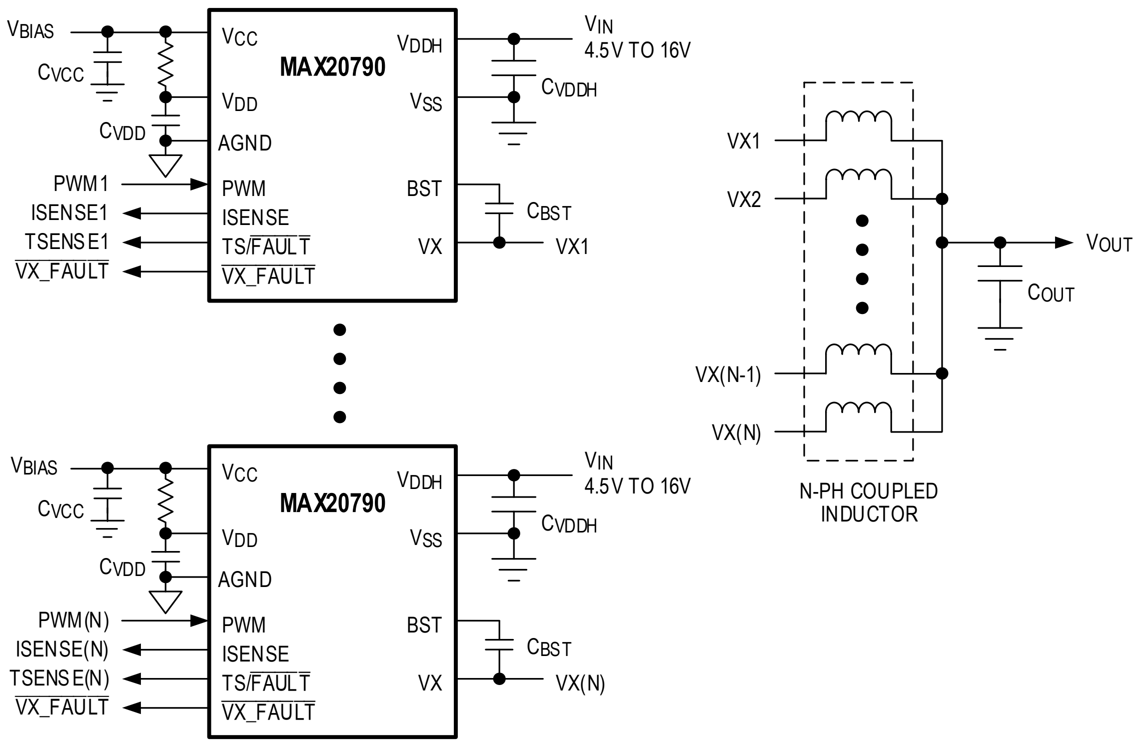
where VX(Abs Max) and I(Peak VX Current) are from the *Absolute Maximum Ratings* section.

Following recommended component selection, placement, and board layout, the voltage spike duration is typically only a few nanoseconds. There is still at least 80% derating if the voltage spike duration is as long as 20ns.

Table 2. Typical Boost-, Filtering-, and Decoupling-Capacitor Requirements

DESCRIPTION	VALUE	TYPE	PACKAGE	QUANTITY	
				IC SIDE	OTHER SIDE
V_{DD} Capacitor	0.47µF, 6.3V	X7R, +125°C	0402	0	1
V_{CC} Capacitor	1µF, 6.3V	X7R, +125°C	0402	1	1
Boost Capacitor	0.68µF, 6.3V	X7R, +125°C	0402	1	0
V_{DD} Filter Resistor	10Ω	1/16W 1%	0402	0	1
V_{DDH} HF Capacitor	4.7nF, 50V	X7R, +125°C	0603	1	0
V_{DDH} HF Capacitor	4.7nF, 50V	X7R, +125°C	0402	2	0
V_{DDH} MF Capacitor	1µF, 25V	X7R, +125°C	0603	0	2
V_{DDH} Bulk Capacitor	10µF, 25V	X5R	0805	0	1

Typical Multiphase Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20790GFC+	-40°C to +125°C	12 FC2QFN
MAX20790GFC+T	-40°C to +125°C	12 FC2QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/20	Initial release	—
1	4/21	Updated *Absolute Maximum Ratings*, *Typical Operating Characteristics*, *Pin Description* table, and *Typical Multiphase Application Circuit*	2, 6, 7, 13