DLP471TE 0.47 4K UHD DMD

1 Features

- 0.47-Inch diagonal micromirror array
  - 4K UHD (3840 × 2160) display resolution
  - 5.4-µm micromirror pitch
  - ±17° micromirror tilt (relative to flat surface)
  - Bottom illumination
- High Speed Serial Interface (HSSI) input data bus
- Supports 4K UHD at 60 Hz and full HD at 240 Hz
- Laser-phosphor, LED, RGB laser and lamp operation supported by DLPC7540 display controller, DLPA100 power management and motor driver IC

2 Applications

- Smart projector
- Enterprise projector
- Laser TV

3 Description

The DLP471TE digital micromirror device (DMD) is a digitally controlled micro-electromechanical system (MEMS) spatial light modulator (SLM) that enables bright 4K UHD display systems. The TI DLP® Products 0.47” 4K UHD chipset is composed of the DMD, DLPC7540 display controller, and DLPA100 Power and motor driver. The compact physical size of the chipset provides a complete system solution that enables small form factor 4K UHD displays.

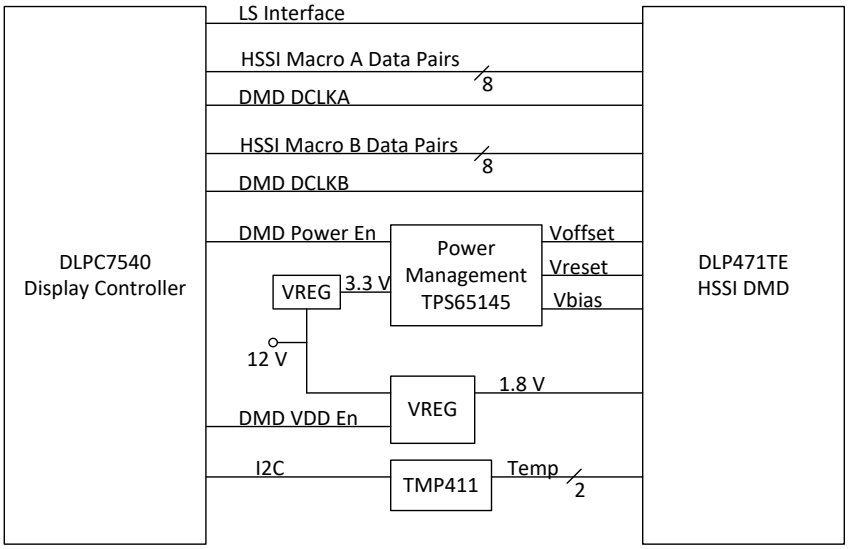
The DMD ecosystem includes established resources to help the user accelerate the design cycle, which include production ready optical modules, optical module manufacturers, and design houses.

Visit the Getting Started with TI DLP display technology page to learn more about how to start designing with the DMD.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP471TE	FYN (149)	32.2 mm × 22.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2021) to Revision B (April 2022)	Page
• Updated the definition of t_{DELAY2} and corrected a typo in t_{DELAY3} units in Table 9-1	33
• Updated Figure 9-1	33

Changes from Revision * (September 2020) to Revision A (June 2021)	Page
• Updated minimum value of | V_{ID} | CLK Recommended Operating Conditions	7
• Updated ILL_{UV} value and wavelength range in Recommended Operating Conditions	7
• Updated table header with package information in Section 6.5	9
• Corrected typo in Figure 6-8	12
• Update table in Section 6.12	20
• Corrected typo in Section 7.2	21
• Corrected typo in Section 7.7.4	25
• Added pin connection conditions for when the temp sensor is not used in Section 8.3.	31
• Merged Table 9-1 and Table 9-2 into a new Table 9-1	33
• Updated table references to reflect Table 9-2 was merged into Table 9-1 in Section 9.1	33
• Updated table references to reflect Table 9-2 was merged into Table 9-1 and fixed typos in Section 9.2	33
• Updated Figure 9-1	33

5 Pin Configuration and Functions

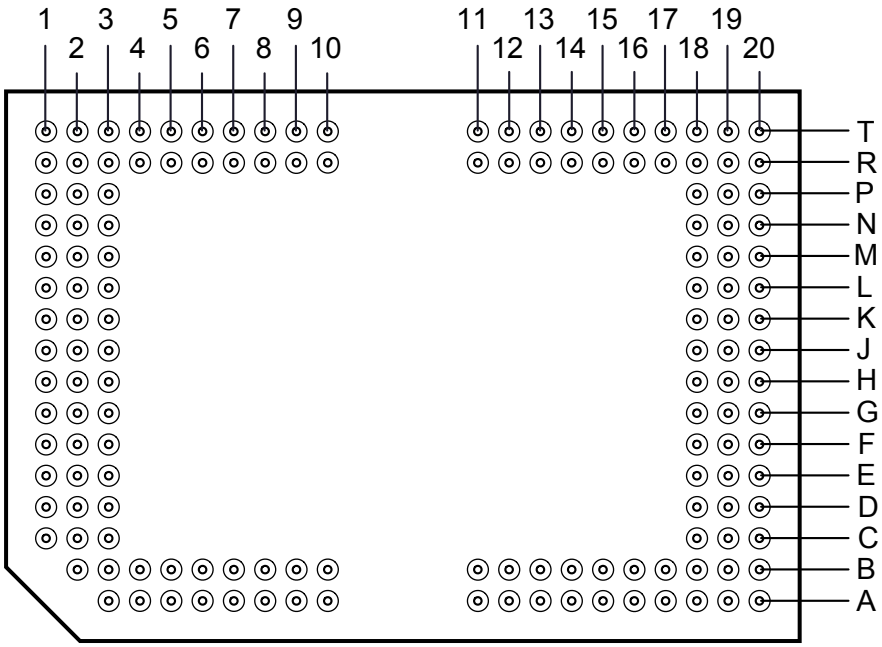


Figure 5-1. FYN Package 149-Pin PGA Bottom View

CAUTION

Properly manage the layout and the operation of signals identified in the Pin Functions table to make sure there is reliable, long-term operation of the .47" 4K UHD S451 DMD. Refer to the *PCB Design Requirements for TI DLP TRP Digital Micromirror Devices* application report for specific details and guidelines before designing the board.

Table 5-1. Pin Functions

PIN		INPUT-OUTPUT(1)	DESCRIPTION	TRACE LENGTH (mm)
NAME	No.			
D_AP(0)	J1	I	High-speed differential data pair lane A0	16.24427
D_AN(0)	H1	I	High-speed differential data pair lane A0	16.24426
D_AP(1)	G1	I	High-speed differential data pair lane A1	16.39699
D_AN(1)	F1	I	High-speed differential data pair lane A1	16.39691
D_AP(2)	F2	I	High-speed differential data pair lane A2	15.58905
D_AN(2)	E2	I	High-speed differential data pair lane A2	15.58908
D_AP(3)	D2	I	High-speed differential data pair lane A3	14.98471
D_AN(3)	C2	I	High-speed differential data pair lane A3	14.9844
D_AP(4)	A3	I	High-speed differential data pair lane A4	12.89101
D_AN(4)	A4	I	High-speed differential data pair lane A4	12.89101
D_AP(5)	A5	I	High-speed differential data pair lane A5	10.57206
D_AN(5)	A6	I	High-speed differential data pair lane A5	10.57242
D_AP(6)	A7	I	High-speed differential data pair lane A6	8.48593
D_AN(6)	A8	I	High-speed differential data pair lane A6	8.48702
D_AP(7)	A9	I	High-speed differential data pair lane A7	6.63434
D_AN(7)	A10	I	High-speed differential data pair lane A7	6.63441

Table 5-1. Pin Functions (continued)

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TRACE LENGTH (mm)
NAME	No.			
DCLK_AP	C1	I	High-speed differential clock A	15.53899
DCLK_AN	D1	I	High-speed differential clock A	15.53868
D_BP(0)	A11	I	High-speed differential data pair lane B0	4.52398
D_BN(0)	A12	I	High-speed differential data pair lane B0	4.52368
D_BP(1)	A13	I	High-speed differential data pair lane B1	6.4103
D_BN(1)	A14	I	High-speed differential data pair lane B1	6.40894
D_BP(2)	A15	I	High-speed differential data pair lane B2	8.78102
D_BN(2)	A16	I	High-speed differential data pair lane B2	8.78364
D_BP(3)	A18	I	High-speed differential data pair lane B3	12.05827
D_BN(3)	A19	I	High-speed differential data pair lane B3	12.06154
D_BP(4)	D19	I	High-speed differential data pair lane B4	11.04817
D_BN(4)	C19	I	High-speed differential data pair lane B4	11.0479
D_BP(5)	H20	I	High-speed differential data pair lane B5	14.54976
D_BN(5)	J20	I	High-speed differential data pair lane B5	14.54991
D_BP(6)	D20	I	High-speed differential data pair lane B6	11.67363
D_BN(6)	E20	I	High-speed differential data pair lane B6	11.67598
D_BP(7)	F20	I	High-speed differential data pair lane B7	12.33442
D_BN(7)	G20	I	High-speed differential data pair lane B7	12.33409
DCLK_BP	B17	I	High-speed differential clock B	10.22973
DCLK_BN	B18	I	High-speed differential clock B	10.22551
LS_WDATA_P	T10	I	LVDS data	7.8047
LS_WDATA_N	R11	I	LVDS data	0.64391
LS_CLK_P	R9	I	LVDS CLK	8.20952
LS_CLK_N	R10	I	LVDS CLK	7.35885
LS_RDATA_A_BISTA	T13	O	LVCMOS output	2.01174
BIST_B	T12	O	LVCMOS output	2.20006
AMUX_OUT	B20	O	Analog test mux	10.74435
DMUX_OUT	R14	O	Digital test mux	2.25459
DMD_DEN_ARSTZ	T11	I	ARSTZ	2.00365
TEMP_N	R8	I	Temp diode N	9.03231
TEMP_P	R7	I	Temp diode P	11.38391
VDD	B13, B7, C18, E3, H3, J2, K3, L2, L19, M1, M2, N3, N19, P2, P18, R3, R5, R12, R17, R19, T2, T4, T6, T8, T18	P	Digital Core supply voltage	Plane
VDDA	B11, B16, B4, B9, C20, D3, E18, G2, G19	P	HSSI supply voltage	Plane
VRESET	B3, R1	P	Supply voltage for negative bias of micromirror reset signal	Plane
VBIAS	E1, P1	P	Supply voltage for positive bias of micromirror reset signal	Plane
VOFFSET	A20, B2, T1, T20	P	Supply voltage for HVCMOS logic, stepped up logic level	Plane

Table 5-1. Pin Functions (continued)

PIN		INPUT-OUTPUT(1)	DESCRIPTION	TRACE LENGTH (mm)
NAME	No.			
VSS	A17, B10, B14, B6, D18, F3, F19, J3, K19, K2, L1, L3, M3, N2, N18, N20, P3, P20, R2, R4, R6, R13, R20, T5, T7, T16, T17, T19	G	Ground	Plane
VSSA	B12, B15, B19, B5, B8, C3, E19, G3, H2, H19, K1, N1, P19, R18, T3, T9	G	Ground	Plane
N/C	F18, G18, H18, J18, J19, K18, K20, L18, L20, M18, M19, M20, R15, R16, T14, T15		No connect	

(1) I=Input, O=Output, P=Power, G=Ground, NC = No Connect

6 Specifications

6.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic and LVCMOS low speed interface (LSIF)(1)	–0.5	2.3	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers(1)	–0.3	2.2	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(1) (2)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(1)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(1)	–15	0.5	V
$\lvert V_{DDA} - V_{DD} \rvert$	Supply voltage delta (absolute value)(3)		0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(4)		11	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value)(5)		34	V
INPUT VOLTAGE				
	Input voltage for other inputs – LSIF and LVCMOS(1)	–0.5	2.45	V
	Input voltage for other inputs – HSSI(1) (6)	–0.2	V_{DDA}	V
LOW SPEED INTERFACE (LSIF)				
f_{CLOCK}	LSIF clock frequency (LS_CLK)		130	MHz
$\lvert V_{ID} \rvert$	LSIF differential input voltage magnitude(6)		810	mV
I_{ID}	LSIF differential input current		10	mA
HIGH SPEED SERIAL INTERFACE (HSSI)				
f_{CLOCK}	HSSI clock frequency (DCLK)		1.65	GHz
$\lvert V_{ID} \rvert$	HSSI differential input voltage magnitude Data Lane(6)		700	mV
$\lvert V_{ID} \rvert$	HSSI differential input voltage magnitude Clock Lane(6)		700	mV
ENVIRONMENTAL				
T_{WINDOW} and T_{ARRAY}	Temperature, operating(7)	0	90	°C
	Temperature, non-operating(7)	–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(8)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDA} and V_{DD} may result in excessive current draw.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS and HSSI differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) The highest temperature of the active array (as calculated using Micromirror Array Temperature Calculation) or of any point along the window edge as defined in Figure 7-1. The locations of thermal test points TP2, TP3, TP4 and TP5 in Figure 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature, non-condensing(1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range, non-condensing(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	months

(1) The average temperature over time (including storage and operating temperatures) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES (1) (2)					
V_{DD}	Supply voltage for LVCMOS core logic and low speed interface (LSIF)	1.71	1.8	1.95	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers	1.71	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(3)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for micromirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
$\lvert V_{DDA} - V_{DD} \rvert$	Supply voltage delta, absolute value(4)			0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta, absolute value(5)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta, absolute value			33	V
LVCMOS INPUT					
V_{IH}	High level input voltage(6)	0.7 × V_{DD}			V
V_{IL}	Low level input voltage(6)			0.3 × V_{DD}	V
LOW SPEED SERIAL INTERFACE (LSIF)					
f_{CLOCK}	LSIF clock frequency (LS_CLK)(7)	108	120	130	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK)	44%		56%	
$\lvert V_{ID} \rvert$	LSIF differential input voltage magnitude(7)	150	350	440	mV
V_{LVDS}	LSIF voltage(7)	575		1520	mV
V_{CM}	Common mode voltage(7)	700	900	1300	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
HIGH SPEED SERIAL INTERFACE (HSSI)					
f_{CLOCK}	HSSI clock frequency (DCLK)(8)	1.2		1.6	GHz
DCD_{IN}	HSSI duty cycle distortion (DCLK)	44%	50%	56%	

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
$\lvert V_{ID} \rvert$ Data	HSSI differential input voltage magnitude data lane(8)	100		600	mV
$\lvert V_{ID} \rvert$ CLK	HSSI differential input voltage magnitude clock Lane(8)	295		600	mV
VCM_{DC} Data	Input common mode voltage (DC) data lane(8)	200	600	800	mV
VCM_{DC} CLK	Input common mode voltage (DC) clk lane(8)	200	600	800	mV
VCM_{ACp-p}	AC peak to peak (ripple) on common mode voltage of data lane and clock lane(8)			100	mV
Z_{LINE}	Line differential impedance (PWB/trace)		100		Ω
Z_{IN}	Internal differential termination resistance. (R_{Xterm})	80	100	120	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational(9) (10) (11) (12) (13)	10		40 to 70	°C
	Array temperature, short-term operational, 500-hr max(10) (14)	0		10	°C
T_{WINDOW}	Window temperature, operational(15)			85	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(16)			14	°C
T_{DP-AVG}	Average dew point temperature (non–condensing)(17)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(18)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	months
ILL_{θ}	Illumination marginal ray angle(19)			55	°
LAMP ILLUMINATION					
ILL_{UV}	Illumination wavelength < 395 nm(9)		0.68	2	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 395 nm and 800 nm(13)			36.8	W/cm^2
ILL_{IR}	Illumination wavelength > 800 nm			10	mW/cm^2
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination wavelength < 410 nm(9)			3	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 410 nm and 800 nm(13)			44.9	W/cm2
ILL_{IR}	Illumination wavelength > 800 nm			10	mW/cm^2

(1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the V_{SS} ground pins.
(3) V_{OFFSET} supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta $\lvert V_{DDA} - V_{DD} \rvert$ must be less than specified limit.
(5) To prevent excess current, the supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than specified limit.
(6) LVCMOS input pin is DMD_DEN_ARSTZ.
(7) See the low speed interface (LSIF) timing requirements in *Timing Requirements*.
(8) See the high speed serial interface (HSSI) timing requirements in *Timing Requirements*.
(9) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination reduces device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 7-1 and the package thermal resistance using the *Micromirror Array Temperature Calculation*.
(11) Per Figure 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(12) Long-term is defined as the usable life of the device.
(13) The maximum optical power that can be incident on the DMD is limited by the maximum optical power density and the micromirror array temperature
(14) Short-term is the total cumulative time over the useful life of the device.
(15) The locations of thermal test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.

(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.
(17) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(18) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(19) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including pond of micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

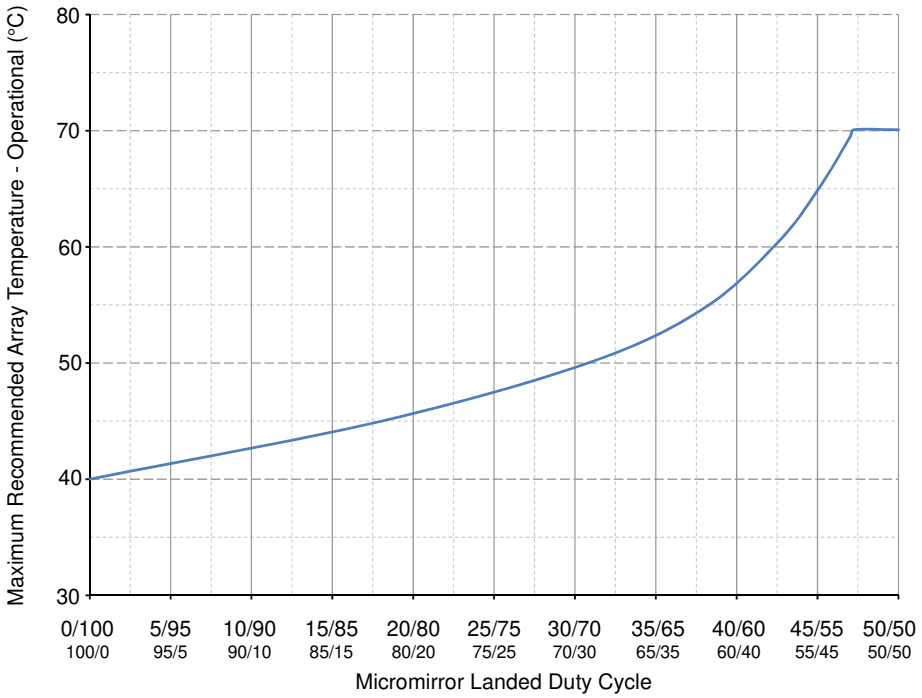


Figure 6-1. Maximum Recommended Array Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP471TE FYN PACKAGE 149 PINS	Unit
Thermal Resistance, active area to test point 1 (TP1)(1)	0.8	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the *Recommended Operating Conditions* . The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER (1) (2)		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
CURRENT – TYPICAL						
I_{DD}	Supply current V_{DD} (3)			800	1200	mA
I_{DDA}	Supply current V_{DDA} (3)			1000	1200	mA
I_{DDA}	Supply current V_{DDA} (3)	Single macro mode		500	600	mA

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER (1) (2)		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
I_{OFFSET}	Supply current V_{OFFSET} (4) (5)			20	25	mA
I_{BIAS}	Supply current V_{BIAS} (4) (5)			2.5	4.0	mA
I_{RESET}	Supply current V_{RESET} (5)		-9.3	-6.9		mA
POWER – TYPICAL						
P_{DD}	Supply power dissipation V_{DD} (3)			1440	2437.5	mW
P_{DDA}	Supply power dissipation V_{DDA} (3)			1620	2340	mW
P_{DDA}	Supply power dissipation V_{DDA} (3)	single macro mode		900	1170	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} (4) (5)			230	367.5	mW
P_{BIAS}	Supply power dissipation V_{BIAS} (4) (5)			43.2	70.3	mW
P_{RESET}	Supply power dissipation V_{RESET} (5)			107.8	152.25	mW
P_{TOTAL}	Supply power dissipation Total			3441	5367.55	mW
LVCMOS INPUT						
I_{IL}	Low level input current (6)	V_{DD} = 1.95 V, V_I = 0 V	–100			nA
I_{IH}	High level input current (6)	V_{DD} = 1.95 V, V_I = 1.95 V			135	µA
LVCMOS OUTPUT						
V_{OH}	DC output high voltage (7)	I_{OH} = -2 mA	0.8 x V_{DD}			V
V_{OL}	DC output low voltage (7)	I_{OL} = 2 mA			0.2 x V_{DD}	V
RECEIVER EYE CHARACTERISTICS						
A1	Minimum data eye opening (8) (9)		100		600	mV
	Minimum clock eye opening (8) (9)		295		600	mV
A2	Maximum data signal swing (8) (9)				600	mV
X1	Maximum data eye closure (8)				0.275	UI
X2	Maximum data eye closure (8)				0.4	UI
$\lvert t_{DRIFT} \rvert$	Drift between Clock and Data between Training Patterns				20	ps
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	f = 1 MHz			10	pF
C_{IN}	Input capacitance LSIF (low speed interface)	f = 1 MHz			20	pF
C_{IN}	Input capacitance HSSI (high speed serial interface)	f = 1 MHz			20	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF

(1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta $\lvert V_{DDA} - V_{DD} \rvert$ must be less than specified limit.
(4) To prevent excess current, the supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than specified limit.
(5) Supply power dissipation based on 3 global resets in 200 µs.
(6) LVCMOS input specifications are for pin DMD_DEN_ARSTZ.
(7) LVCMOS output specification is for pins LS_RDATA_A and LS_RDATA_B.
(8) Refer to Figure 6-11, Receiver Eye Mask (1e-12 BER).
(9) Defined in the *Recommended Operating Conditions*.

6.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Output propagation, Clock to Q (C2Q), rising edge of LS_CLK (differential clock signal) input to LS_RDATA output.(1)	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
	Slew rate, LS_RDATA	20%–80%, C_L <10 pF	0.5			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B	50–(C2Q rise – C2Q fall) × 130e6 × 100	40%		60%	

(1) See Figure 6-2.

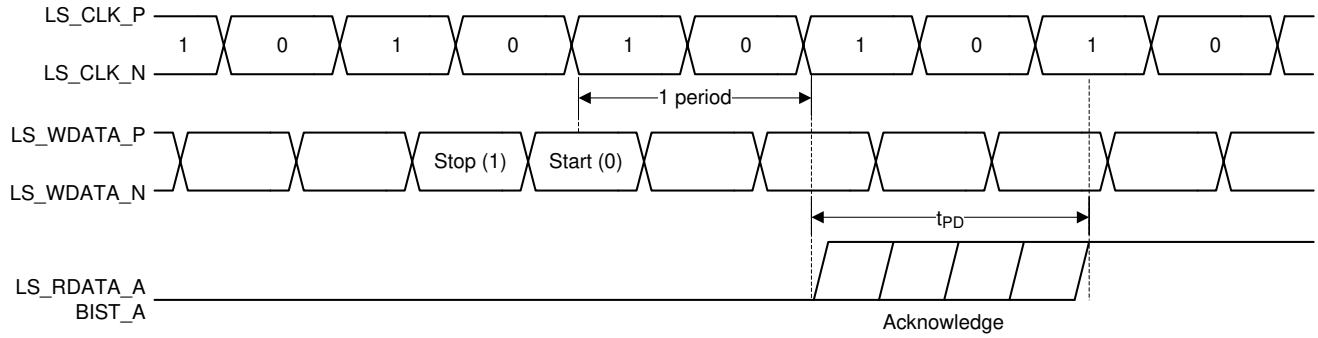


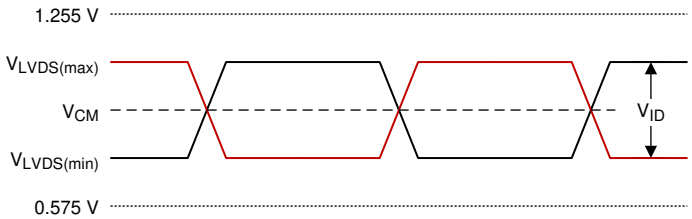
Figure 6-2. Switching Characteristics

6.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS						
t_r	Rise time(1)	20% to 80% reference points			25	ns
t_f	Fall time(1)	80% to 20% reference points			25	ns
LOW SPEED INTERFACE (LSIF)						
t_r	Rise time(2)	20% to 80% reference points			450	ps
t_f	Fall time(2)	80% to 20% reference points			450	ps
$t_{W(H)}$	Pulse duration high(3)	LS_CLK. 50% to 50% reference points	3.1			ns
$t_{W(L)}$	Pulse duration low(3)	LS_CLK. 50% to 50% reference points	3.1			ns
t_{su}	Setup time(4)	LS_WDATA valid before rising edge of LS_CLK (differential)			1.5	ns
t_h	Hold time(4)	LS_WDATA valid after rising edge of LS_CLK (differential)			1.5	ns
HIGH SPEED SERIAL INTERFACE (HSSI)						
t_r	Rise time(5) (6)—data	from -A1 to A1 minimum eye height specification	50		115	ps
	Rise time(5) (6)—clock	rom -A1 to A1 minimum eye height specification	50		135	ps
t_f	Fall time(5) (6)—data	from A1 to -A1 minimum eye height specification	50		115	ps
	Fall time(5) (6)—clock	from A1 to -A1 minimum eye height specification	50		135	
$t_{W(H)}$	Pulse duration high(7)	DCLK. 50% to 50% reference points	0.275			ns
$t_{W(L)}$	Pulse duration low(7)	DCLK. 50% to 50% reference points	0.275			ns

(1) See Figure 6-9 for rise time and fall time for LVCMOS.
(2) See Figure 6-5 for rise time and fall time for LSIF.
(3) See Figure 6-4 for pulse duration high and low time for LSIF.
(4) See Figure 6-4 for setup and hold time for LSIF.
(5) See Figure 6-11 for rise time and fall time for HSSI Eye Characteristics.
(6) See Figure 6-10 for rise time and fall time for HSSI.
(7) See Figure 6-12 for pulse duration high and low for HSSI.



A. See Equation 1 and Equation 2.

Figure 6-3. LSIF Waveform Requirements

$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (1)$$

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (2)$$

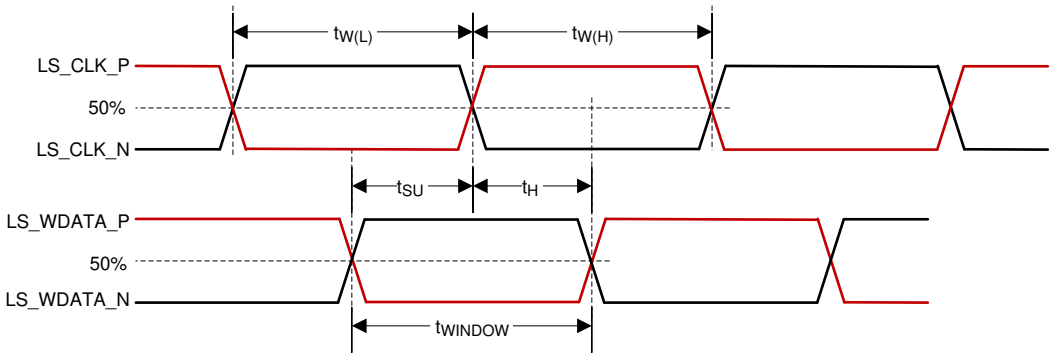


Figure 6-4. LSIF Timing Requirements

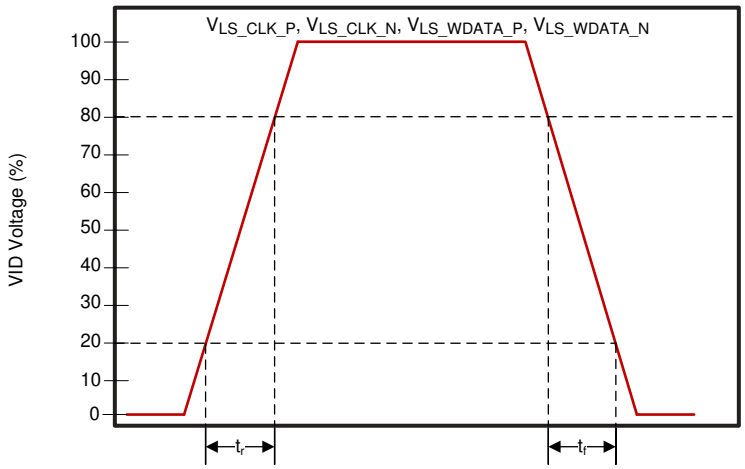


Figure 6-5. LSIF Rise, Fall Time Slew

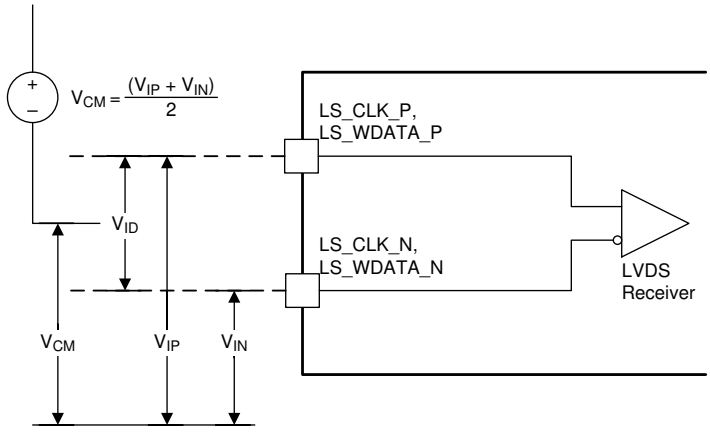


Figure 6-6. LSIF Voltage Requirements

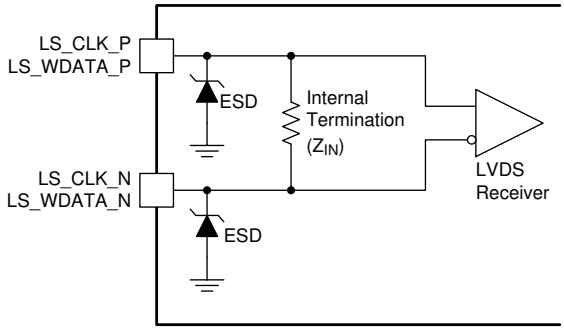


Figure 6-7. LSIF Equivalent Input

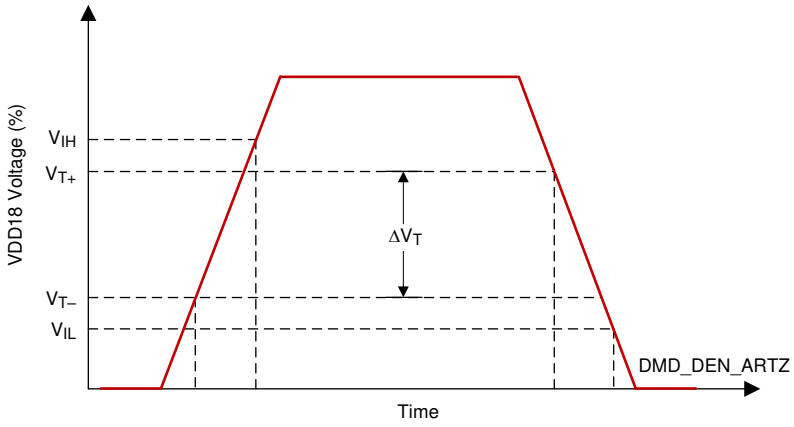


Figure 6-8. LVCMOS Input Hysteresis

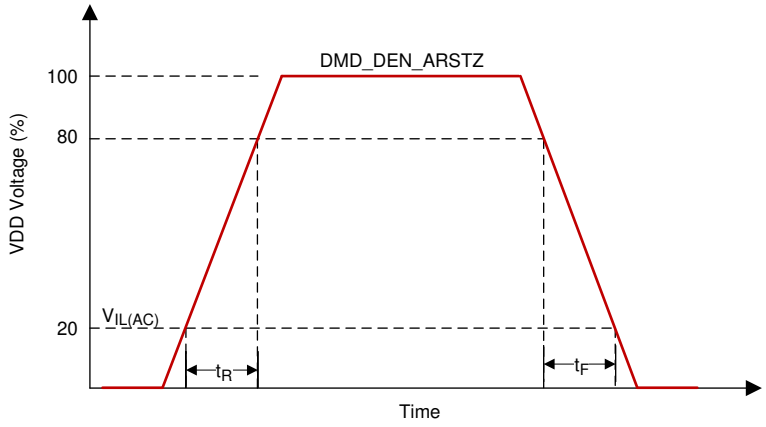
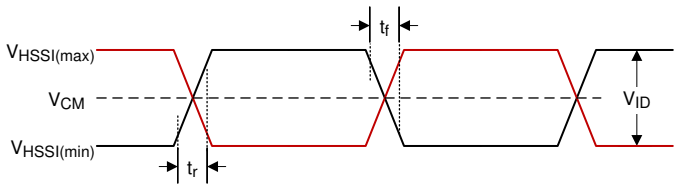


Figure 6-9. LVCMOS Rise, Fall Time Slew Rate



A. See Equation 1 and Equation 2.

Figure 6-10. HSSI Waveform Requirements

$$V_{HSSI\,(max\,)} = V_{CM\,(max\,)} + \left|\frac{1}{2} \times V_{ID\,(max\,)}\right| \quad (3)$$

$$V_{HSSI\,(min\,)} = V_{CM\,(min\,)} - \left|\frac{1}{2} \times V_{ID\,(max\,)}\right| \quad (4)$$

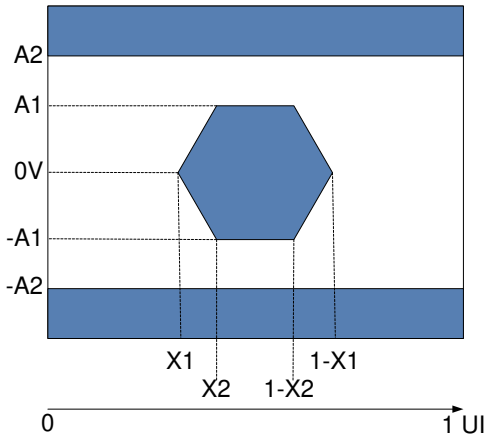


Figure 6-11. HSSI Eye Characteristics

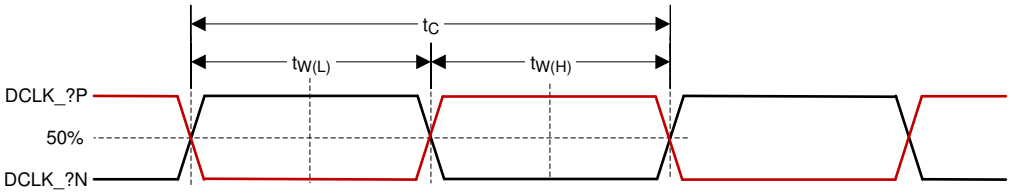


Figure 6-12. HSSI CLK Characteristics

6.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
When loads are applied to the electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area(1)			111	N
Maximum load to be applied to the thermal interface area(1)			111	N
When a load is applied to only the electrical interface area				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) The load should be uniformly applied in the corresponding areas shown in Figure 6-13.

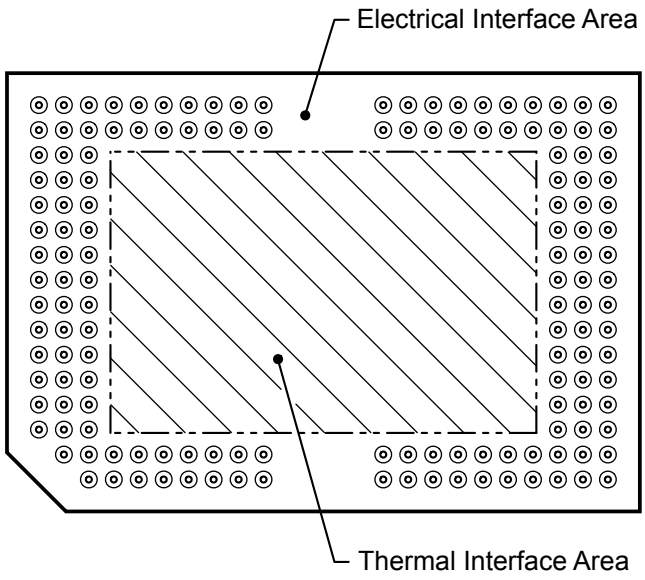


Figure 6-13. System Mounting Interface Loads

6.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns(1) (2)	M	1920	micromirrors
Number of active rows(1) (2)	N	1080	micromirrors
Micromirror (pixel) pitch (1)	P	5.4	µm
Micromirror active array width(1)	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height(1)	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border(3)	Pond of micromirror (POM)	20	micromirrors/side

(1) See Figure 6-14.
(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed.
(3) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the *Pond Of Micromirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

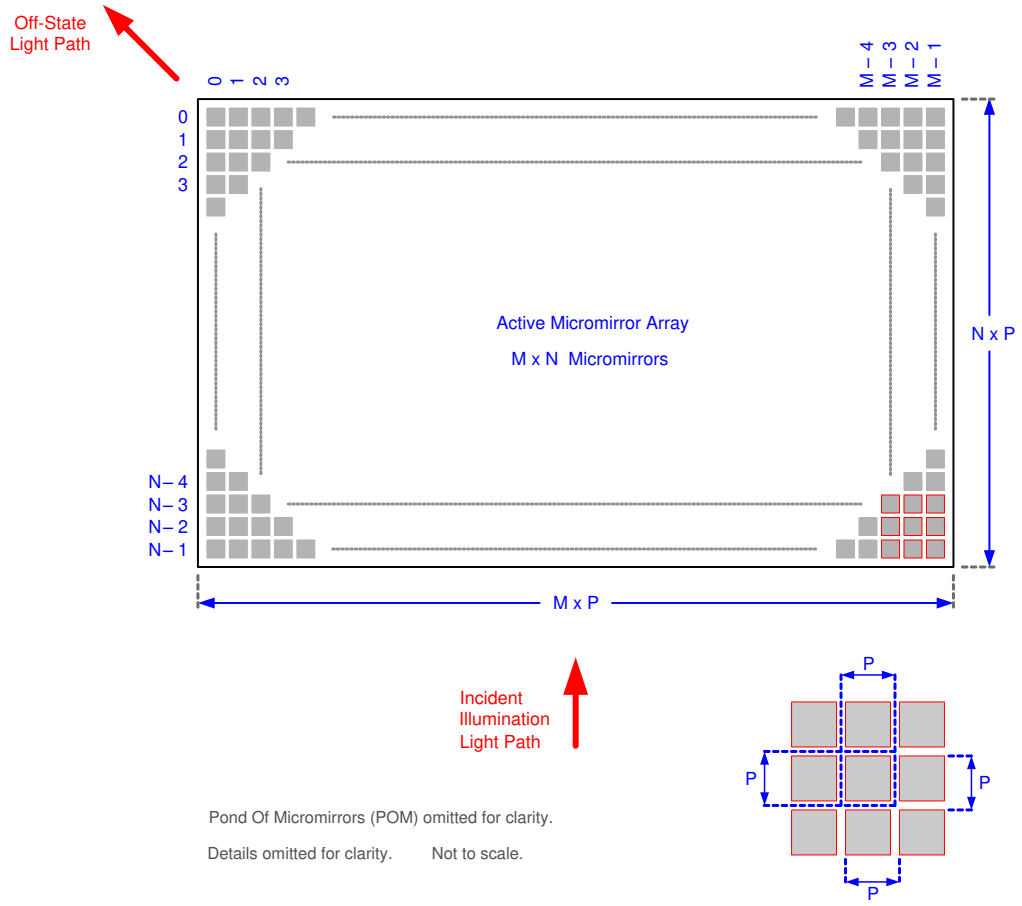


Figure 6-14. Micromirror Array Physical Characteristics

6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle (1) (2) (3) (4)		Landed state	15.6		18.4	degrees
Micromirror crossover time (5)		Typical performance		1	3	µs
Micromirror switching time (6)		Typical performance	6			
Image performance(7)	Bright pixel(s) in active area (8)	Gray 10 Screen (9)			0	micromirrors
	Bright pixel(s) in the POM (10)	Gray 10 Screen (9)			1	
	Dark pixel(s) in the active area (11)	White Screen			4	
	Adjacent pixel(s) (12)	Any Screen			0	
	Unstable pixel(s) in active area (13)	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(3) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(4) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction. See Figure 6-15.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(6) The minimum time between successive transitions of a micromirror.
(7) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear.
Test set brightness and contrast shall be set to nominal.
The diagonal size of the projected image shall be a minimum of 60 inches.
The projections screen shall be 1X gain.
The projected image shall be inspected from a 8 foot minimum viewing distance.
The image shall be in focus during all image quality tests.
(8) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
(9) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(10) POM definition: Rectangular border of off-state mirrors surrounding the active area.
(11) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

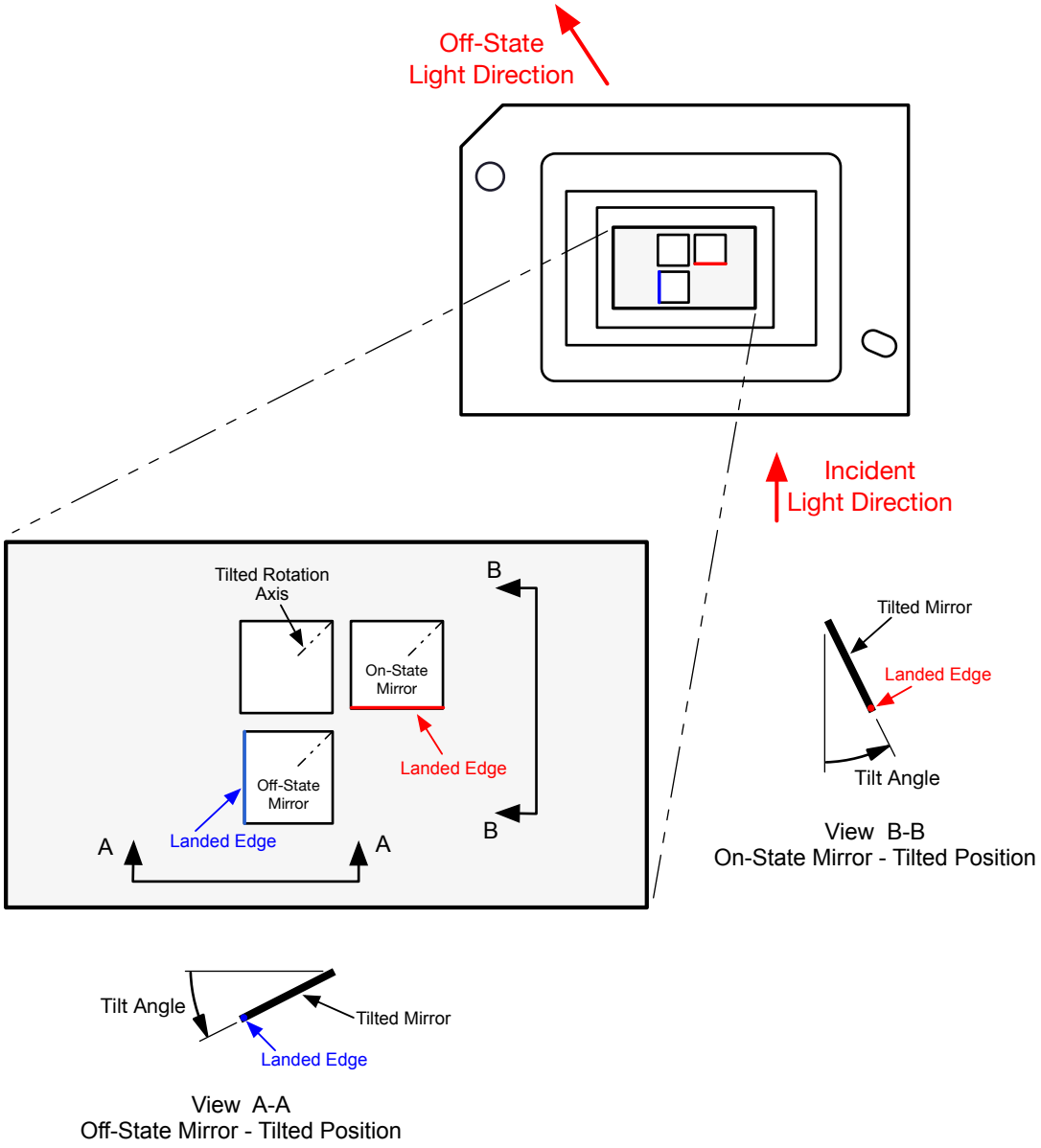


Figure 6-15. Micromirror Landed Orientation and Tilt

6.12 Window Characteristics

DESCRIPTION[1]		MIN	TYP	MAX
Window material			Corning Eagle XG	
Window refractive index	At wavelength 546.1 nm		1.5119	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI [2]	97%		
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI [2]	97%		

(1) See Section 7.5 for more information.
(2) Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP471TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

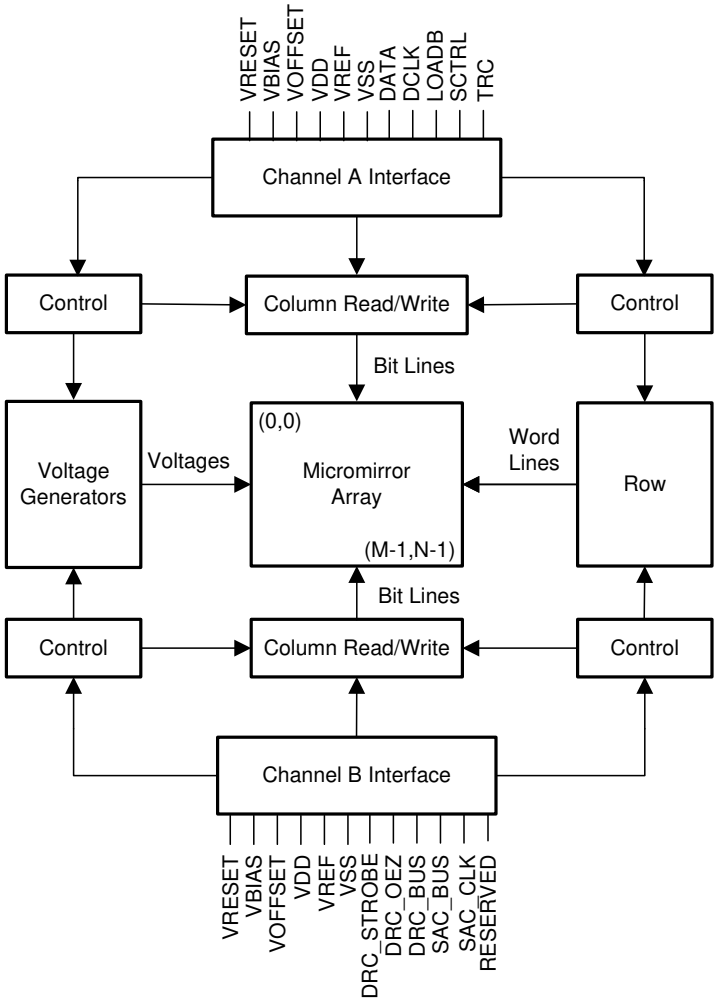
7 Detailed Description

7.1 Overview

The DMD is a 0.47-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the *Functional Block Diagram*. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.47” 4K UHD chipset is comprised of the DLP471TE DMD, DLPC7540 display controller and the DLPA100 power management and motor driver. To ensure reliable operation, the DLP471TE DMD must always be used with the DLP display controller and the power management and motor driver specified in the chipset.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Power Interface

The DMD requires 4 DC voltages: 1.8 V source, V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical configuration, 3.3 V is created by the DLPA100 power management and motor driver and is used on the DMD board to create the 1.8 V. The TI voltage regulator TPS65145 takes in the 3.3 V and outputs V_{OFFSET}, V_{RESET}, V_{BIAS}.

7.3.2 Timing

The data sheet specifies timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC7540 display controller. See the DLPC7540 display controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

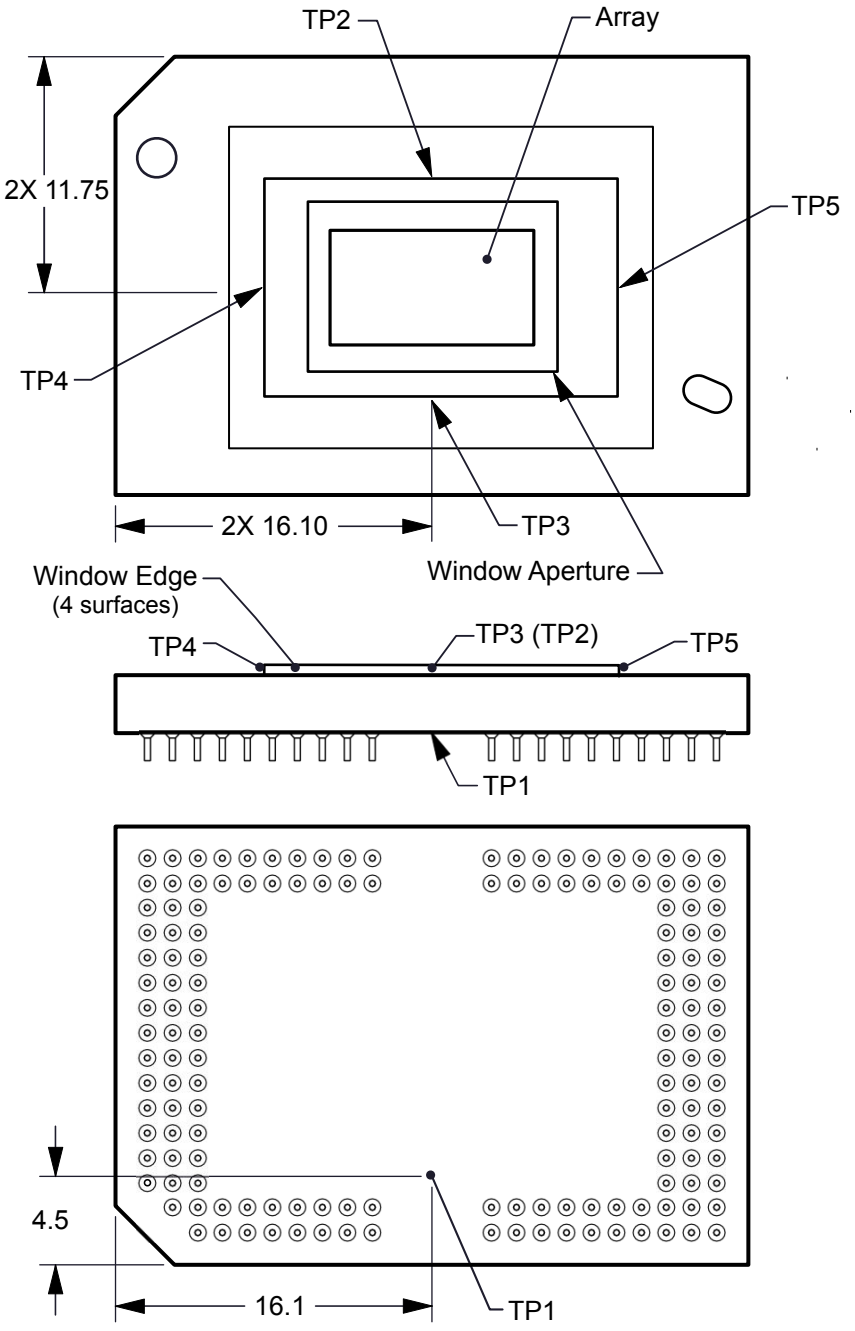


Figure 7-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in Figure 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (5)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (6)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in *Thermal Information* from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.40

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 2.5 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multi-chip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 25 \text{ W (measured)} \quad (7)$$

$$T_{CERAMIC} = 55.0°C \text{ (measured)} \quad (8)$$

$$Q_{ELECTRICAL} = 2.5 \text{ W} \quad (9)$$

$$Q_{ARRAY} = 2.5 \text{ W} + (0.40 \times 25 \text{ W}) = 12.5 \text{ W} \quad (10)$$

$$T_{ARRAY} = 55.0°C + (12.5 \text{ W} \times 0.8°C/W) = 65.0°C \quad (11)$$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the de-rating curve shown in Figure 6-1. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in Table 7-1.

Table 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use Equation 12 to calculate the landed duty cycle of a given pixel during a given time period

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (12)$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in Table 7-2 and Table 7-3.

Table 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
30%	50%	20%

Table 7-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	30/70
0%	100%	0%	50/50
0%	0%	100%	20/80
0%	12%	0%	6/94
0%	0%	35%	7/93
60%	0%	0%	18/82
0%	100%	100%	70/30
100%	0%	100%	50/50
100%	100%	0%	80/20
0%	12%	35%	13/87
60%	0%	35%	25/75
60%	12%	0%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC7540 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC7540 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 7-2.

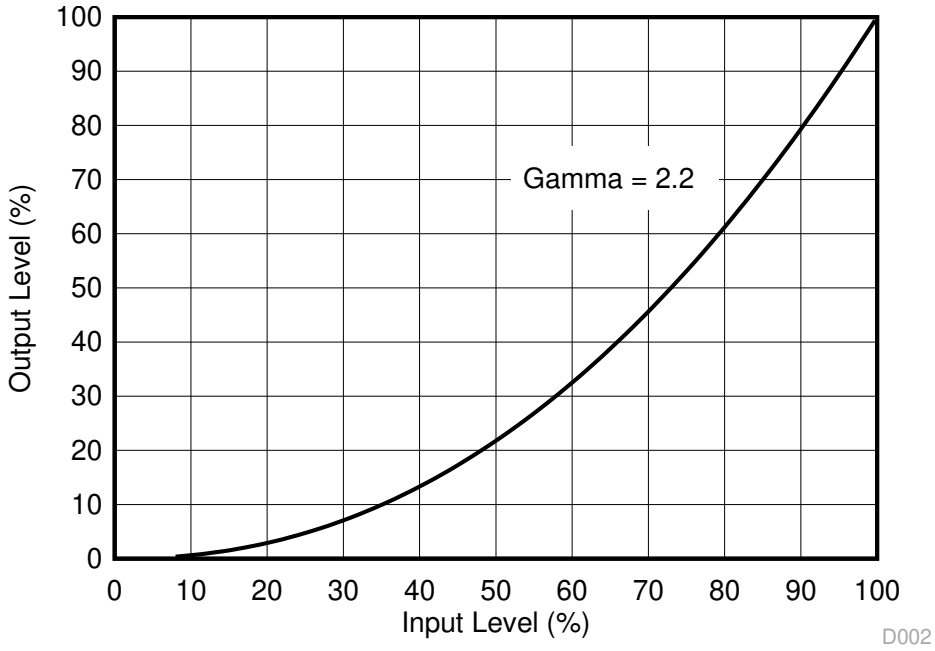


Figure 7-2. Example of Gamma = 2.2

From Figure 7-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing which occurs before the DLPC7540 controllers.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC7540 controller. The high tilt pixel in the bottom-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness constrained applications. Typical applications using the DLP471TE include Laser TVs and enterprise projectors.

DMD power-up and power-down sequencing is strictly controlled by the DLPC7540 through the TPS65145 PMIC. Refer to Section 9 for power-up and power-down specifications. To ensure reliable operation, the DLP471TE DMD must always be used with DLPC7540 controller, a DLPA100 PMIC/Motor driver and aTPS65145 PMIC.

8.2 Typical Application

The DLP471TE DMD combined with DLPC7540 digital controller and a power management device provides full 4K UHD resolution for bright, colorful display applications. A typical display system using laser phosphor illumination combines the DLP471TE DMD, DLPC7540 display controller, TPS65145 voltage regulator and DLPA100 PMIC and motor driver. Figure 8-1 shows a system block diagram for this configuration of the DLP 0.47" 4K UHD chipset and additional system components needed. See Figure 8-2, a block diagram showing the system components needed along with the lamp configuration of the DLP 0.47" 4K UHD chipset. The components include the DLP471TE DMD, DLPC7540 display controller and the DLPA100 PMIC and motor driver and a TPS65145 PMIC.

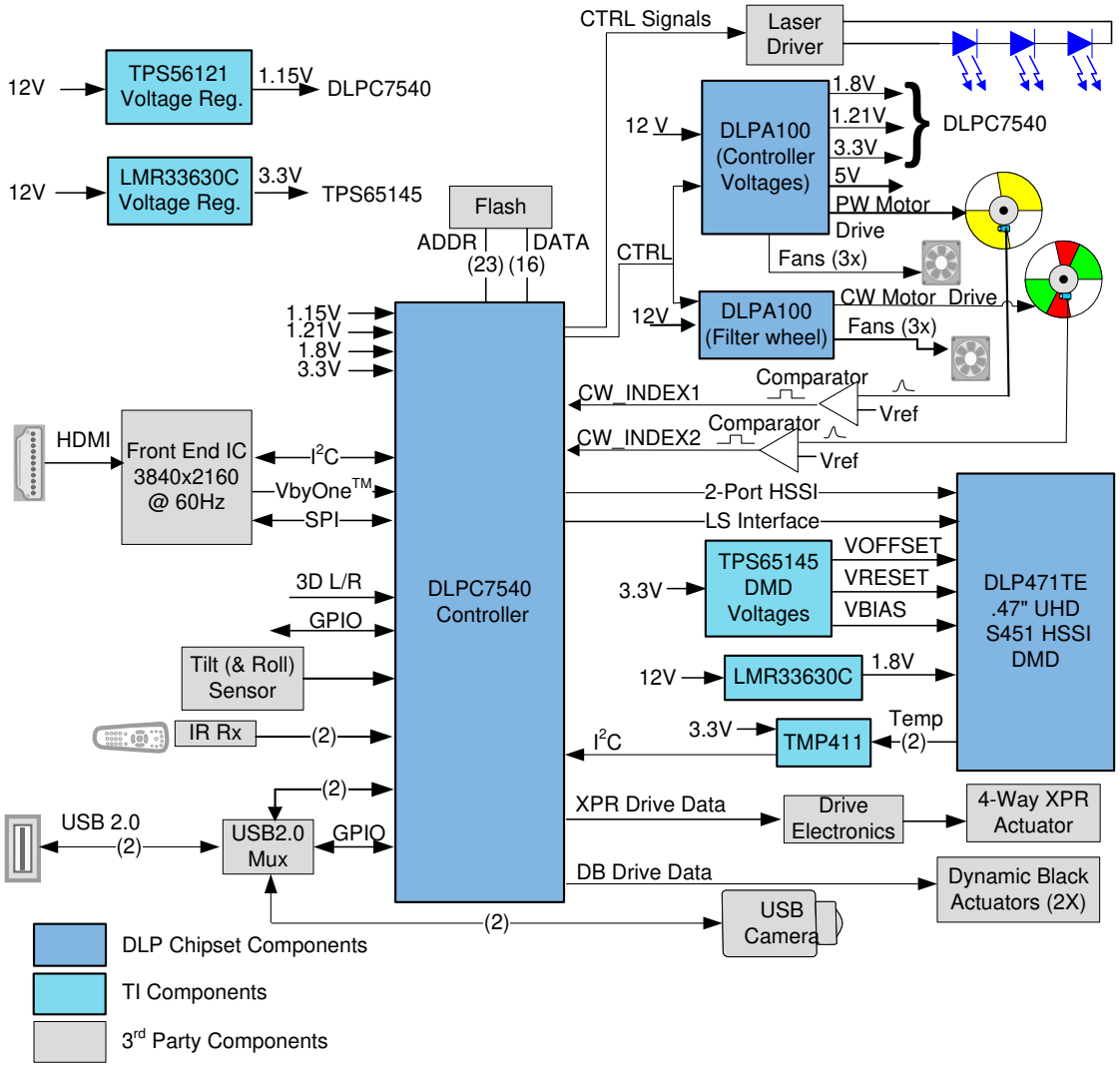


Figure 8-1. Typical 4K UHD Laser Phosphor Application Diagram

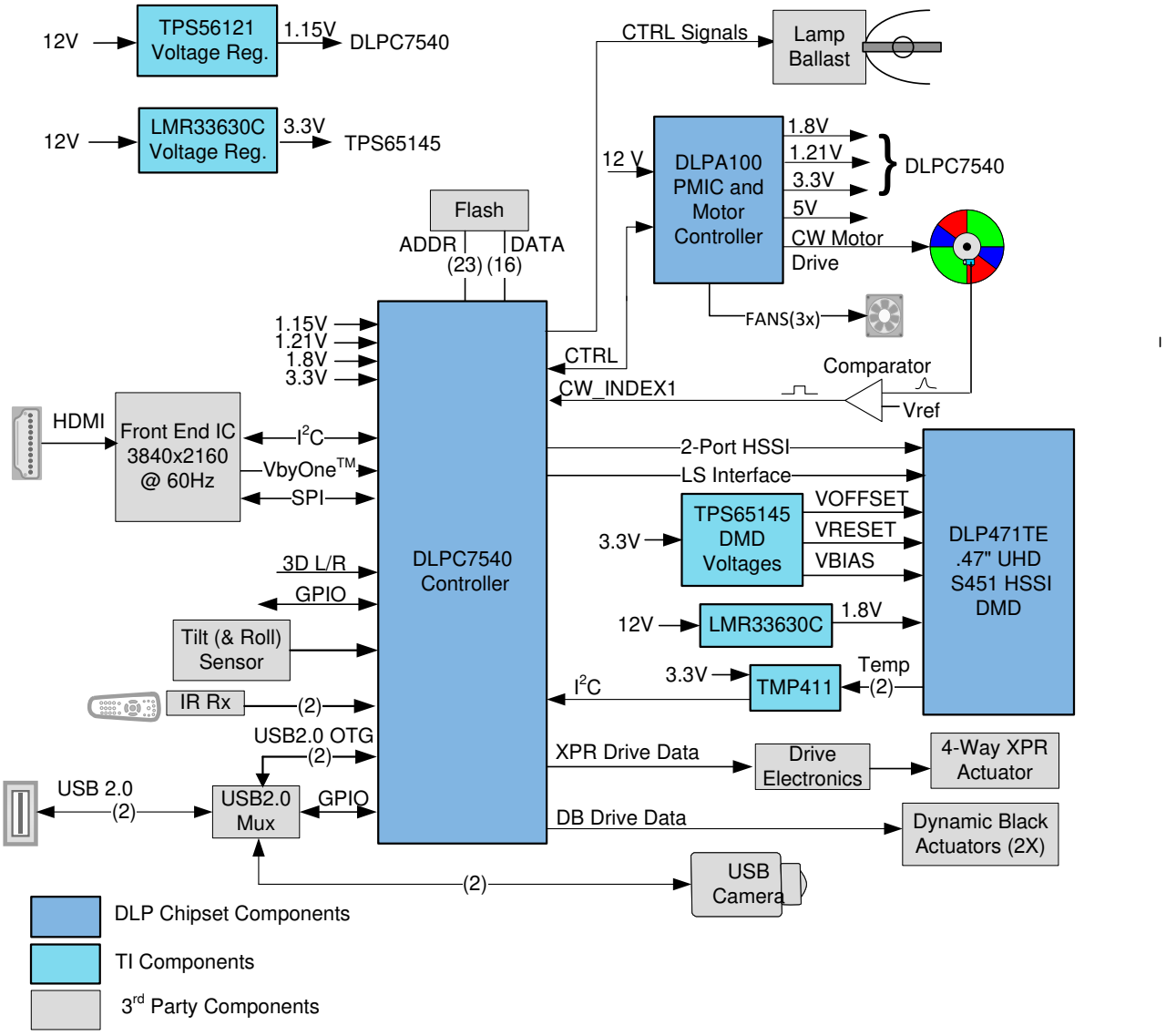


Figure 8-2. Typical 4K UHD Lamp Application Diagram

8.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness has a major effect on the overall system design and size.

The display system uses the DLP471TE as the core imaging device and contains a 0.47-inch array of micromirrors. The DLPC7540 controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver and driving the DMD over a high-speed interface. The DLPA100 PMIC serves as a voltage regulator for the controller, and color filter wheel and phosphor wheel motor control. The TPS65145 provide the DMD reset, offset and bias voltages. The LMR33630C provides the 1.8V power to the DLP471TE.

8.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP471TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with DLPC7540 display controller and the TPS65145 PMIC and DLPA100. Refer to PCB Design Requirements for TI DLP TRP Digital Micromirror Devices for the DMD board design and manufacturing handling of the DMD sub assemblies.

8.2.3 Application Curves

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determines the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. Figure 8-3 describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit. .

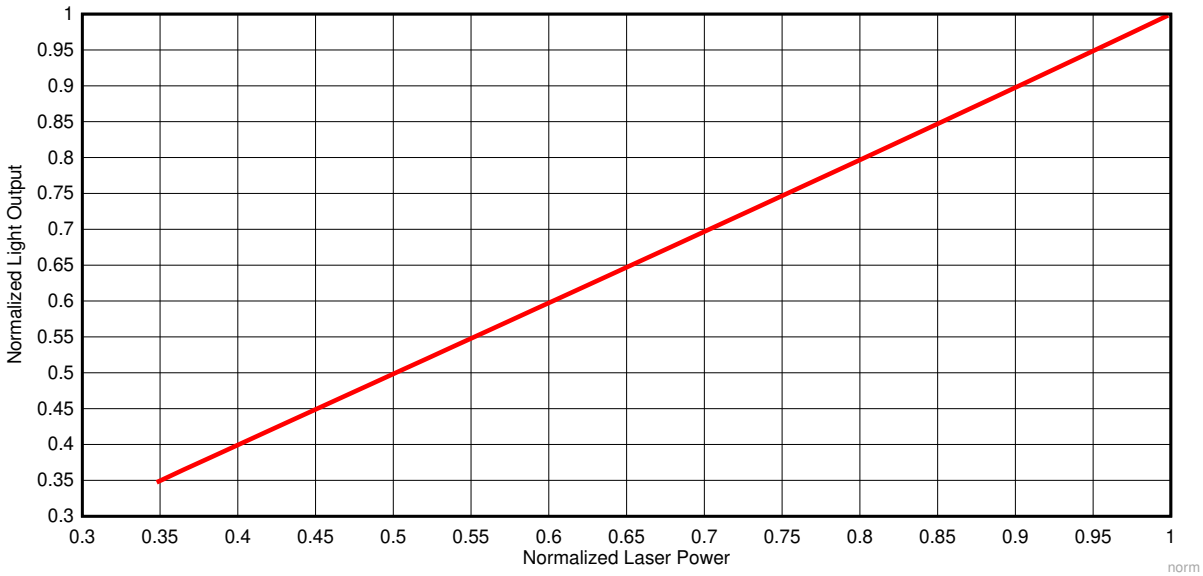
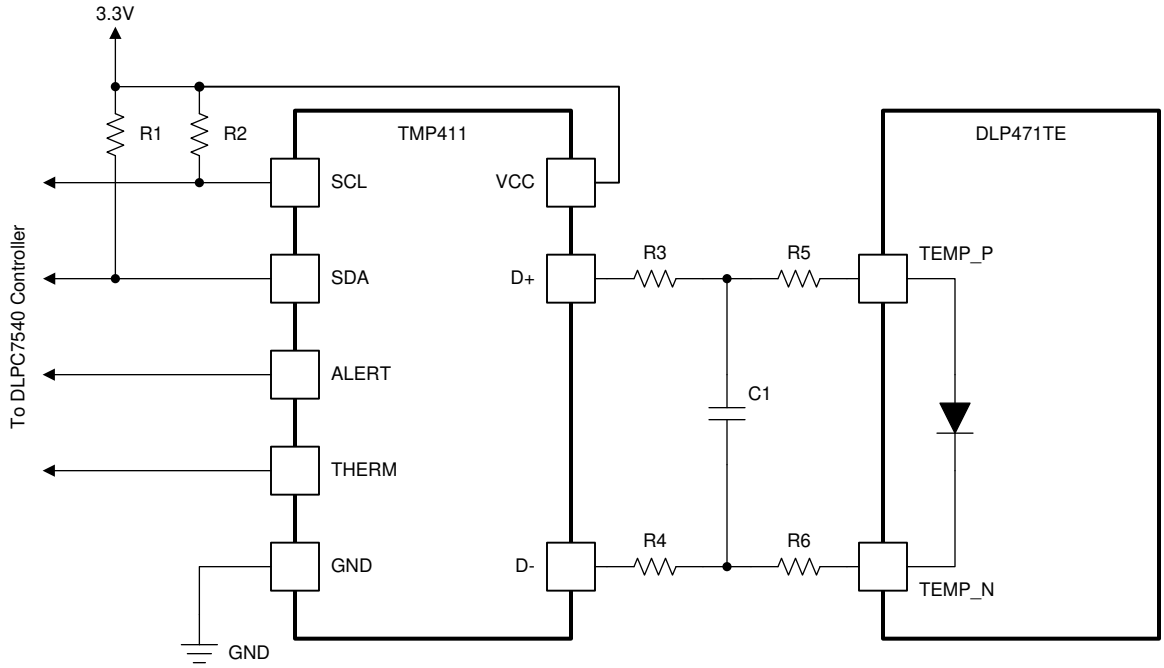


Figure 8-3. Normalized Light Output vs. Normalized Laser Power for Laser Phosphor Illumination

8.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in Figure 8-4. The software application contains functions to configure the TMP411 to read the DLP471TE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the TMP411 and the DLPC7540 controller happens over the I^2C interface. The TMP411 connects to the DMD via pins outlined in Table 5-1.

If the temp sensor is not used, TEMP_N and TEMP_P pins should be left unconnected (NC).



A. Details omitted for clarity.
B. See the TMP411 datasheet for system board layout recommendation.
C. See the TMP411 datasheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0 Ω. R6 = 0 Ω. Place 0-Ω resistors close to the DMD package pins.

Figure 8-4. TMP411 Sample Schematic

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 9-1.

V_{BIAS}, V_{DD}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

Table 9-1. Power Supply Sequence Requirements

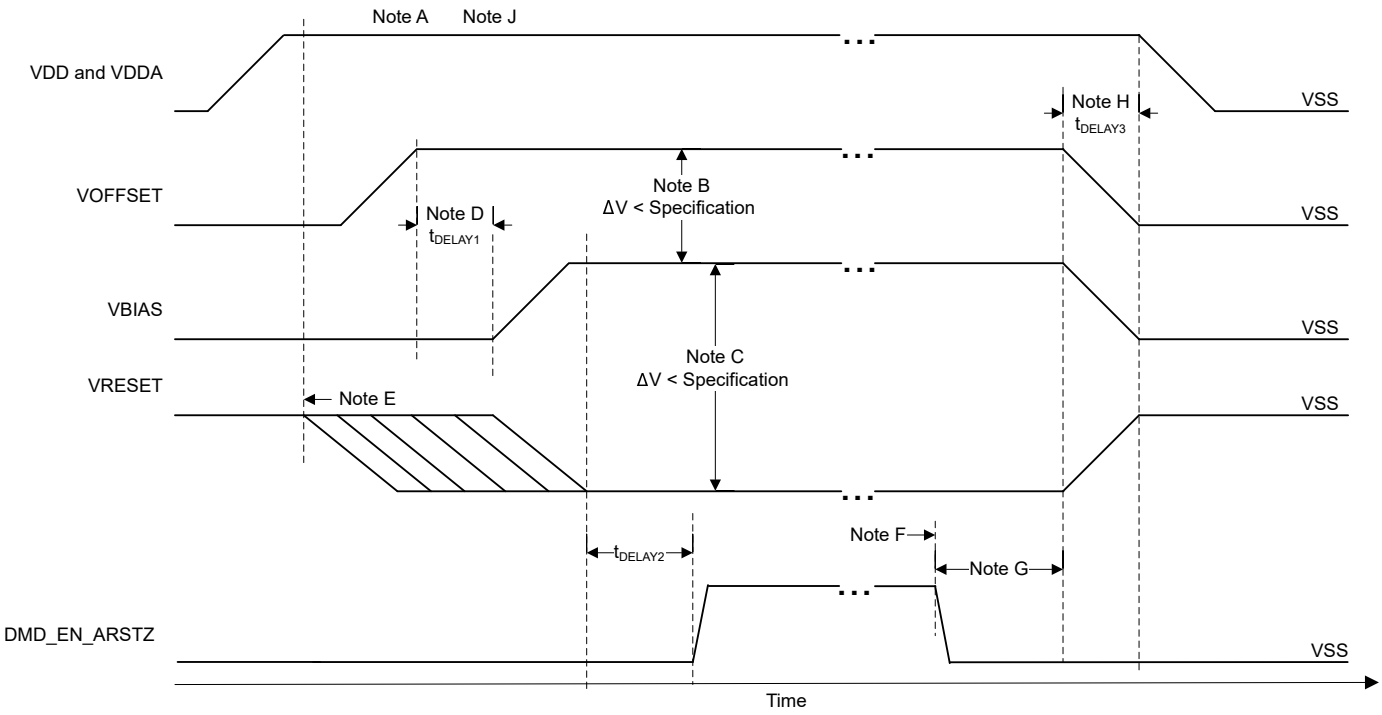
SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY1}	Delay requirement	from V_{OFFSET} power up to V_{BIAS} power up	1	2		ms
t_{DELAY2}	Delay requirement	from V_{BIAS} and V_{RESET} powered on and stable to DMD_EN_ARSTZ going high	20			µs
t_{DELAY3}	Delay requirement	from V_{OFFSET}, V_{BIAS}, and V_{RESET} power down to when VDD and VDDA can power down	50			µs

9.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} must always start and settle before V_{OFFSET} plus t_{DELAY1} specified in Table 9-1, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Table 9-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} has settled at operating voltage listed in *Recommended Operating Conditions*.

9.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See Table 9-1.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Table 9-1.
- During power-down, LVCMOS input pins must be less than specified in *Recommended Operating Conditions*.



A. See *Table 5-1* for pin functions.
B. To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit in *Recommended Operating Conditions*.
C. To prevent excess current, the supply difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit in the *Recommended Operating Conditions*.
D. V_{BIAS} must power up after V_{OFFSET} has powered up, per the t_{DELAY1} specification in Table 9-1.
E. V_{RESET}, V_{OFFSET}, V_{BIAS} ramps must start after VDD and BDDA are powered up and stable.
F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET} and V_{OFFSET}.
G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware DMD_EN_ARSTZ goes low.
H. V_{DD} must remain high until after V_{OFFSET}, V_{BIAS}, V_{RESET} go low, per Delay2 specification in Table 9-1.
I. To prevent excess current, the supply voltage delta $|V_{DDA} – V_{DD}|$ must be less than specified limit in *Recommended Operating Conditions*.
J. Not to scale. Details omitted for clarity.

Figure 9-1. DMD Power Supply Requirements

10 Layout

10.1 Layout Guidelines

The DLP471TE DMD is part of a chipset that is controlled by the DLPC7540 display controller in conjunction with theTPS65145 PMIC and the DLPA100 power and motor controller. These guidelines are targeted at designing a PCB board with the DLP471TE DMD. The DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic including double data rate 3.2 Gbps and 250 Mbps differential data buses run to the DMD. TI recommends that full or mini power planes are used for V_{OFFSET}, V_{RESET}, and V_{BIAS}. Solid planes are required for ground (V_{SS}). The target impedance for the PCB is 50 Ω ±10% with exceptions listed in Table 10-1. TI recommends a 10 layer stack-up as described in Table 10-2. TI recommends manufacturing the PCB with a high quality FR-4 material.

10.2 Impedance Requirements

TI recommends a target impedance for the PCB of 50 Ω ±10% for all signals. The exceptions are listed in Table 10-1.

Table 10-1. Special Impedance Requirements

Signal Type	Signal Name	Impedance (ohms)
DMD High Speed Data Signals	DMD_HSSI0_N_(0…7), DMD_HSSI0_P_(0…7), DMD_HSSI1_N_(0…7), DMD_HSSI1_P_(0…7), DMD_HSSI0_CLK_N, DMD_HSSI0_CLK_P, DMD_HSSI1_CLK_N, DMD_HSSI1_CLK_P	100-Ω differential (50-Ω single ended)
DMD Low Speed Interface Signals	DMD_LS0_WDATA_N, DMD_LS0_WDATA_P, DMD_LS0_CLK_N, DMD_LS0_CLK_P	100-Ω differential (50-Ω single ended)

10.3 Layers

The layer stack-up and copper weight for each layer is shown in Table 10-2.

Table 10-2. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A – DMD, primary components, power mini-planes	0.5 oz (before plating)	DMD and escapes. Two data input connectors. Top components including power generation and two data input connectors. Low frequency signals routing. Use copper fill (GND) plated up to 1 oz.
2	Ground	0.5	Solid ground plane (net GND) reference for signal layers #1, 3.
3	Signal (High frequency)	0.5	High speed signal layer. High Speed differential data buses from input connector to DMD.
4	Ground	0.5	Solid ground plane (net GND) reference for signal layers #3, #5.
5	Power	0.5	Primary split power planes for 1.8 V, 3.3 V, 10 V, –14 V, 18 V
6	Power	0.5	Primary split power planes for 1.8 V, 3.3 V, 10 V, –14 V, 18 V
7	Ground	0.5	Solid ground plane (net GND) Reference for signal layer #8
8	Signal (high frequency)	0.5	High speed signal layer. High speed differential data buses from input connector to DMD.
9	Ground	0.5	Solid ground plane (net GND) Reference for signal layers #8, 10.
10	Side B—Secondary components, power mini-planes	0.5 oz (before plating)	Discrete components if necessary. Low frequency signals routing. Use copper fill plated up to 1 oz.

10.4 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005”/0.015” (Trace-Width/Spacing) design rule. Use an analysis of impedance and stack-up requirements to determine and calculate actual trace widths.

Maximized the width of all voltage signals as space permits. Follow the width and spacing requirements listed in Table 10-3.

Table 10-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH (MIL)	MINIMUM TRACE SPACING (MIL)	LAYOUT REQUIREMENT
GND	MAXIMIZE	5	Maximize trace width to connecting pin as a minimum.
V_{DD}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias.
V_{DDA}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias.
V_{OFFSET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{RESET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{BIAS}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.

10.5 Power

TI strongly discourages signal routing on power planes or on planes adjacent to power planes. If signals must be routed on layers adjacent to power planes, they must not cross splits in power planes to prevent EMI and preserve signal integrity.

Connect all internal digital ground (GND) planes in as many places as possible. Connect all internal ground planes with a minimum distance between connections of 0.5”. Extra vias may not required if there are sufficient ground vias due to normal ground connections of devices.

Connect power and ground pins of each component to the power and ground planes with at least one via for each pin. Minimize trace lengths for component power and ground pins. (ideally, less than 0.100”).

Ground plane slots are strongly discouraged.

10.6 Trace Length Matching Recommendations

Table 10-4 and Table 10-5 describe recommended signal trace length matching requirements. Follow these guidelines to avoid routing long traces over large areas of the PCB:

- Match the trace lengths so that longer signals route in a serpentine pattern
- Minimize the number of turns.
- Ensure that the turn angles no sharper than 45 degrees.

Figure 10-1 shows an example of the HSSI signal pair routing.

Signals listed in Table 10-4 are specified fro data rate operation at up to 3.2 Gbps. Minimize the layer changes for these signals. Minimize the number of vias. Avoid sharp turns and layer switching while minimizing the lengths. When layer changes are necessary, place GND vias around the signal vias to provide a signal return path. The distance from one pair of differential signals to another must be at least 2 times the distance within the pair.

Table 10-4. HSSI High Speed DMD Data Signals

SIGNAL NAME	REFERENCE SIGNAL	ROUTING SPECIFICATION	UNIT
DMD_HSSI0_N(0...7), DMD_HSSI0_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	±0.25	inch
DMD_HSSI1_N(0...7), DMD_HSSI1_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	±0.25	inch
DMD_HSSI0_CLK_P	DMD_HSSI1_CLK_P	±0.05	inch
Intra-pair P	Intra-pair N	±0.01	inch

Table 10-5. Other Timing Critical Signals

SIGNAL NAME	Constraints	Routing Layers
LS_CLK_P, LS_CLK_N LS_WDATA_P, LS_WDATA_N LS_RDATA_A	Intra-pair (P to N) Matched to 0.01 inches Signal-to-signal Matched to +/- 0.25 inches	Layers 3, 8

-

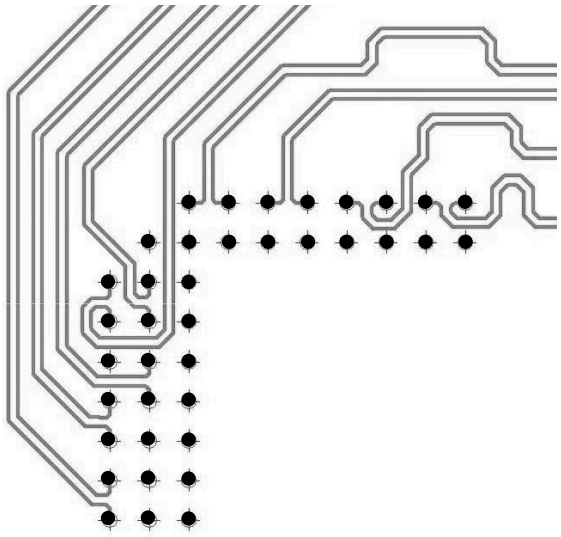


Figure 10-1. Example HSSI PCB Routing

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Device Support

11.2.1 Device Nomenclature

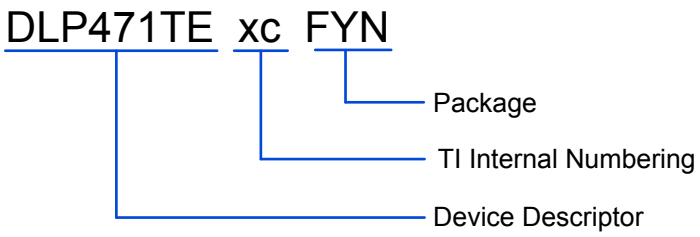

Figure 11-1. Part Number Description

11.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 11-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

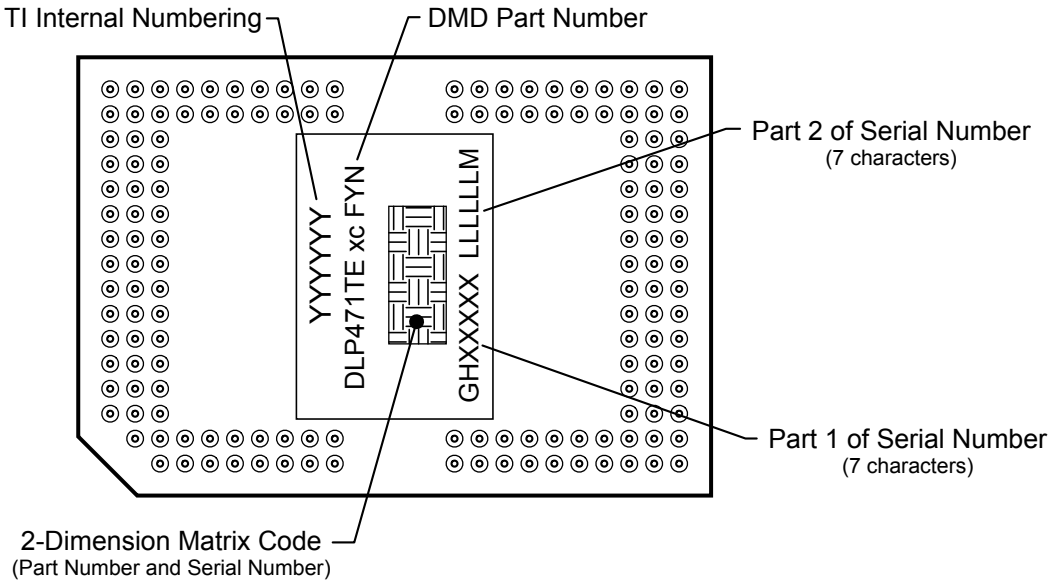

Figure 11-2. DMD Marking Locations

11.3 Documentation Support

11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- DLPC7540 Display Controller Data Sheet
- TPS65145 Data Sheet
- DLPA100 Power and Motor Driver Data Sheet

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

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DLP® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
DLP471TEA0FYN	ACTIVE	CPGA	FYN	149	33	RoHS & Green	Call TI	Call TI		see *Device Marking* section

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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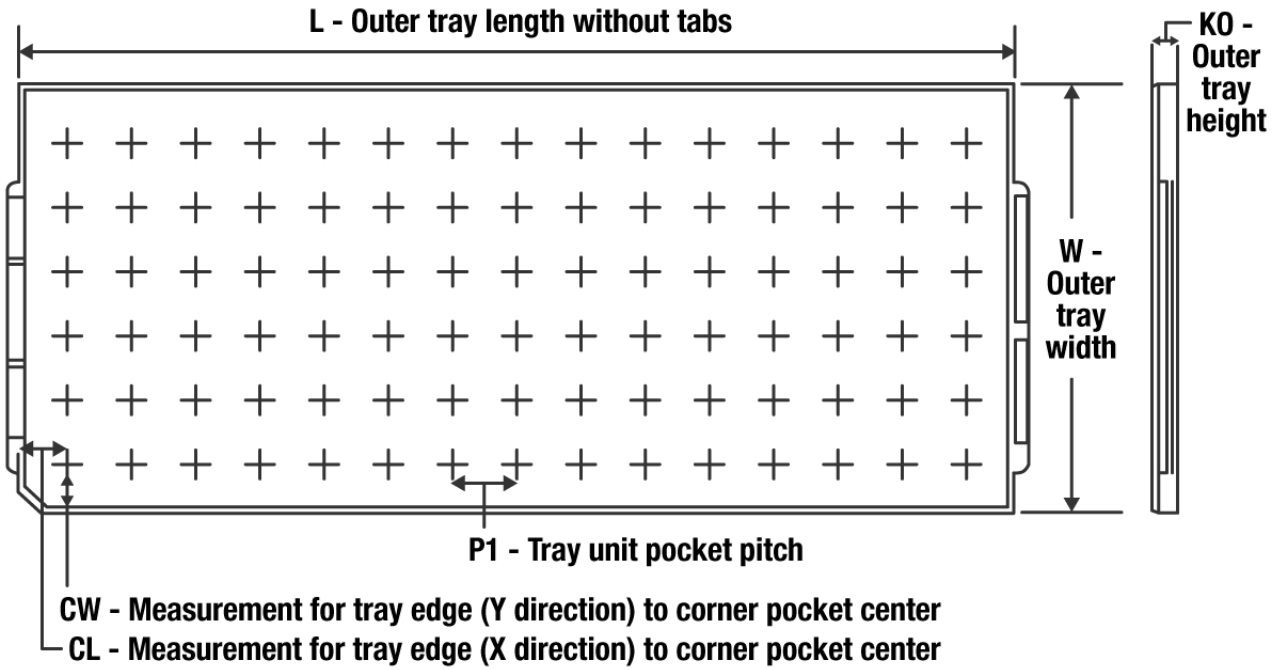
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

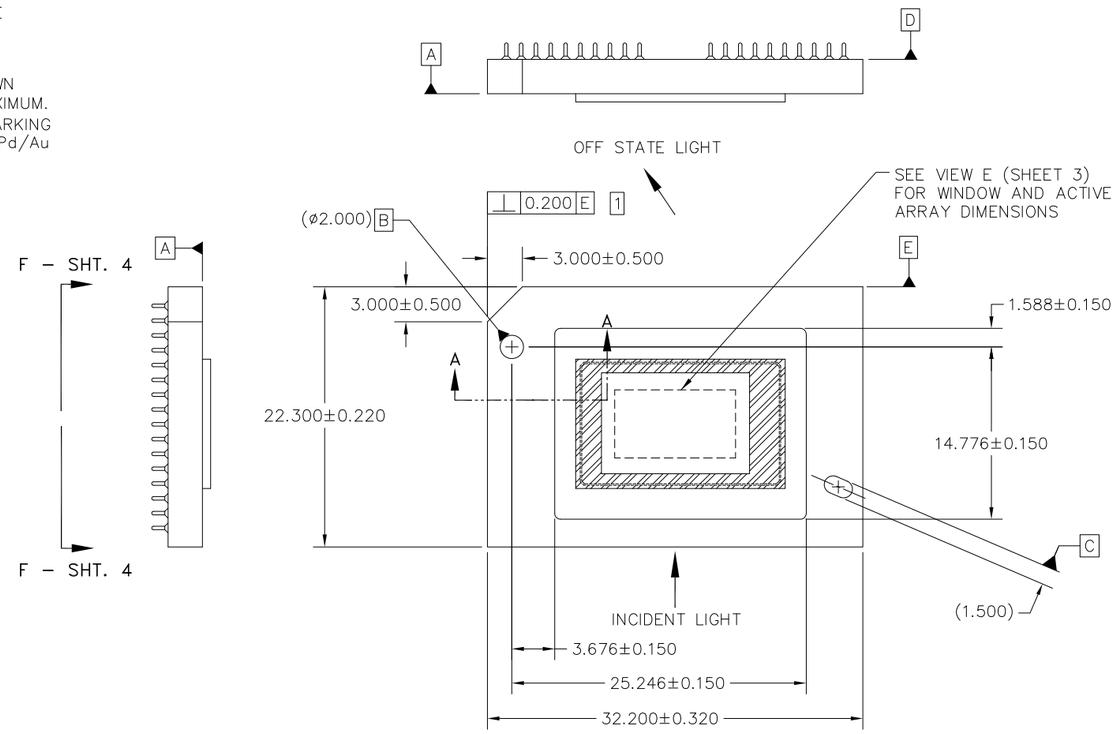
*All dimensions are nominal

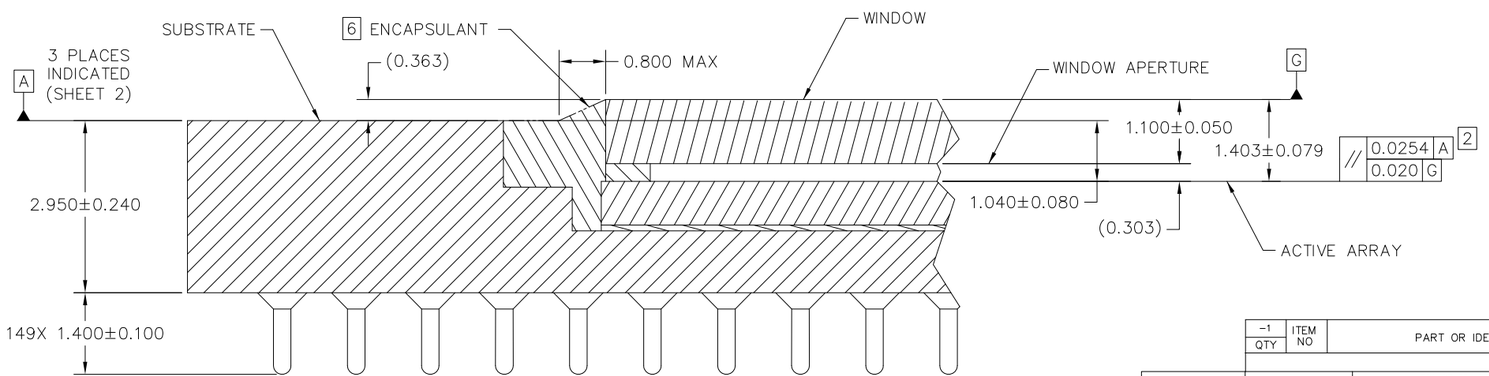
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP471TEA0FYN	FYN	CPGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2178180, INITIAL RELEASE	12/18/2018	F. ARMSTRONG
B	ECO 2179961, REMOVE '4K' DESIGNATION FROM TITLE	03/04/2019	F. ARMSTRONG
C	ECO 2180674, CORRECT THE ENCAP ON CERAMIC ALLOWABLE DIM FROM 3.226 MIN TO 2.300 MIN.	04/09/2019	F. ARMSTRONG
D	ECO 2187478, ADD APERTURE SLOTS PICTORIALLY	05/04/2020	P. CREERY

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
5. MAXIMUM ENCAPSULANT PROFILE SHOWN
6. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
7. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

PARTS LIST

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

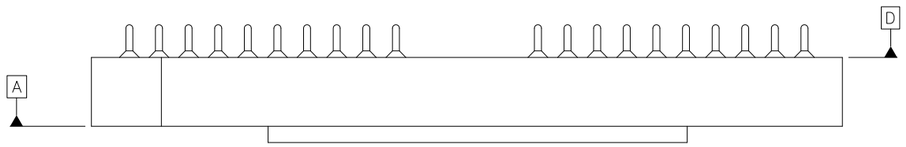
UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

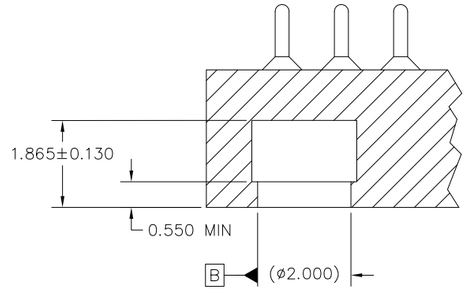
THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

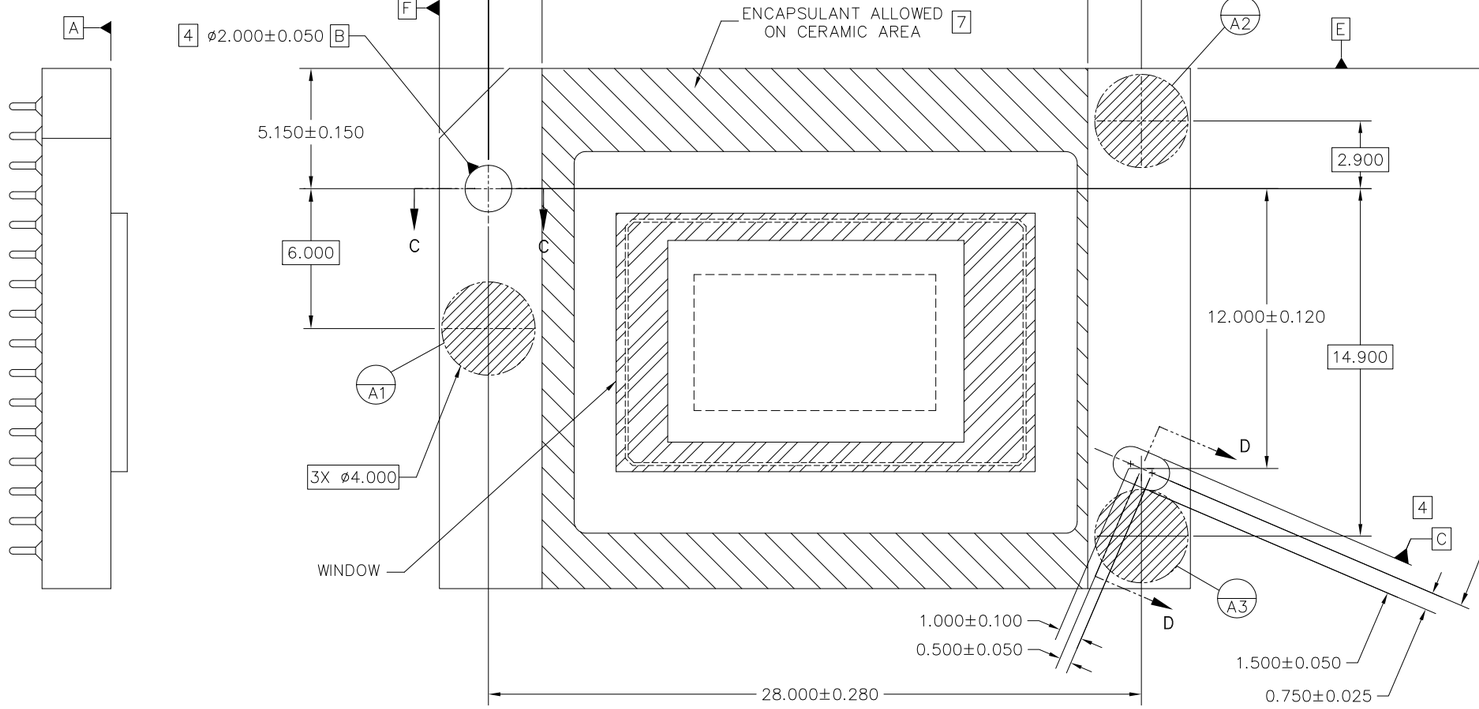
DWN F. ARMSTRONG	DATE 12/18/18	TEXAS INSTRUMENTS Dallas, Texas
ENGR F. ARMSTRONG	12/18/18	ICD, MECHANICAL, DMD .47" MTRP HSSI SERIES 451 (FYN PACKAGE)
QA K. DICKERSON	12/21/18	
CQE M. DORAK	12/21/18	SIZE B · DRAWING NO 2516515 · REV D
		SCALE 4/1 · SHEET 1 OF 4

ACED1g

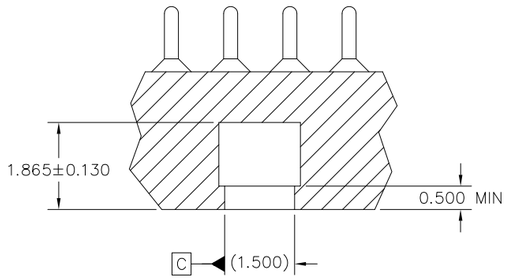




SECTION C–C
DATUM B
SCALE 16/1



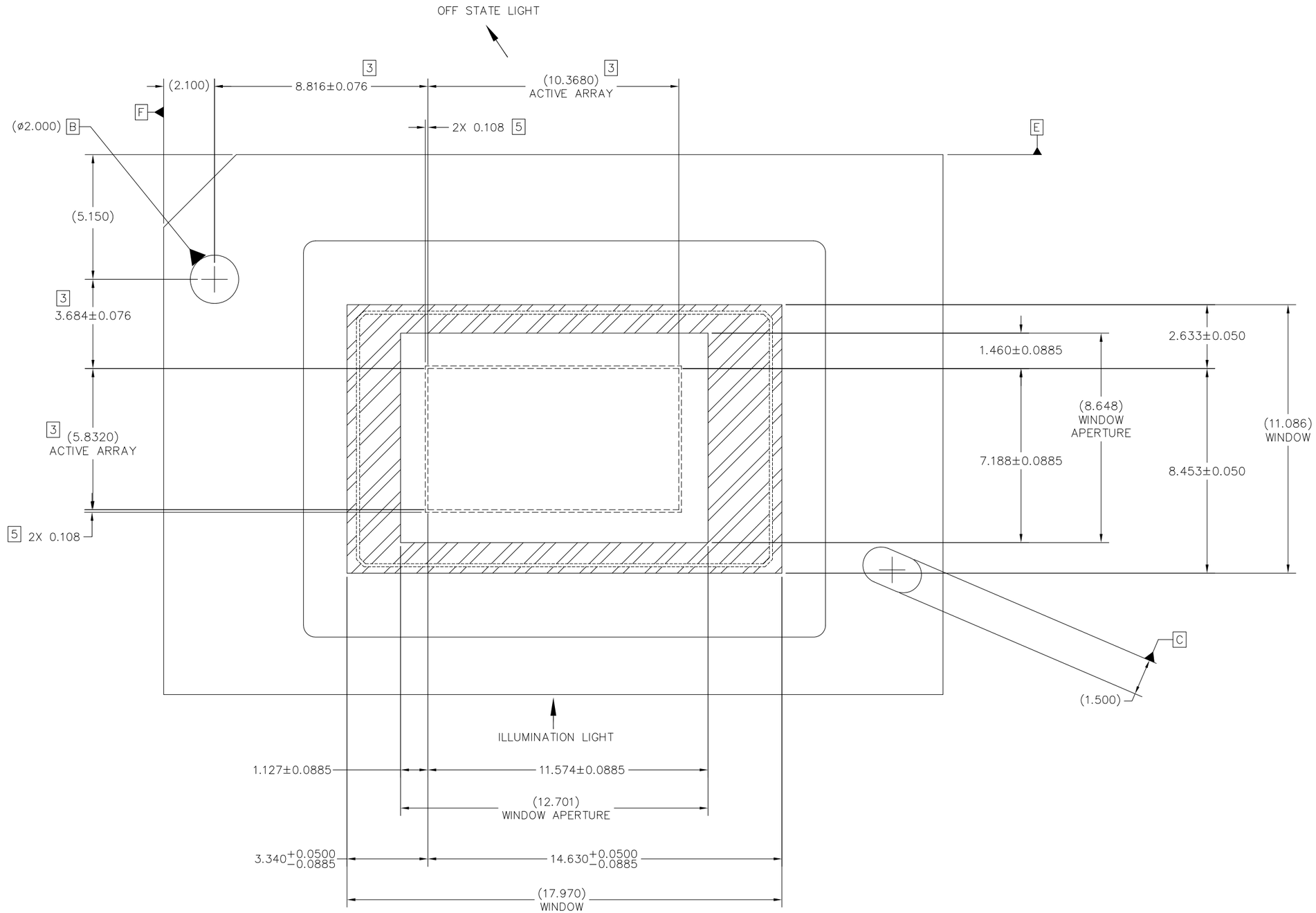
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE B	DRAWING NO 2516515	REV D
		SCALE 4/1	SHEET 2	

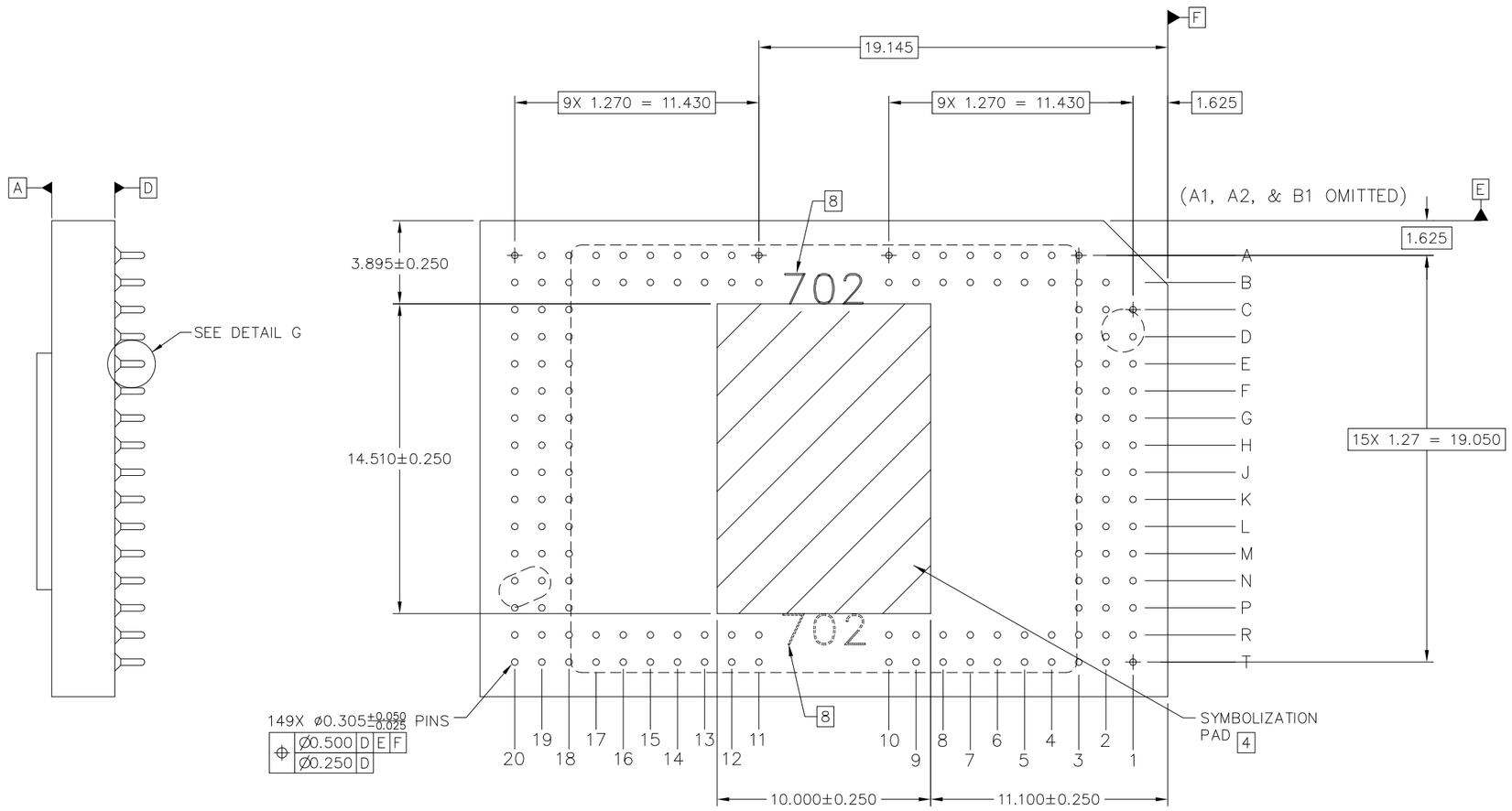
ACED2c



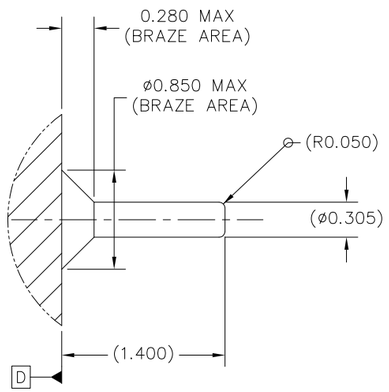
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12/1

Texas Instruments, Dallas, Texas	DWN DATE	SIZE B		DRAWING NO 2516515	REV D
	ISSUE DATE	SCALE 4/1		SHEET 3	

ACED2c



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

Texas Instruments, Dallas, Texas	DWN DATE	SIZE B	DRAWING NO 2516515	REV D
	ISSUE DATE	SCALE 4/1	SHEET 4	

ACED2c

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