74AHC573-Q100; 74AHCT573-Q100

Octal D-type transparent latch; 3-state

Rev. 3.1 — 11 October 2023 Product data sheet

1. General description

The 74AHC573-Q100; 74AHCT573-Q100 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ($\overline{OE}$) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 5.5 V
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Common 3-state output enable input
- Input levels:
  - For 74AHC573-Q100: CMOS input level
  - For 74AHCT573-Q100: TTL input level
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC573D-Q100 74AHCT573D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC573PW-Q100 74AHCT573PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHC573BQ-Q100 74AHCT573BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

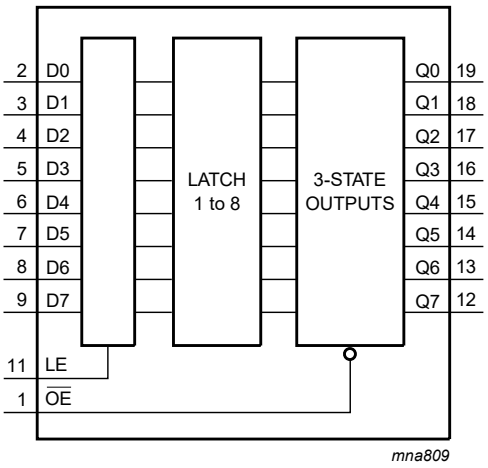


Fig. 1. Functional diagram

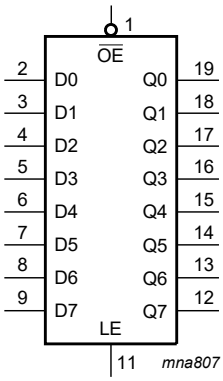


Fig. 2. Logic symbol

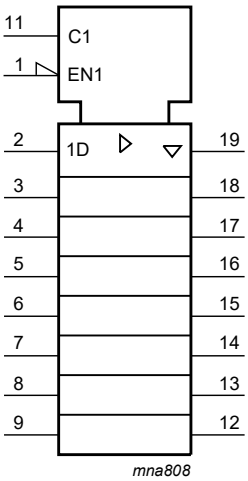


Fig. 3. IEC logic symbol

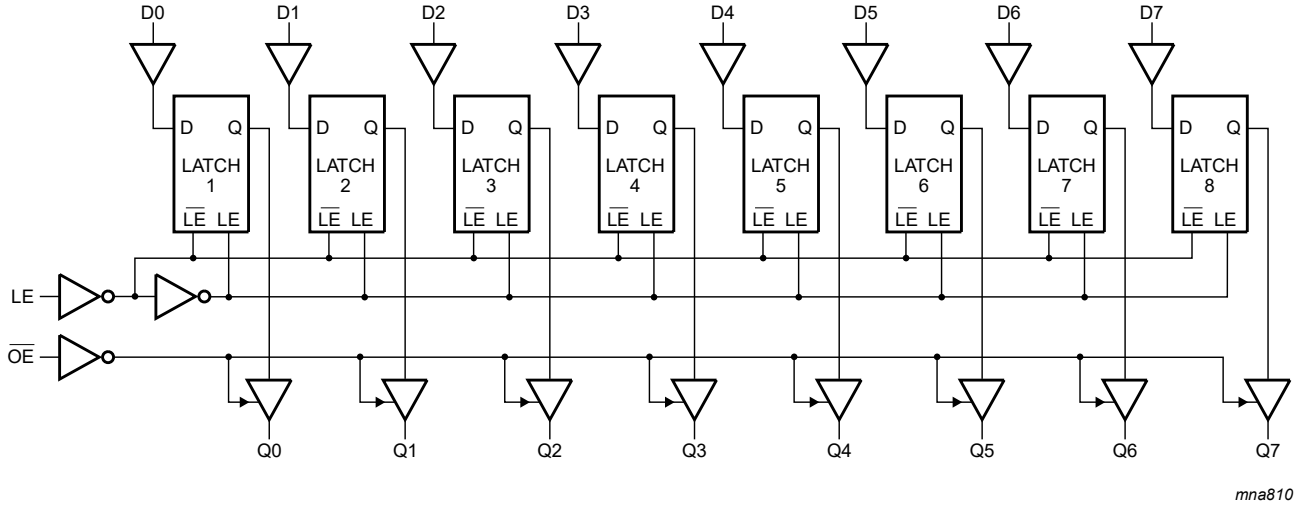
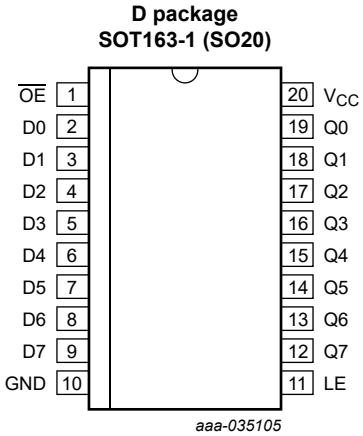
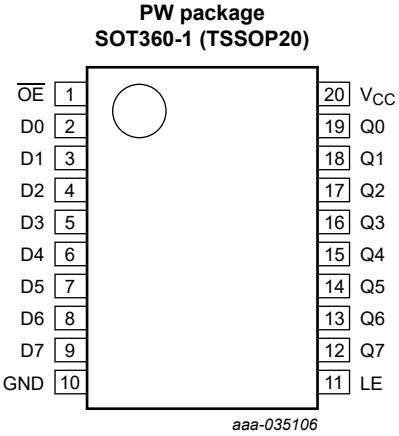


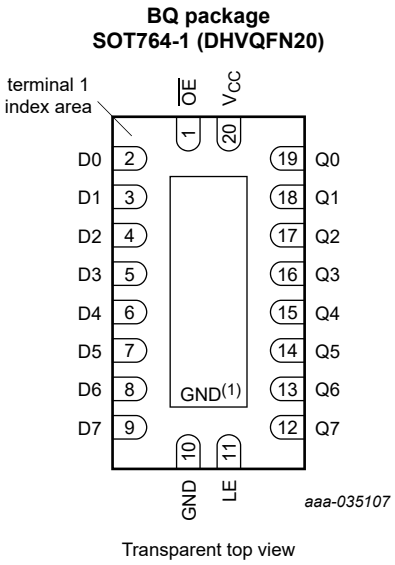
Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning







(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
LE	11	latch enable (active HIGH)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	data output
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

Operating mode	Input			Internal latch	Output
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V	[1]	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	[1]	-20	+20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		-25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC573-Q100			74AHCT573-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V_{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max	Min	Typ	Max	
74AHC573-Q100											
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}									
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	-	V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	-	V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	-	V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}									
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	-	0.55	V
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	-	±10.0	µA
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	-	80	µA
C_I	input capacitance	V_I = V_{CC} or GND	-	3	10	-	10	-	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	10	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max	Min	Typ	Max	
74AHCT573-Q100											
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V									
		I_O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	-	V
		I_O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V									
		I_O = 50 µA	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	-	0.55	V
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	-	±10.0	µA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	-	1.5	mA
C_I	input capacitance	V_I = V_{CC} or GND	-	3	10	-	10	-	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

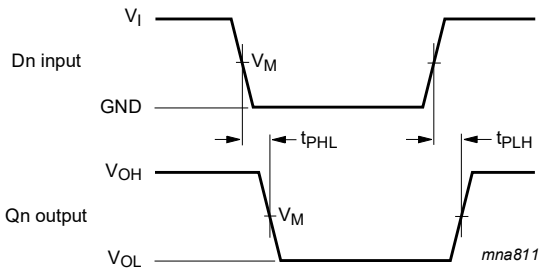
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC573-Q100										
t_{pd}	propagation delay	Dn to Qn; see Fig. 5 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.5	11.0	1.0	13.0	1.0	14.0	ns
		C_L = 50 pF	-	7.8	14.5	1.0	16.5	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.9	6.8	1.0	8.0	1.0	8.5	ns
		C_L = 50 pF	-	5.5	8.8	1.0	10.0	1.0	11.0	ns
		LE to Qn; see Fig. 6 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.8	11.9	1.0	14.0	1.0	15.0	ns
		C_L = 50 pF	-	8.3	15.4	1.0	17.5	1.0	19.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.2	7.7	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF	-	5.9	9.7	1.0	11.0	1.0	12.5	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 7 [3]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.8	11.5	1.0	13.5	1.0	14.5	ns
		C_L = 50 pF	-	8.3	15.0	1.0	17.0	1.0	19.0	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.4	7.7	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF	-	6.3	9.7	1.0	11.0	1.0	12.5	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 7 [4]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	6.8	11.0	1.0	13.0	1.0	14.0	ns
		C_L = 50 pF	-	9.7	14.5	1.0	16.5	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.6	7.7	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF	-	7.4	9.7	1.0	11.0	1.0	12.5	ns
t_W	pulse width	LE HIGH; see Fig. 6								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	Dn to LE; see Fig. 8								
		V_{CC} = 3.0 V to 3.6 V	3.5	-	-	3.5	-	3.5	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.5	-	-	3.5	-	3.5	-	ns
t_h	hold time	Dn to LE; see Fig. 8								
		V_{CC} = 3.0 V to 3.6 V	1.5	-	-	1.5	-	1.5	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.5	-	-	1.5	-	1.5	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [5]	-	12	-	-	-	-	-	pF
74AHCT573-Q100; V_{CC} = 4.5 V to 5.5 V										
t_{pd}	propagation delay	Dn to Qn; see Fig. 5 [2]								
		C_L = 15 pF	-	3.5	5.5	1	6.5	1	7.0	ns
		C_L = 50 pF	-	4.9	7.5	1	8.5	1	9.5	ns
		LE to Qn; see Fig. 6 [2]								
		C_L = 15 pF	-	3.9	6.0	1	7.0	1	7.5	ns
		C_L = 50 pF	-	5.5	8.5	1	9.5	1	11.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 7 [3]								
		C_L = 15 pF	-	4.1	6.5	1	7.5	1	8.5	ns
		C_L = 50 pF	-	5.9	8.5	1	10.0	1	11.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 7 [4]								
		C_L = 15 pF	-	4.5	6.5	1	7.5	1	8.5	ns
		C_L = 50 pF	-	6.4	9.0	1	10.0	1	11.5	ns
t_W	pulse width	LE HIGH; see Fig. 6	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	Dn to LE; see Fig. 8	3.5	-	-	3.5	-	3.5	-	ns
t_h	hold time	Dn to LE; see Fig. 8	1.5	-	-	1.5	-	1.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [5]	-	18	-	-	-	-	-	pF

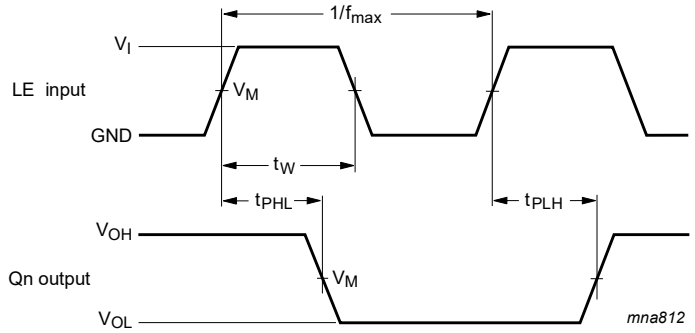
[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{en} is the same as t_{PZH} and t_{PZL}.
[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

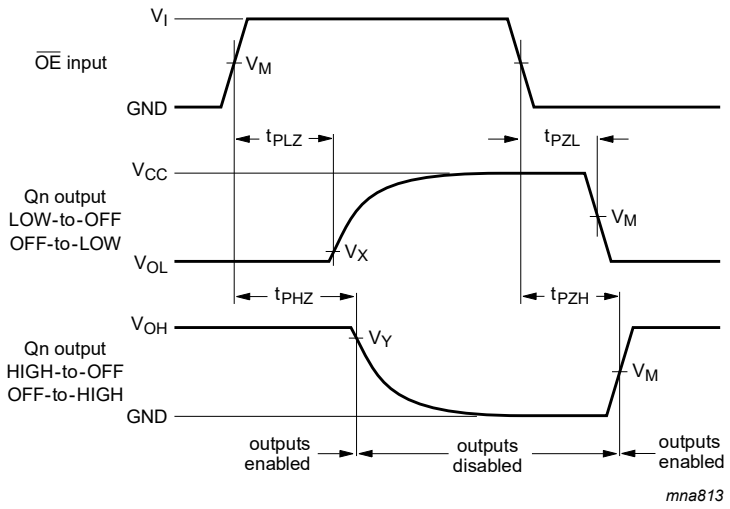
Fig. 5. Data input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

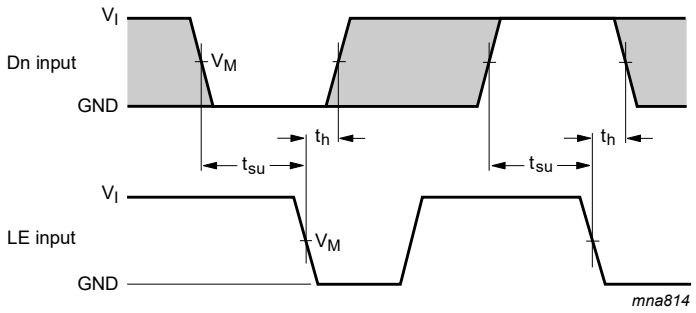
Fig. 6. Latch enable input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Enable and disable times



Measurement points are given in Table 8.

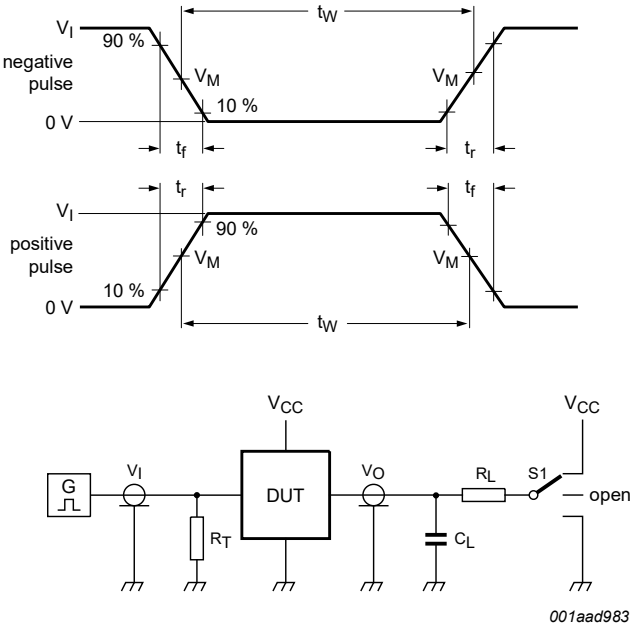
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig. 8. Data set-up and hold times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC573-Q100	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V
74AHCT573-Q100	1.5 V	0.5 × V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

S1 = test selection switch.

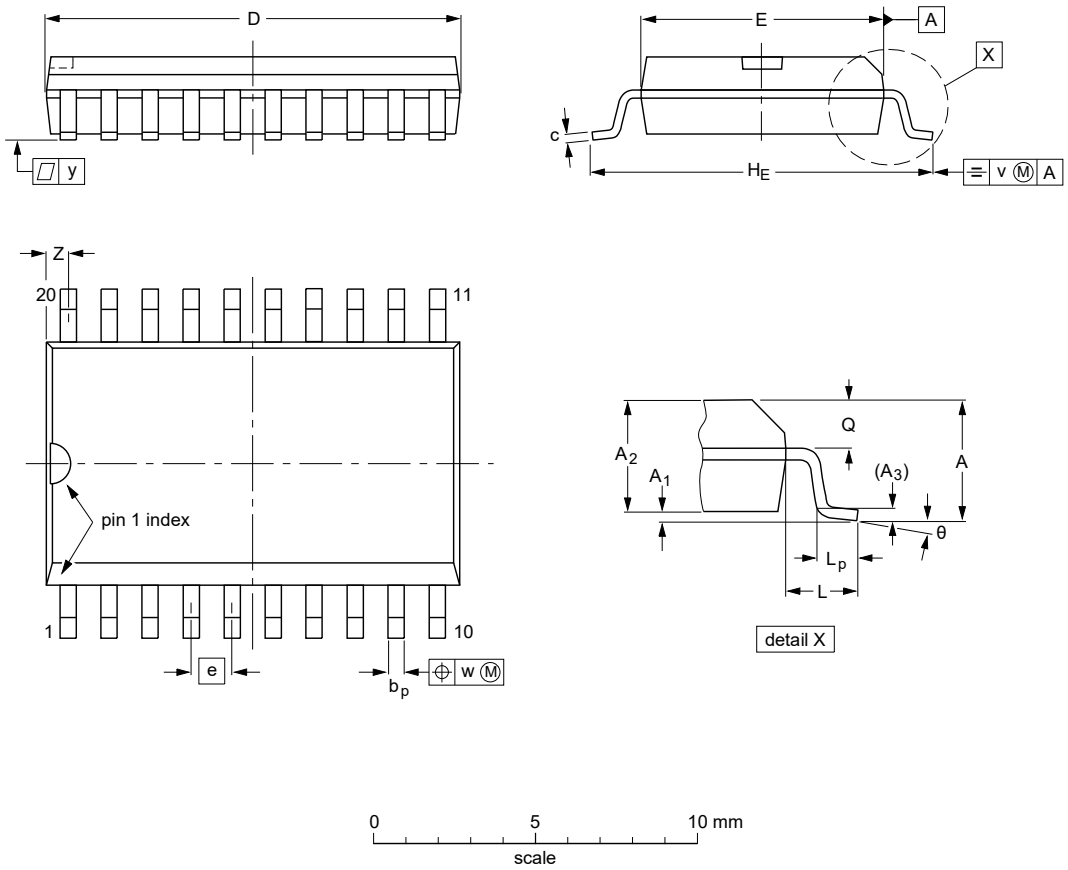
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC573-Q100	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT573-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

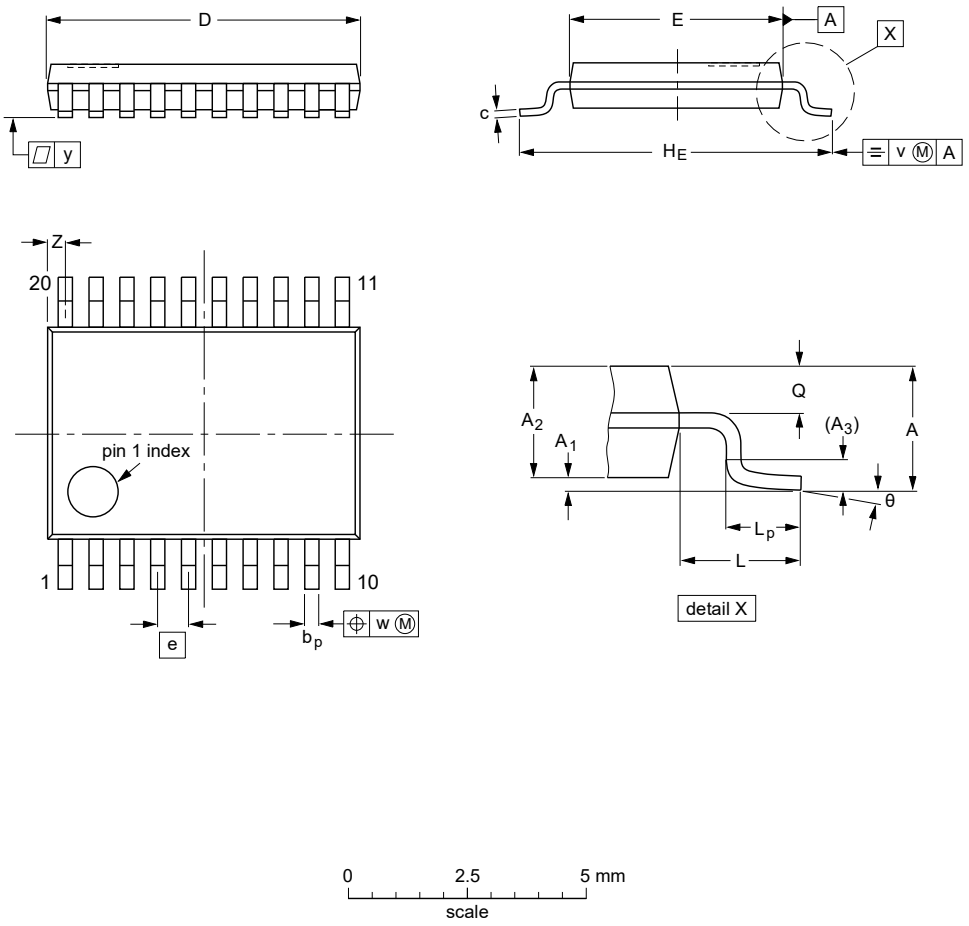
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

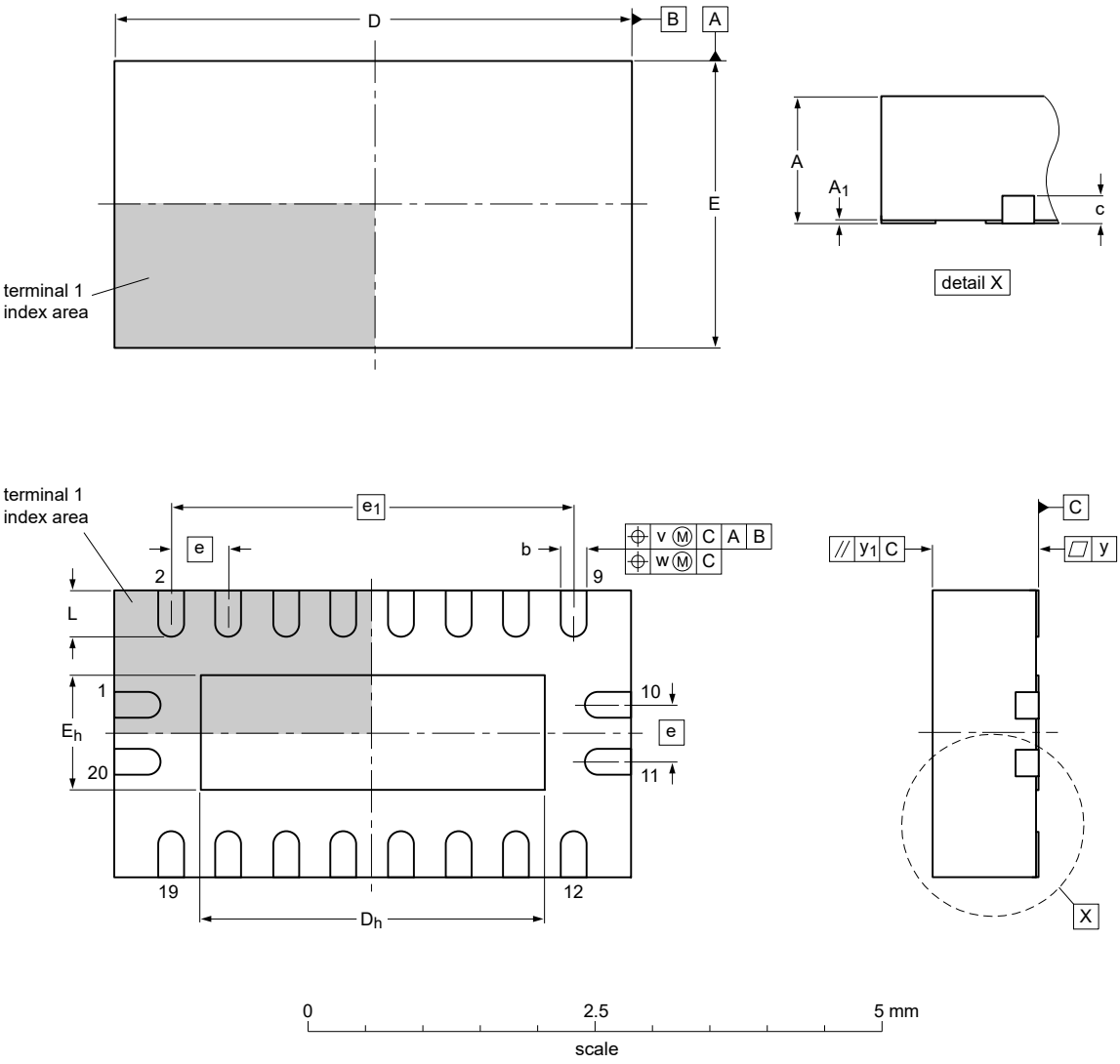
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 11. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig. 12. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT573_Q100 v.3.1	20231011	Product data sheet	-	74AHC_AHCT573_Q100 v.2
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AHC_AHCT573_Q100 v.2	20200713	Product data sheet	-	74AHC_AHCT573_Q100 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation have been updated. • Table 6: Conditions for I_{OZ} corrected. • Package outline drawing of SOT764-1 (Fig. 12) updated.			
74AHC_AHCT573_Q100 v.1	20130610	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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