

# NCA9535

## Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

Rev. 1 — 31 March 2023

Product data sheet

## 1. General description

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The NCA9535 provides 16 bits of General Purpose Input/Output (GPIO) expansion for I<sup>2</sup>C-bus/SMBus applications. It is designed for a wide voltage range of 1.65 V to 5.5 V with interrupt. Nexperia GPIO expanders provide an elegant solution when additional IOs are needed while keeping the interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs and fan control. The NCA9535 contains a set of 8 bit input, output, configuration and polarity inversion registers. At power up all IOs default to inputs. Each IO can be configured as either input or output by changing the corresponding bit in the configuration register. The data for each input or output is stored in the corresponding input or output register. The polarity inversion register can be programmed to invert the polarity of the input register. The NCA9535 has an open-drain interrupt output which is activated when any one of the GPIO changes from its corresponding input port register state. The power on reset sets the registers to default values and initializes the device state machine. The NCA9535 has three address pins A0, A1 and A2 which can be used to configure the I<sup>2</sup>C bus slave address of the device. It allows up-to eight devices to share the same I<sup>2</sup>C-bus/SMBus.

## 2. Features and benefits

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- I<sup>2</sup>C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 2.5  $\mu$ A (maximum)
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - $V_{\text{hys}} = 0.10 \times V_{\text{CC}}$  (typical)
  - Noise filter on SCL and SDA inputs
- 5 V tolerant I/Os
- 16 I/O pins which power up configured in input state
- Open-drain active LOW interrupt output (INT)
- 400 kHz Fast-mode I<sup>2</sup>C-bus
- Internal power-on reset
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1000 V
- Package offered: TSSOP24
- Specified from -40 °C to +85 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">NCA9535PW</a>	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	<a href="#">SOT355-1</a>

### 4. Block diagram

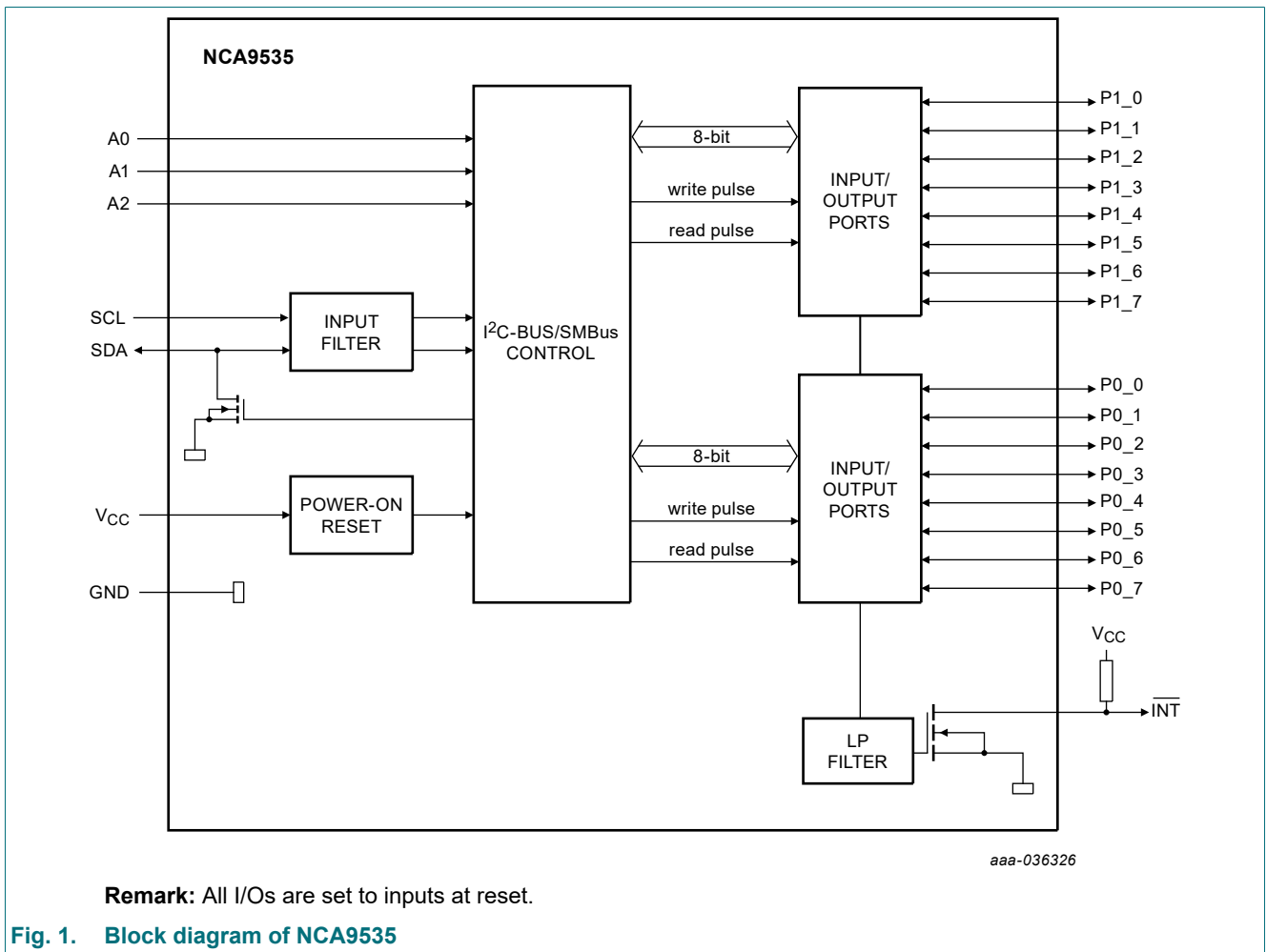


Fig. 1. Block diagram of NCA9535

## 5. Pinning information

### 5.1. Pinning

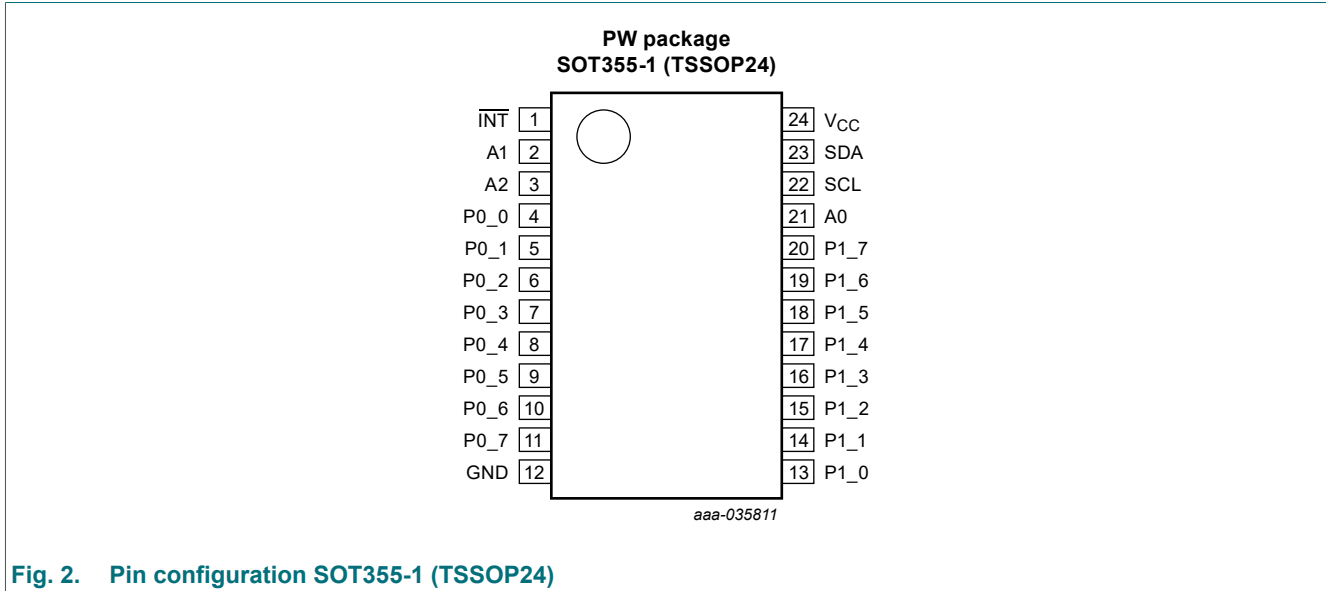


Fig. 2. Pin configuration SOT355-1 (TSSOP24)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
INT	1	O	Interrupt output. Connect to V <sub>CC</sub> through a pull-up resistor
A1	2	I	Address input 1. Connect directly to V <sub>CC</sub> or GND
A2	3	I	Address input 2. Connect directly to V <sub>CC</sub> or GND
P0_0 [1]	4	I/O	Parallel port I/O. Push-pull driver. At power on, P0_0 is configured as input
P0_1 [1]	5	I/O	Parallel port I/O. Push-pull driver. At power on, P0_1 is configured as input
P0_2 [1]	6	I/O	Parallel port I/O. Push-pull driver. At power on, P0_2 is configured as input
P0_3 [1]	7	I/O	Parallel port I/O. Push-pull driver. At power on, P0_3 is configured as input
P0_4 [1]	8	I/O	Parallel port I/O. Push-pull driver. At power on, P0_4 is configured as input
P0_5 [1]	9	I/O	Parallel port I/O. Push-pull driver. At power on, P0_5 is configured as input
P0_6 [1]	10	I/O	Parallel port I/O. Push-pull driver. At power on, P0_6 is configured as input
P0_7 [1]	11	I/O	Parallel port I/O. Push-pull driver. At power on, P0_7 is configured as input
GND	12	power	Ground
P1_0 [2]	13	I/O	Parallel port I/O. Push-pull driver. At power on, P1_0 is configured as input
P1_1 [2]	14	I/O	Parallel port I/O. Push-pull driver. At power on, P1_1 is configured as input
P1_2 [2]	15	I/O	Parallel port I/O. Push-pull driver. At power on, P1_2 is configured as input
P1_3 [2]	16	I/O	Parallel port I/O. Push-pull driver. At power on, P1_3 is configured as input
P1_4 [2]	17	I/O	Parallel port I/O. Push-pull driver. At power on, P1_4 is configured as input
P1_5 [2]	18	I/O	Parallel port I/O. Push-pull driver. At power on, P1_5 is configured as input
P1_6 [2]	19	I/O	Parallel port I/O. Push-pull driver. At power on, P1_6 is configured as input
P1_7 [2]	20	I/O	Parallel port I/O. Push-pull driver. At power on, P1_7 is configured as input
A0	21	I	Address input 0. Connect directly to V <sub>CC</sub> or GND

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Symbol	Pin	Type	Description
SCL	22	I	Serial clock bus. Connect to V <sub>CC</sub> through a pull-up resistor
SDA	23	I/O	Serial data bus. Connect to V <sub>CC</sub> through a pull-up resistor.
V <sub>CC</sub>	24	power	Supply voltage.

- [1] Pins P0\_0 to P0\_7 correspond to bits P0.0 to P0.7. At power-up, all I/O are configured as high-impedance inputs.
- [2] Pins P1\_0 to P1\_7 correspond to bits P1.0 to P1.7. At power-up, all I/O are configured as high-impedance inputs.

## 6. Functional description

For the block diagram of the NCA9535 see [Fig. 1](#).

### 6.1. Device address

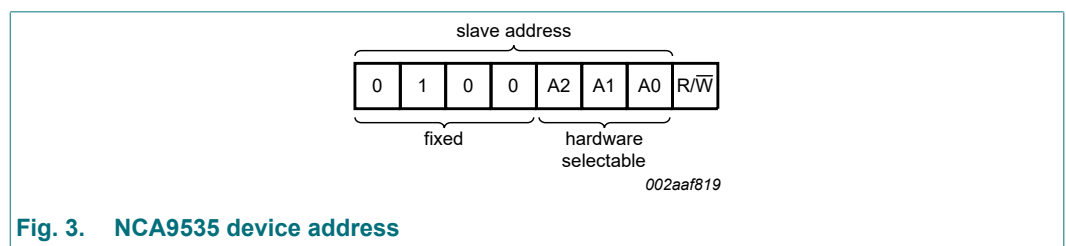


Fig. 3. NCA9535 device address

A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/W) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

### 6.2. Registers

#### 6.2.1. Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the address pointer register of the NCA9535. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

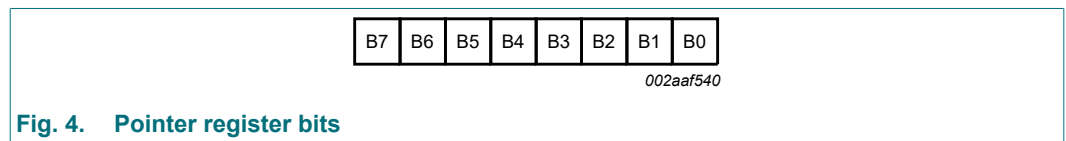


Fig. 4. Pointer register bits

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Table 3. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx [1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111

[1] The default value 'X' is determined by the externally applied logic level.

### 6.2.2. Input port register pair (00h, 01h)

The Input port registers (registers 0 and 1) reflect the logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in [Section 7.2](#).

Table 4. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 5. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

### 6.2.3. Output port register pair (02h, 03h)

The Output port registers (registers 2 and 3) define the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 6. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 7. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

#### 6.2.4. Polarity inversion register pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the Input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

**Table 8. Polarity inversion port 0 register (address 04h)**

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

**Table 9. Polarity inversion port 1 register (address 05h)**

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

#### 6.2.5. Configuration register pair (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

**Table 10. Configuration port 0 register (address 06h)**

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

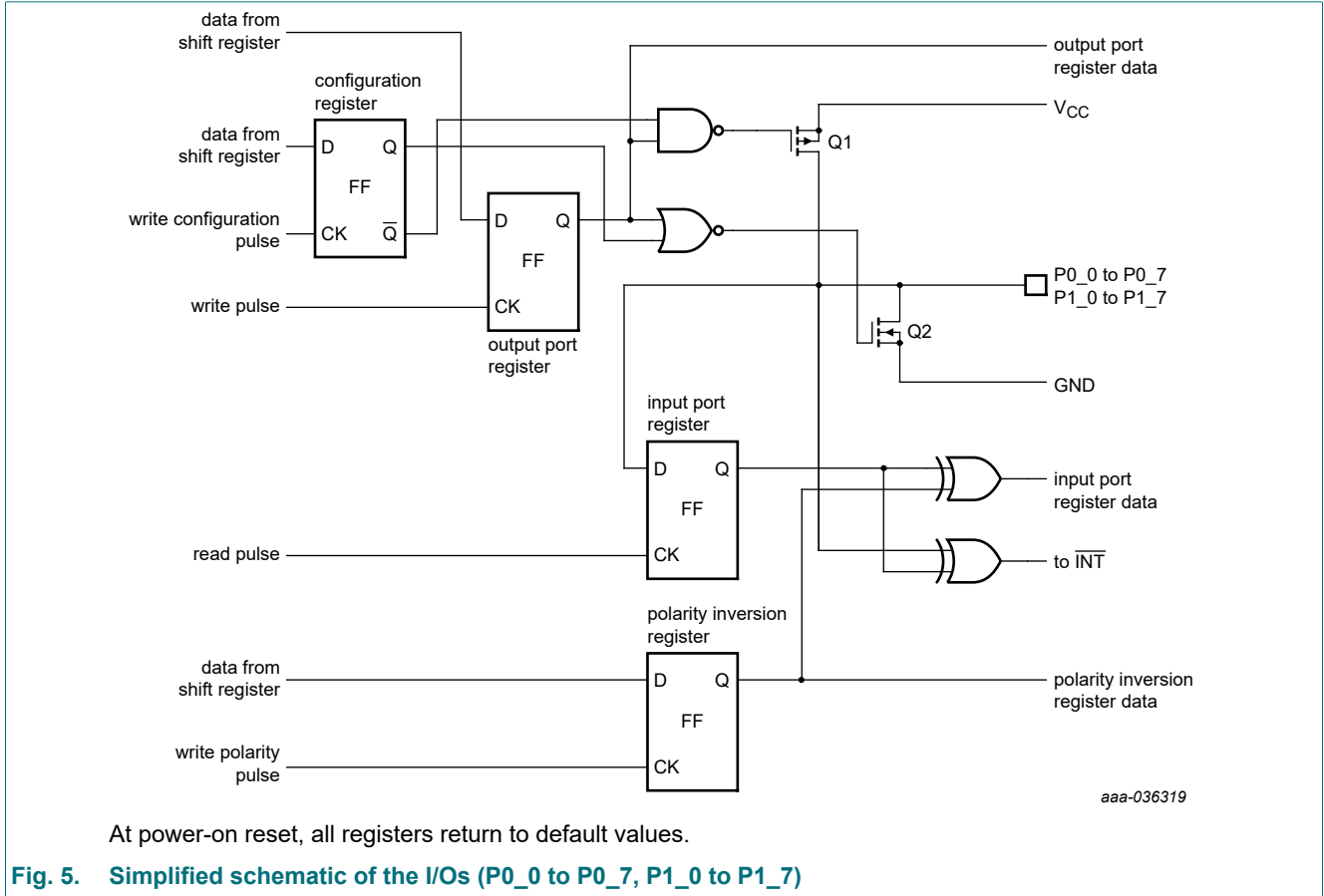
**Table 11. Configuration port 1 register (address 07h)**

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

### 6.3. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above  $V_{CC}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either  $V_{CC}$  or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



## 6.4. Power-on reset

When power (from 0 V) is applied to  $V_{CC}$  and starts rising, an internal power-on reset holds the NCA9535 in a reset condition until  $V_{CC}$  has reached  $V_{PORR}$ . At that time, the reset condition is released and the NCA9535 registers and I<sup>2</sup>C-bus/SMBus state machine initializes to their default states. After that,  $V_{CC}$  must be lowered to below  $V_{PORF}$  and back up to the operating voltage for a power-reset cycle. See [Section 8.2](#).

## 6.5. Interrupt output

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time  $t_{v(INT)}$ , the signal  $\overline{INT}$  is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt (see [Fig. 9](#) and [Fig. 10](#)). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as  $\overline{INT}$ .

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

# 7. Bus transactions

The NCA9535 is an I<sup>2</sup>C-bus slave device. Data is exchanged between the master and NCA9535 through write and read commands using I<sup>2</sup>C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

## 7.1. Writing to the port registers

Data is transmitted to the NCA9535 by sending the start condition, device address and setting the read-write bit to a logic 0 (see [Fig. 3](#)). The command byte is sent after the address and determines which register will receive the data following the command byte.

Eight registers within the NCA9535 are configured to operate as four register pairs. The four pairs are input port, output port, polarity inversion, configuration registers. After sending data to one register, the next data byte is sent to the other register in the pair (see [Fig. 6](#) and [Fig. 7](#)). For example, if the first byte is sent to output port 1 (register 3), the next byte is stored in output port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers, or the host can simply update a single register.



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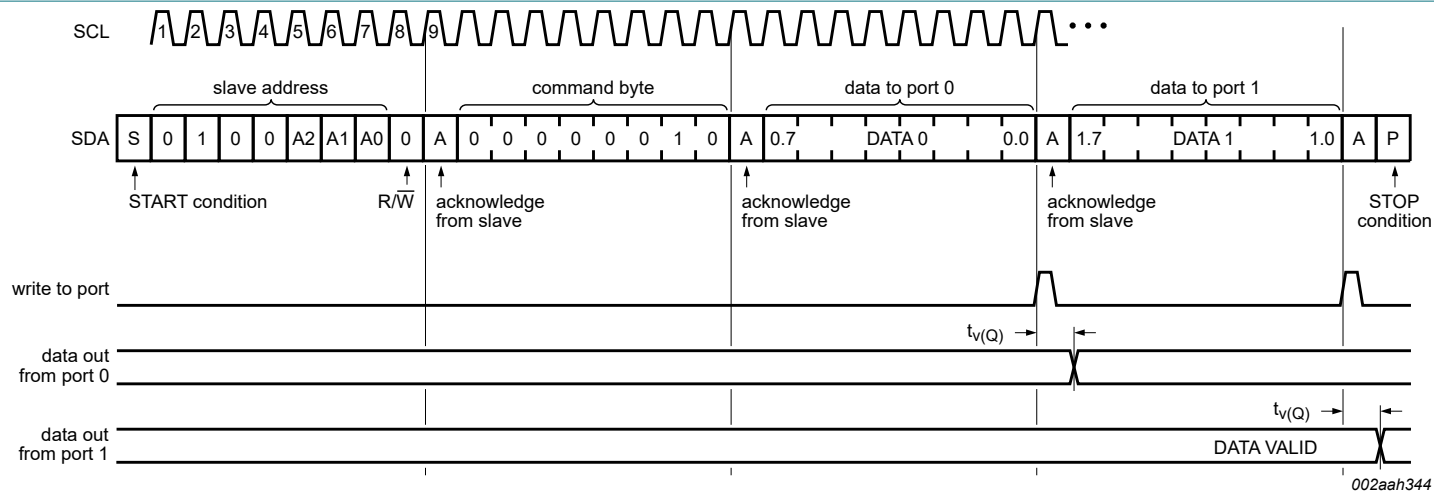


Fig. 6. Write to output port registers

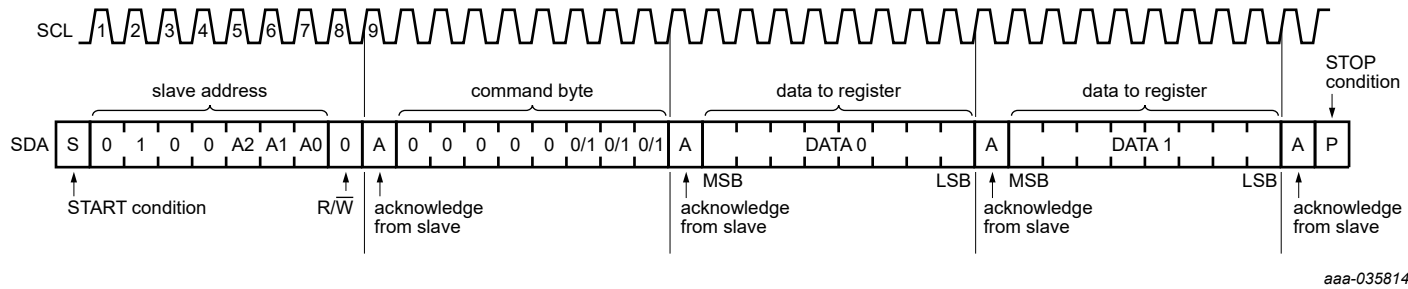


Fig. 7. Write to Control registers

### 7.2. Reading the port registers

In order to read data from the NCA9535, the bus master must first send the start condition, NCA9535 address with the read-write bit set to a logic 0 (see Fig. 3). The command byte is sent after the address and determines which register will be accessed. After a start or restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the NCA9535 (see Fig. 8, Fig. 9 and Fig. 10). Data is clocked into the register on the rising edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent start or restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.

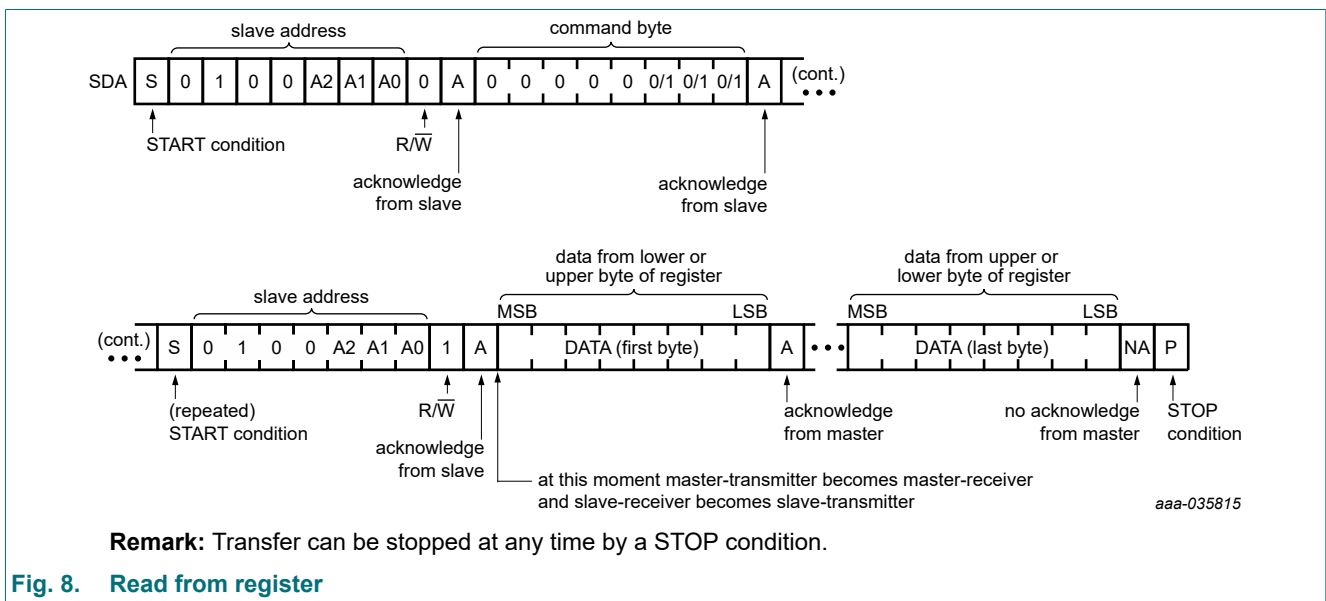
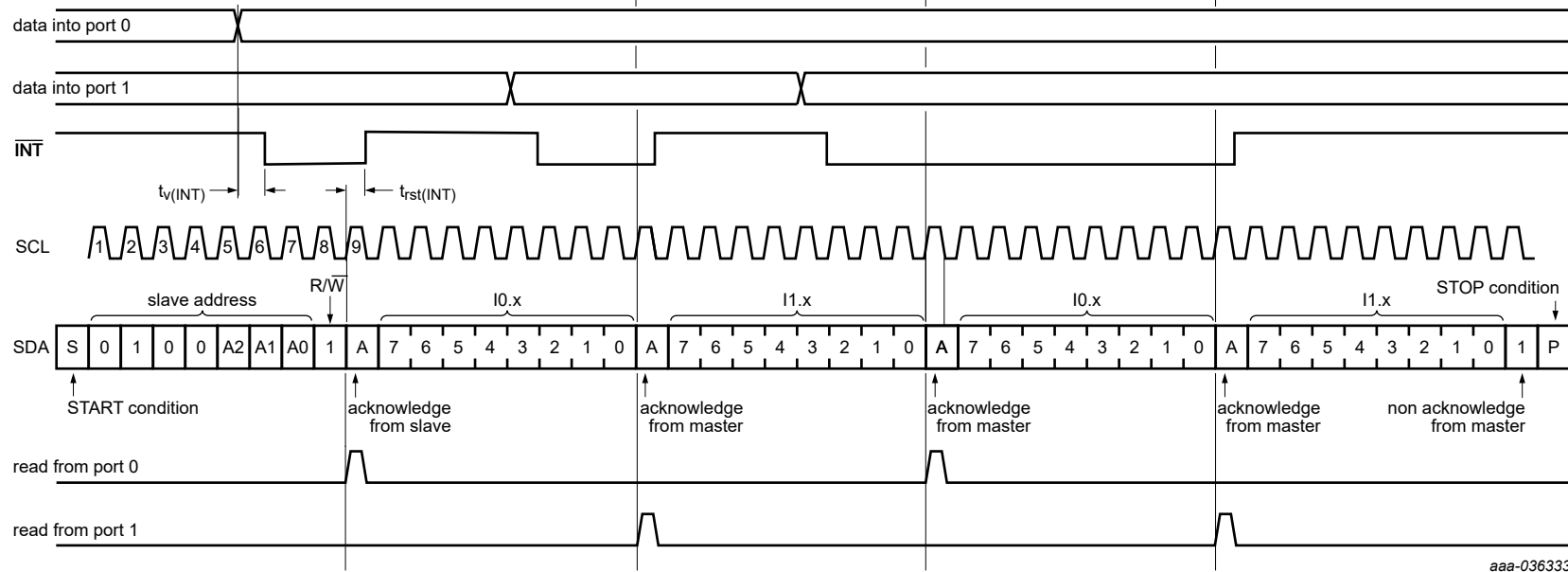


Fig. 8. Read from register

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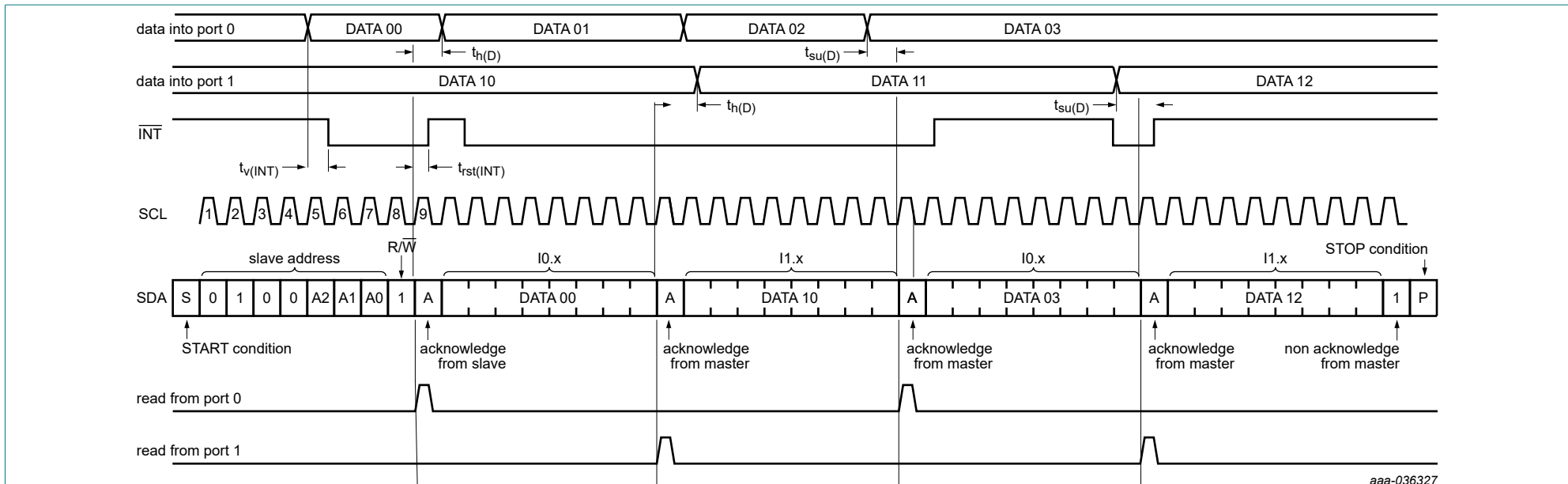
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**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00h' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial slave address call and the actual data transfer from P port (see Fig. 8).

Fig. 9. Read input port register, scenario 1

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**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00h' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial slave address call and the actual data transfer from P port (see Fig. 8).

Fig. 10. Read input port register, scenario 2

## 8. Application design-in information

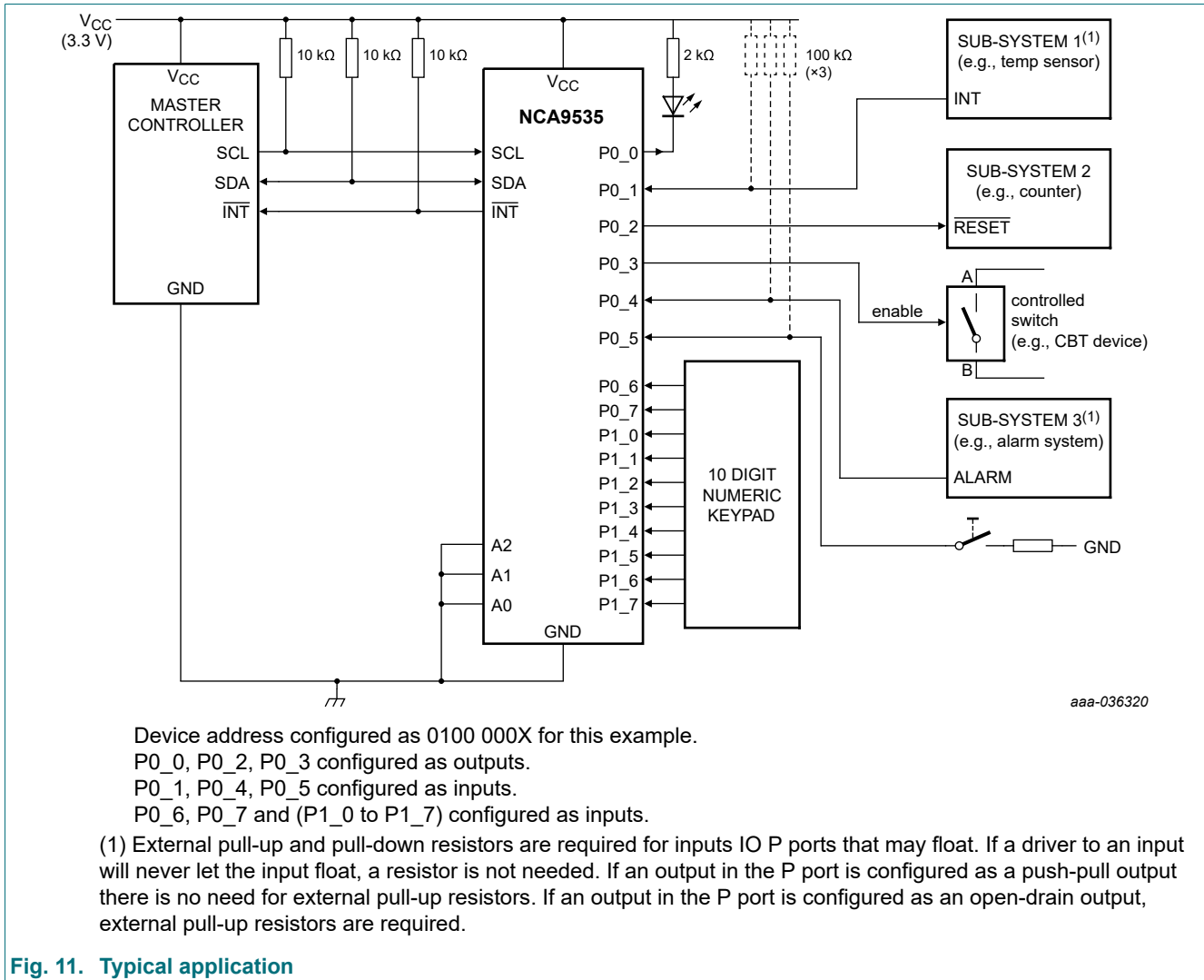


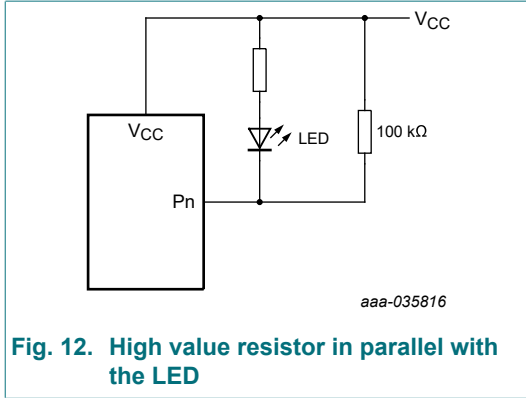
Fig. 11. Typical application

### 8.1. Minimizing $I_{CC}$ when the I/Os are used to control LEDs

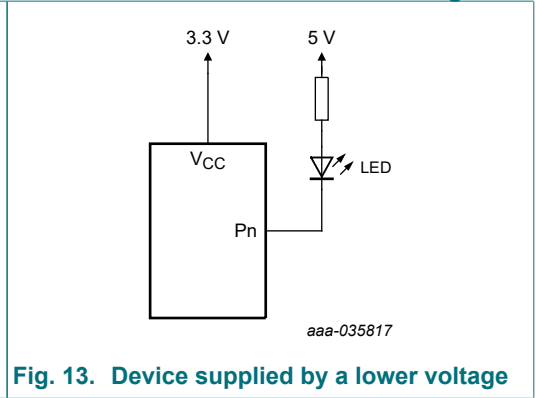
When the I/Os are used to control LEDs, they are normally connected to  $V_{CC}$  through a resistor as shown in Fig. 11. Since the LED acts as a diode, when the LED is off the I/O  $V_I$  is about 1.2 V less than  $V_{CC}$ . The supply current,  $I_{CC}$ , increases as  $V_I$  becomes lower than  $V_{CC}$ .

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to  $V_{CC}$  when the LED is off. Fig. 12 shows a high value resistor in parallel with the LED. Fig. 13 shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_I$  at or above  $V_{CC}$  and prevents additional supply current consumption when the LED is off.

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**Fig. 12. High value resistor in parallel with the LED**

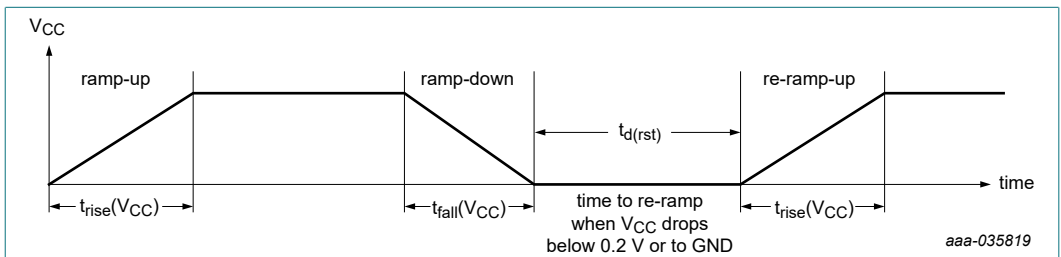


**Fig. 13. Device supplied by a lower voltage**

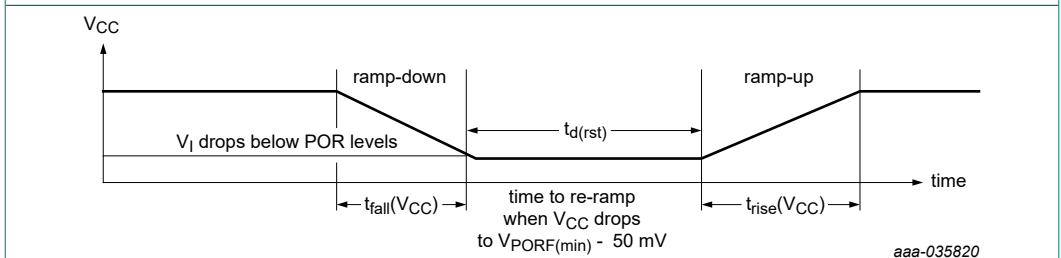
**8.2. Power-on reset requirements**

In the event of a glitch or data corruption, NCA9535 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Fig. 14](#) and [Fig. 15](#).



**Fig. 14. V<sub>CC</sub> is lowered below 0.2 V or to 0 V and then ramped up to V<sub>CC</sub>**



**Fig. 15. V<sub>CC</sub> is lowered below the POR threshold, then ramped back up to V<sub>CC</sub>**

[Table 12](#) specifies the performance of the power-on reset feature for NCA9535 for both types of power-on reset.

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Table 12. Recommended supply sequencing and ramp rates

$T_{amb} = 25\text{ °C}$  (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	$T_{amb} = 25\text{ °C}$			Unit
			Min	Typ	Max	
$t_{rise}(V_{CC})$	supply ramp up time	Fig. 14	0.1	-	2000	ms
$t_{fall}(V_{CC})$	supply ramp down time	Fig. 14	0.1	-	2000	ms
$t_{d}(rst)$	reset delay time	Fig. 14; re-ramp time when $V_{CC}$ drops below 0.2 V or to GND	1	-	-	$\mu$ s
		Fig. 15; re-ramp time when $V_{CC}$ drops to $V_{POR(min)} - 50\text{ mV}$	1	-	-	$\mu$ s
$\Delta V_{CC(gl)}$	glitch supply voltage difference	Fig. 16	-	-	1	V
$V_{CC\_MIN(gl)}$	minimum glitch supply voltage	minimum voltage that $V_{CC}$ can glitch down to, but not cause functional disruption when $t_{w(gl)}V_{CC}$ Fig. 16	1.5	-	-	V
$t_{w(gl)}V_{CC}$	supply voltage glitch pulse width	Fig. 16	-	-	10	$\mu$ s

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $t_{w(gl)}V_{CC}$ ) and glitch height ( $\Delta V_{CC(gl)}$ ) are dependent on each other. The glitch on power supply should never go below  $V_{CC\_MIN(gl)}$  in order to properly guarantee functionality. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Fig. 16 and Table 12 provide more information on how to measure these specifications.

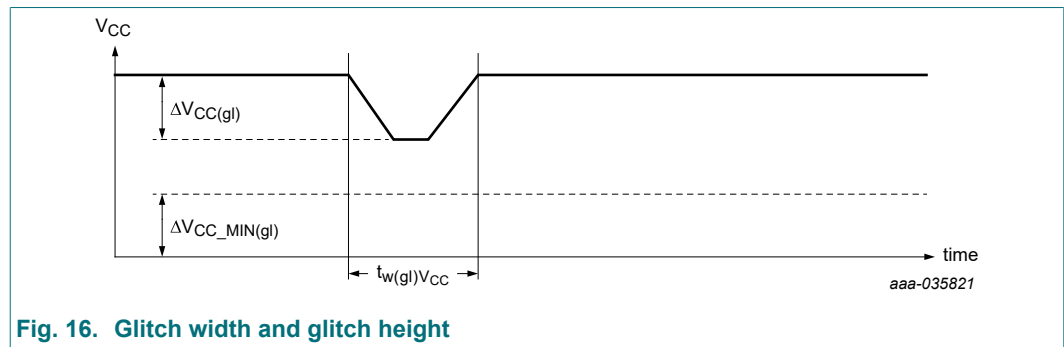


Fig. 16. Glitch width and glitch height

$V_{PORR}$  and  $V_{PORF}$  are critical to the power-on reset.  $V_{PORR}$  is the voltage level of  $V_{CC}$  at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states.  $V_{PORF}$  is the voltage level of  $V_{CC}$  below which NCA9535 enters reset state. Fig. 17 and Section 12 provide more details on this specification.

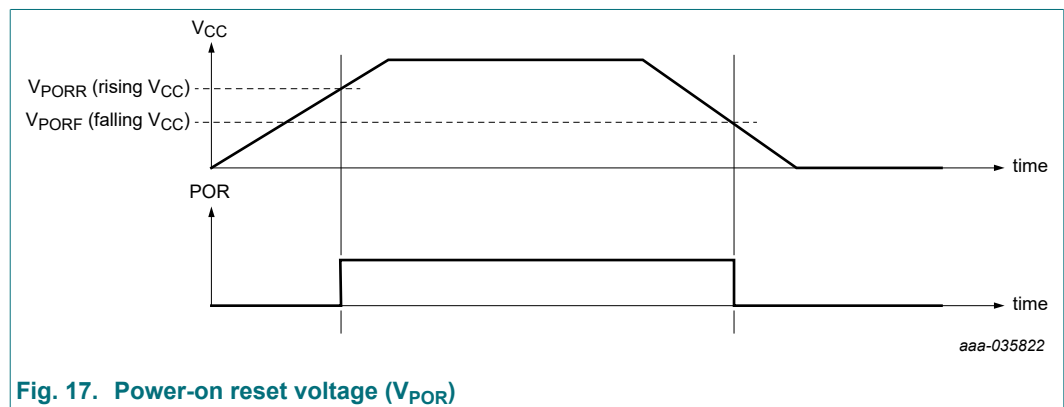


Fig. 17. Power-on reset voltage ( $V_{POR}$ )

## 9. Limiting values

**Table 13. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	6	V
V <sub>I</sub>	input voltage	[1]	-0.5	6	V
V <sub>O</sub>	output voltage	[1]	-0.5	6	V
I <sub>IK</sub>	input clamping current	A0, A1, A2, SCL; V <sub>I</sub> < 0 V	-	-20	mA
I <sub>OK</sub>	output clamping current	INT; V <sub>O</sub> < 0 V	-	-20	mA
I <sub>IOK</sub>	input/output clamping current	P port; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub>	-	±20	mA
		SDA; V <sub>O</sub> < 0 V	-	-20	mA
I <sub>OL</sub>	LOW-level output current	continuous; I/O port	-	50	mA
		continuous; SDA, INT	-	25	mA
I <sub>OH</sub>	HIGH-level output current	continuous; P port	-	25	mA
I <sub>CC</sub>	supply current		-	160	mA
I <sub>GND</sub>	ground supply current		-	250	mA
P <sub>tot</sub>	total power dissipation		-	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j(max)</sub>	maximum junction temperature		-	100	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 10. Recommended operating conditions

**Table 14. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	5.5	V
V <sub>IH</sub>	HIGH-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	5.5	V
		P1_7 to P0_0	0.7 × V <sub>CC</sub>	5.5	V
		A0, A1, A2,	0.7 × V <sub>CC</sub>	V <sub>CC</sub>	V
V <sub>IL</sub>	LOW-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>CC</sub>	V
		A0, A1, A2, P1_7 to P0_0	-0.5	0.3 × V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH-level output current	P1_7 to P0_0	-	10	mA
I <sub>OL</sub>	LOW-level output current	P1_7 to P0_0	-	25	mA
T <sub>amb</sub>	ambient temperature	operating in free air	-40	+85	°C

## 11. Thermal characteristics

**Table 15. Thermal characteristics**

Symbol	Parameter	Conditions	Max	Unit
Z <sub>th(j-a)</sub>	transient thermal impedance from junction to ambient	TSSOP24 package [1]	100	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.



## 12. Static characteristics

**Table 16. Static characteristics**
 $V_{CC} = 1.65\text{ V to }5.5\text{ V}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit	
			Min	Typ [1]	Max		
V <sub>IK</sub>	input clamping voltage	I <sub>I</sub> = -18 mA	-1.2	-	-	V	
V <sub>PORF</sub>	power-on reset trip voltage; V <sub>CC</sub> falling	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 mA	0.85	1.1	-	V	
V <sub>PORR</sub>	power-on reset trip voltage; V <sub>CC</sub> rising	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 mA	-	1.25	1.55	V	
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V; V <sub>CC</sub> = 1.65 V to 5.5 V					
		SDA	3	-	-	mA	
		INT	3	28 [2]	-	mA	
		P port					
		V <sub>OL</sub> = 0.5 V; V <sub>CC</sub> = 1.65 V	[3]	8	-	-	mA
		V <sub>OL</sub> = 0.7 V; V <sub>CC</sub> = 1.65 V	[3]	10	-	-	mA
		V <sub>OL</sub> = 0.5 V; V <sub>CC</sub> = 2.3 V	[3]	8	-	-	mA
		V <sub>OL</sub> = 0.7 V; V <sub>CC</sub> = 2.3 V	[3]	10	-	-	mA
		V <sub>OL</sub> = 0.5 V; V <sub>CC</sub> = 3.0 V	[3]	8	-	-	mA
		V <sub>OL</sub> = 0.7 V; V <sub>CC</sub> = 3.0 V	[3]	10	-	-	mA
		V <sub>OL</sub> = 0.5 V; V <sub>CC</sub> = 4.5 V	[3]	8	-	-	mA
V <sub>OL</sub> = 0.7 V; V <sub>CC</sub> = 4.5 V	[3]	10	-	-	mA		
V <sub>OH</sub>	HIGH-level output voltage	P port					
		I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 1.65 V	[4]	1.2	-	-	V
		I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 1.65 V	[4]	1.1	-	-	V
		I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	[4]	2.0	-	-	V
		I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 2.3 V	[4]	1.9	-	-	V
		I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 3.0 V	[4]	2.6	-	-	V
		I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 3.0 V	[4]	2.5	-	-	V
		I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 4.5 V	[4]	4.1	-	-	V
I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 4.5 V	[4]	4.0	-	-	V		
V <sub>OL</sub>	LOW-level output voltage	P port; I <sub>OL</sub> = 8 mA					
		V <sub>CC</sub> = 1.65 V		-	-	0.45	V
		V <sub>CC</sub> = 2.3 V		-	-	0.30	V
		V <sub>CC</sub> = 3.0 V		-	-	0.25	V
		V <sub>CC</sub> = 4.5 V		-	-	0.2	V
I <sub>I</sub>	input current	V <sub>CC</sub> = 1.65 V to 5.5 V					
		SCL, SDA; V <sub>I</sub> = V <sub>CC</sub> or GND		-	-	1	μA
		A0, A1, A2; V <sub>I</sub> = V <sub>CC</sub> or GND		-	-	±1	μA
I <sub>IH</sub>	HIGH-level input current	P port; V <sub>I</sub> = V <sub>CC</sub> ; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	1	μA	
I <sub>IL</sub>	LOW-level input current	P port; V <sub>I</sub> = GND; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	-1	μA	

registers

**Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers**

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
I <sub>CC</sub>	supply current	SDA, P port, A0, A1, A2; V <sub>I</sub> on SDA = V <sub>CC</sub> or GND; V <sub>I</sub> on P port and A0, A1, A2 = V <sub>CC</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 400 kHz (t <sub>r</sub> , =, 30, ns)				
		V <sub>CC</sub> = 3.6 V to 5.5 V	-	13	28	μA
		V <sub>CC</sub> = 2.3 V to 3.6 V	-	6.4	11	μA
		V <sub>CC</sub> = 1.65 V to 2.3 V	-	3	5.5	μA
		SCL, SDA, P port, A0, A1, A2; V <sub>I</sub> on SCL, SDA = V <sub>CC</sub> or GND; V <sub>I</sub> on P port and A0, A1, A2 = V <sub>CC</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 0 kHz				
		V <sub>CC</sub> = 3.6 V to 5.5 V	-	1.5	2.5	μA
		V <sub>CC</sub> = 2.3 V to 3.6 V	-	0.95	1.6	μA
		V <sub>CC</sub> = 1.65 V to 2.3 V	-	0.5	1.2	μA
		Active mode; P port, A0, A1, A2; V <sub>I</sub> on P port, A0, A1, A2 = V <sub>CC</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 400 kHz (t <sub>r</sub> , =, 30, ns), continuous register read				
		V <sub>CC</sub> = 3.6 V to 5.5 V	-	15	55	μA
		V <sub>CC</sub> = 2.3 V to 3.6 V	-	7.4	22	μA
		V <sub>CC</sub> = 1.65 V to 2.3 V	-	3.5	9	μA
ΔI <sub>CC</sub>	additional quiescent supply current	SCL, SDA; one input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	4.5	μA
		P port, A0, A1, A2; one input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	13	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 1.65 V to 5.5 V	-	1.5	2.5	pF
C <sub>io</sub>	input/output capacitance	V <sub>I/O</sub> = V <sub>CC</sub> or GND; V <sub>D</sub> = 1.65 V to 5.5 V	-	3	4.5	pF

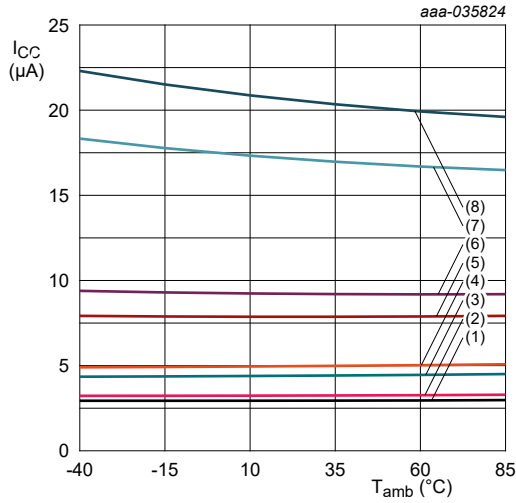
[1] For I<sub>CC</sub>, all typical values are at nominal supply voltage (1.8 V, 3.3 V or 5 V V<sub>CC</sub>) and T<sub>amb</sub> = 25 °C. Except for I<sub>CC</sub>, the typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

[2] Typical value for T<sub>amb</sub> = 25 °C. V<sub>OL</sub> = 0.4 V and V<sub>CC</sub> = 3.3 V.

[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 200 mA.

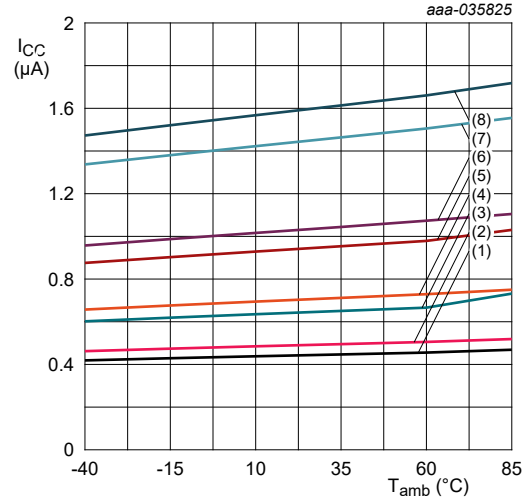
[4] The total current sourced by all I/Os must be limited to 160 mA.

12.1. Typical characteristics



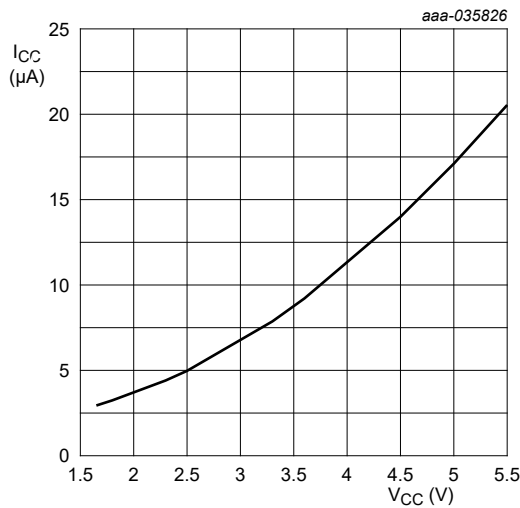
$f_{SCL} = 400 \text{ kHz}$   
 (1)  $V_{CC} = 1.65 \text{ V}$   
 (2)  $V_{CC} = 1.8 \text{ V}$   
 (3)  $V_{CC} = 2.3 \text{ V}$   
 (4)  $V_{CC} = 2.5 \text{ V}$   
 (5)  $V_{CC} = 3.3 \text{ V}$   
 (6)  $V_{CC} = 3.6 \text{ V}$   
 (7)  $V_{CC} = 5.0 \text{ V}$   
 (8)  $V_{CC} = 5.5 \text{ V}$

Fig. 18. Supply current versus ambient temperature



(1)  $V_{CC} = 1.65 \text{ V}$   
 (2)  $V_{CC} = 1.8 \text{ V}$   
 (3)  $V_{CC} = 2.3 \text{ V}$   
 (4)  $V_{CC} = 2.5 \text{ V}$   
 (5)  $V_{CC} = 3.3 \text{ V}$   
 (6)  $V_{CC} = 3.6 \text{ V}$   
 (7)  $V_{CC} = 5.0 \text{ V}$   
 (8)  $V_{CC} = 5.5 \text{ V}$

Fig. 19. Standby supply current versus ambient temperature



$T_{amb} = 25 \text{ °C}; f_{SCL} = 400 \text{ kHz}$

Fig. 20. Supply current versus supply voltage

Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

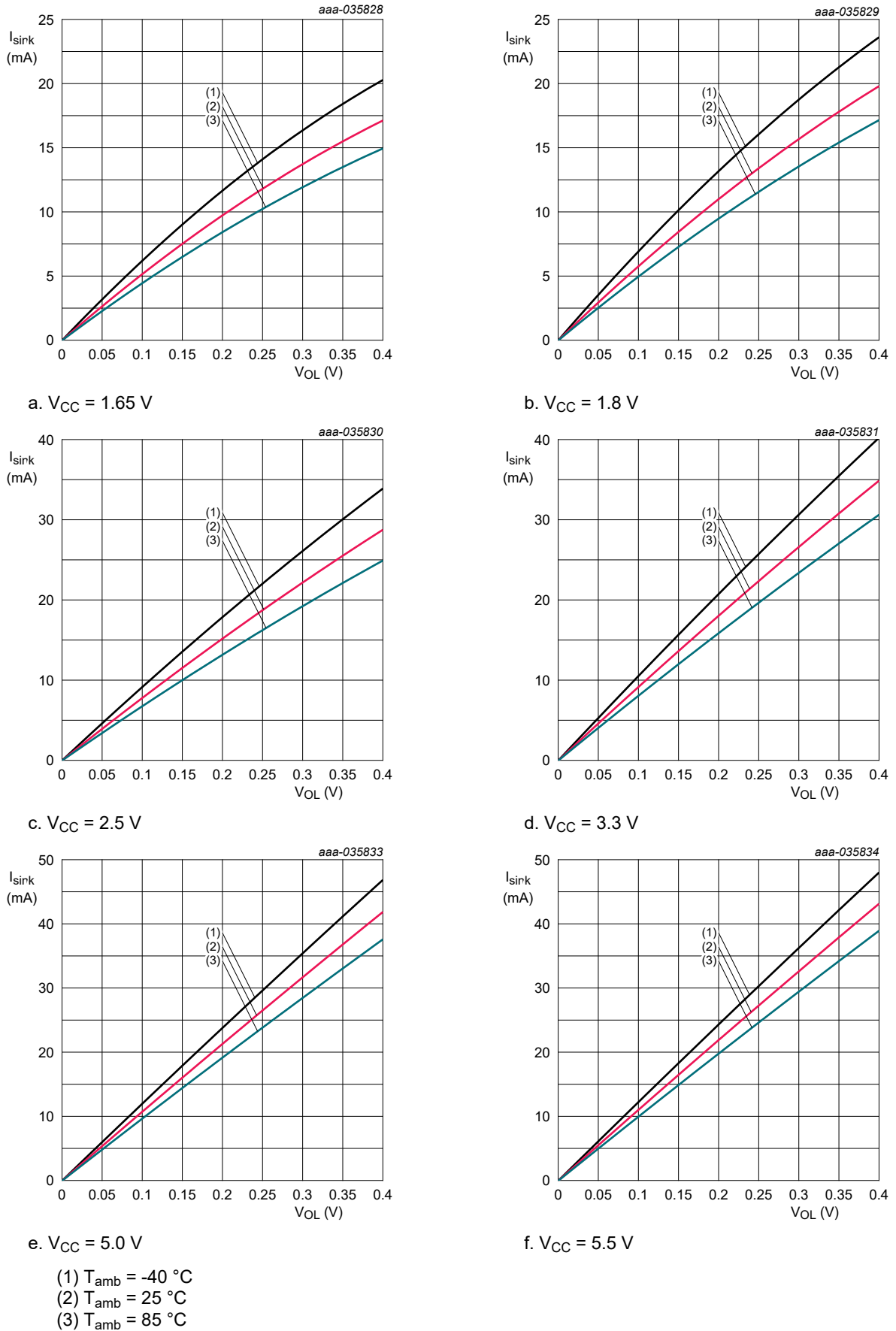


Fig. 21. I/O sink current versus LOW-level output voltage

Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

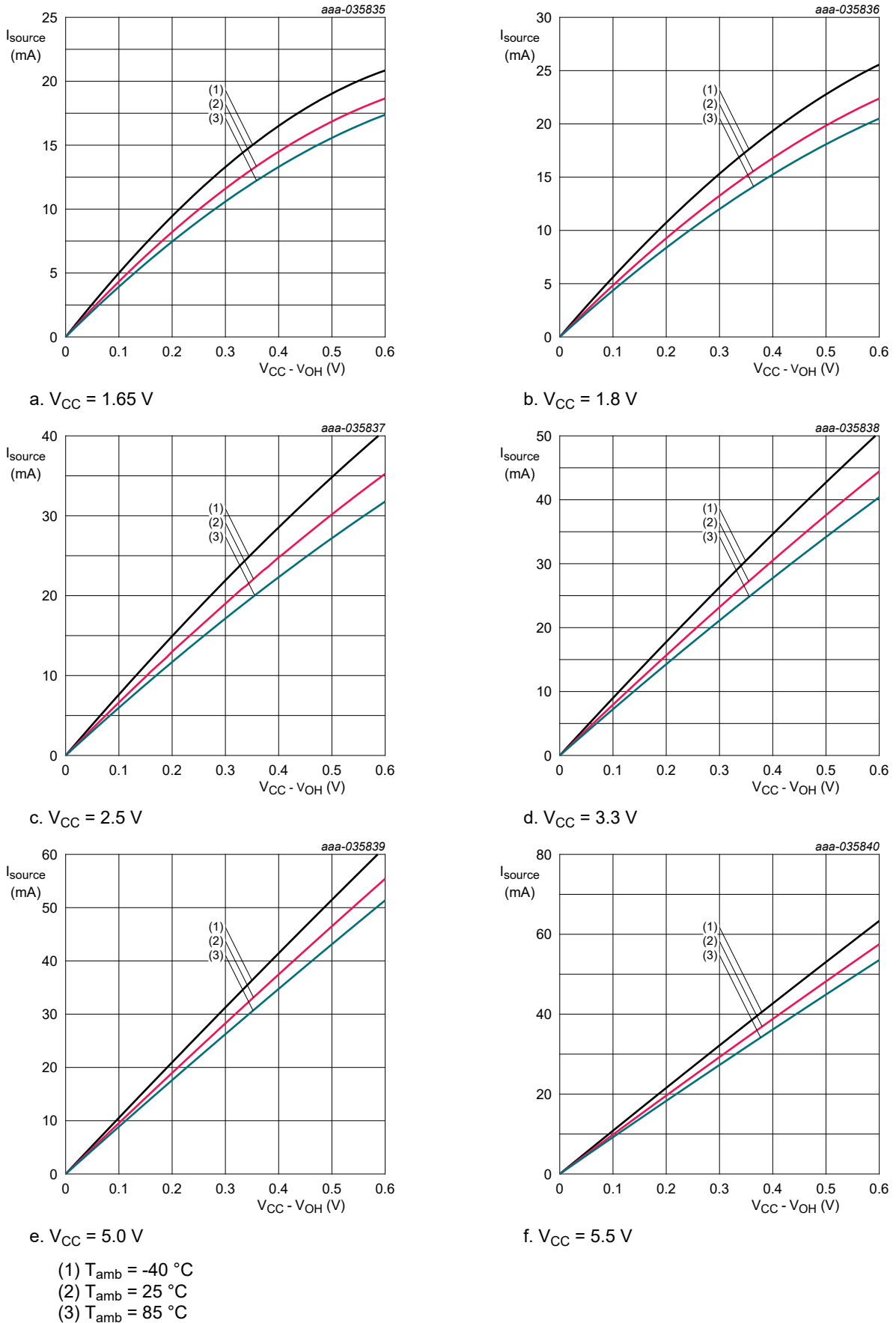


Fig. 22. I/O source current versus HIGH-level output voltage

Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

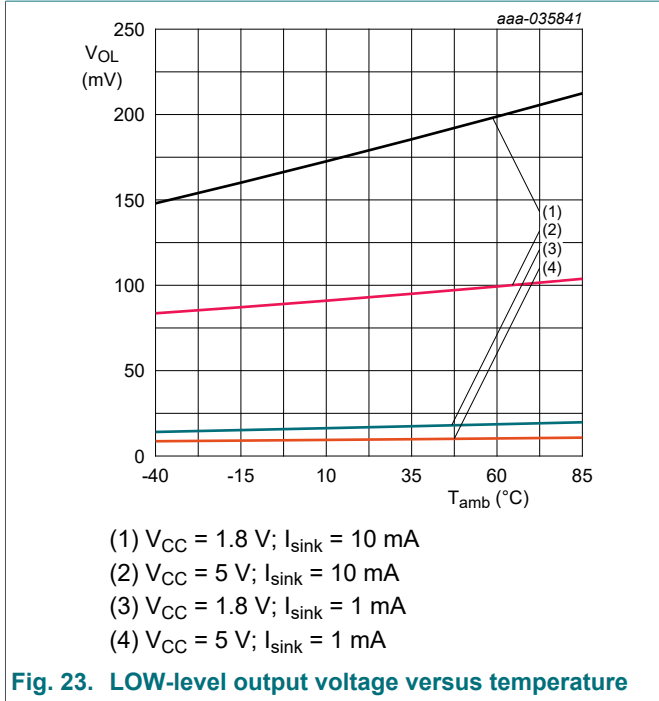


Fig. 23. LOW-level output voltage versus temperature

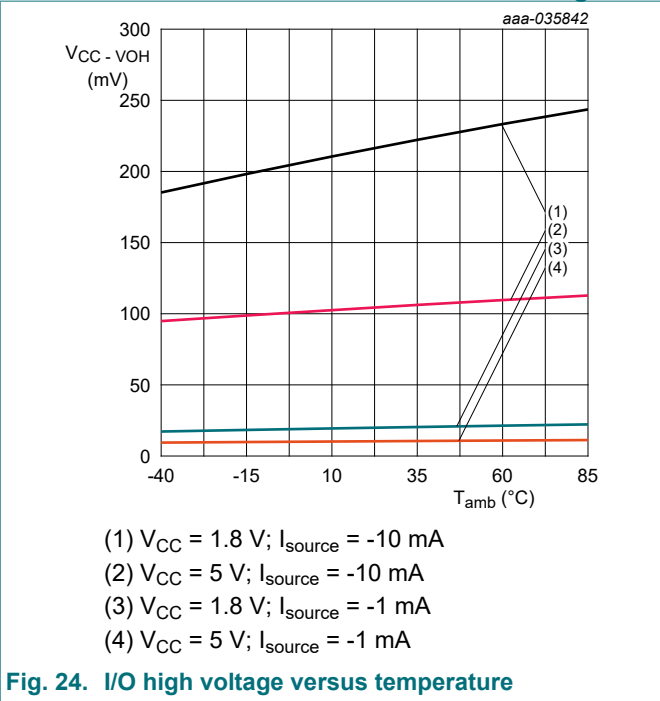


Fig. 24. I/O high voltage versus temperature

### 13. Dynamic characteristics

Table 17. I<sup>2</sup>C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Fig. 25.

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency		0	100	0	400	kHz
$t_{HIGH}$	HIGH period of the SCL clock		4	-	0.6	-	µs
$t_{LOW}$	LOW period of the SCL clock		4.7	-	1.3	-	µs
$t_{SP}$	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU,DAT}$	data set-up time		250	-	100	-	ns
$t_{HD,DAT}$	data hold time		0	-	0	-	ns
$t_r$	rise time of both SDA and SCL signals		-	1000	20	300	ns
$t_f$	fall time of both SDA and SCL signals		-	300	$20 \times (V_{CC}/5.5\text{ V})$	300	ns
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU,STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD,STA}$	hold time (repeated) START condition		4	-	0.6	-	µs
$t_{SU,STO}$	set-up time for STOP condition		4	-	0.6	-	µs
$t_{VD,DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	µs
$t_{VD,ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	µs

Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

Table 18. Switching characteristics

Over recommended operating free air temperature range;  $C_L \leq 100$  pF; unless otherwise specified. See Fig. 26.

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$t_{V(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	$\mu$ s
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	$\mu$ s
$t_{V(Q)}$	data output valid time	from SCL to P port	-	300	-	300	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	-50	-	-50	-	ns
$t_h(D)$	data input hold time	from P port to SCL	240	-	240	-	ns

14. Parameter measurement information

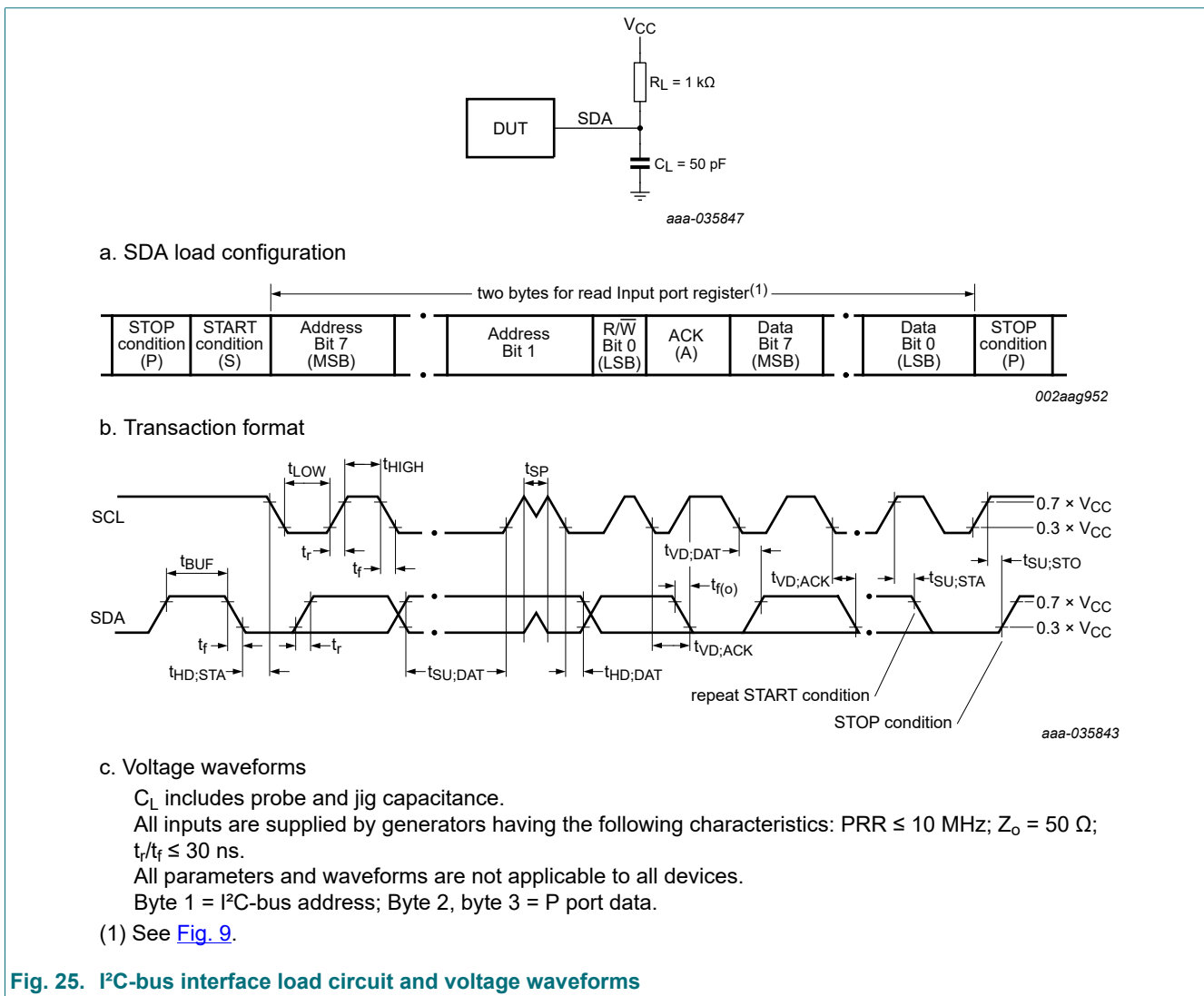


Fig. 25. I<sup>2</sup>C-bus interface load circuit and voltage waveforms

Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

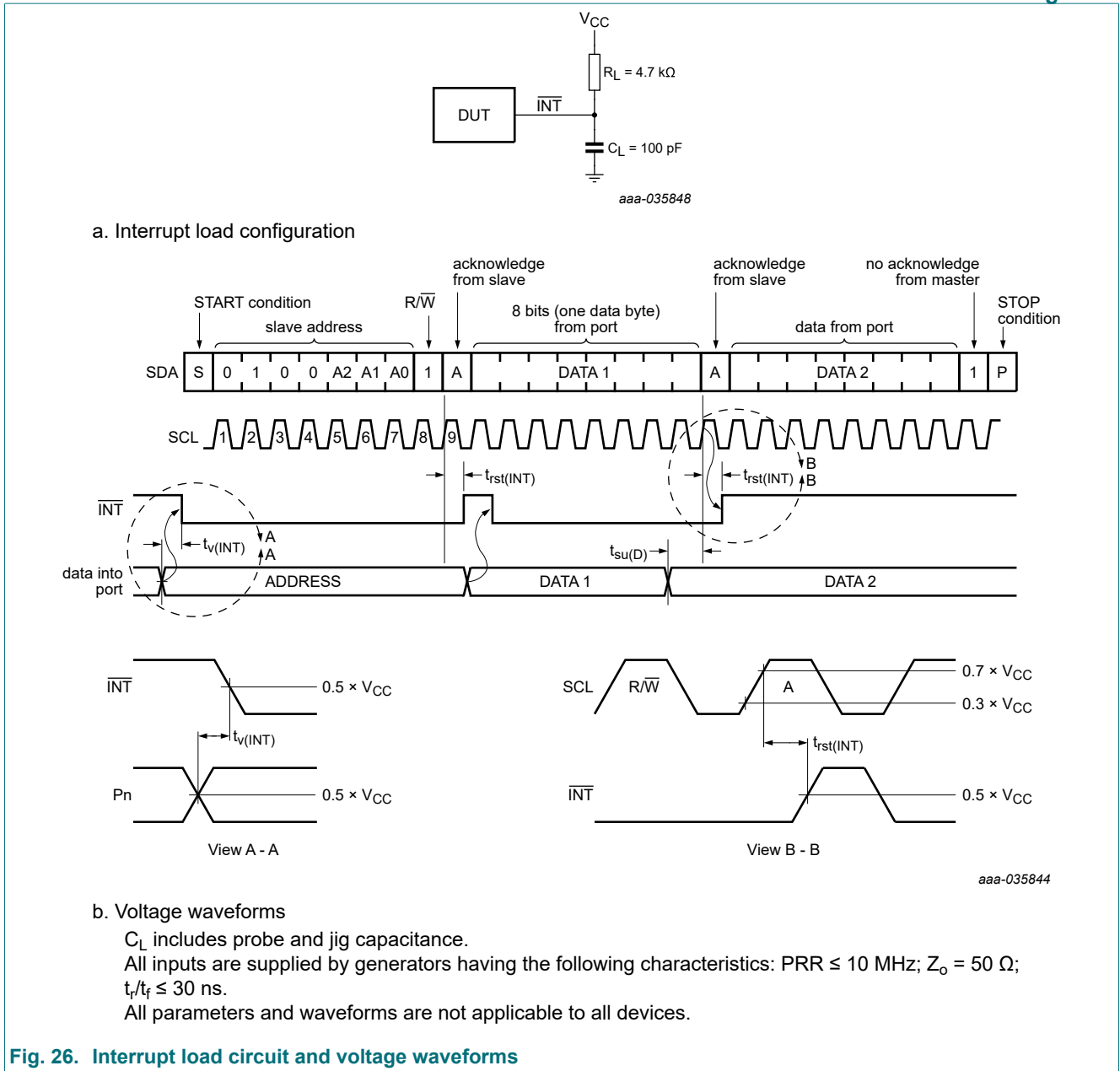


Fig. 26. Interrupt load circuit and voltage waveforms



Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

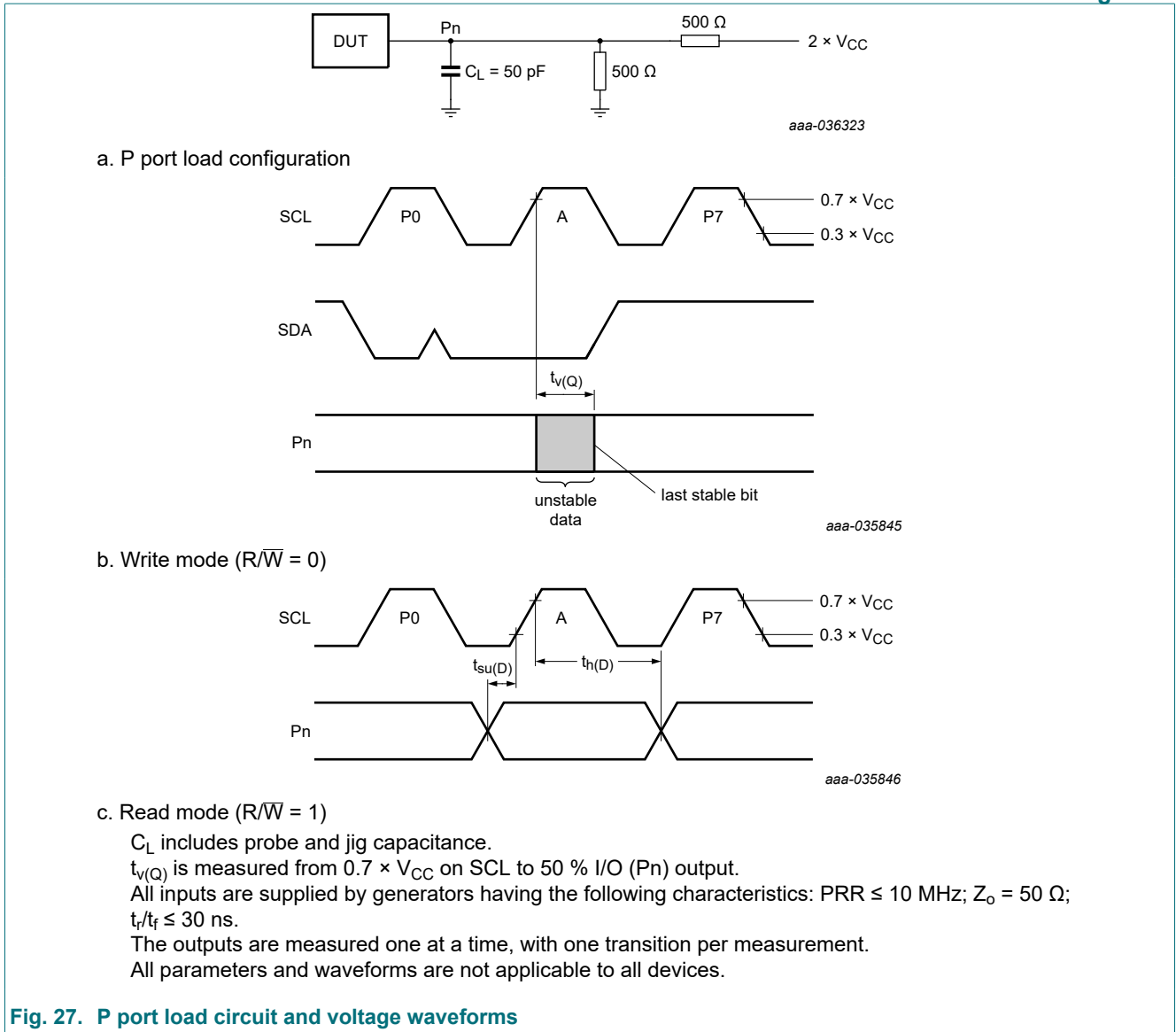


Fig. 27. P port load circuit and voltage waveforms

### 15. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

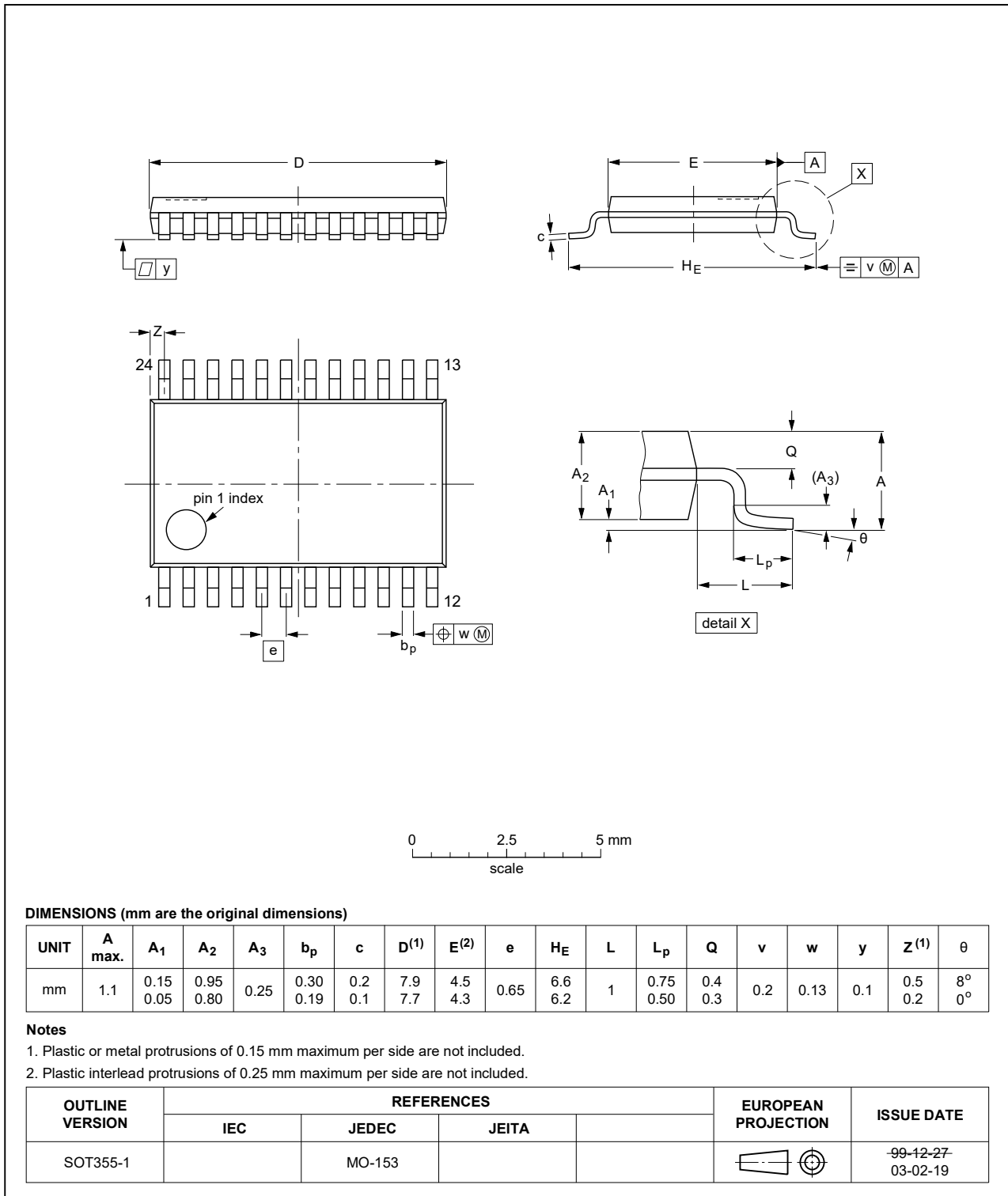


Fig. 28. Package outline SOT355-1 (TSSOP24)

## 16. Abbreviations

Table 19. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
SMBus	System Management Bus

## 17. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA9535 v.1	20230331	Product data sheet	-	-

## Low-voltage 16-bit I<sup>2</sup>C and SMBus low-power I/O expander with interrupt output and configuration registers

### 18. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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 Date of release: 31 March 2023