SLVS406B – JUNE 2002 – REVISED JUNE 2003

27-LINE LVD ONLY SCSI TERMINATOR FOR SPI-5

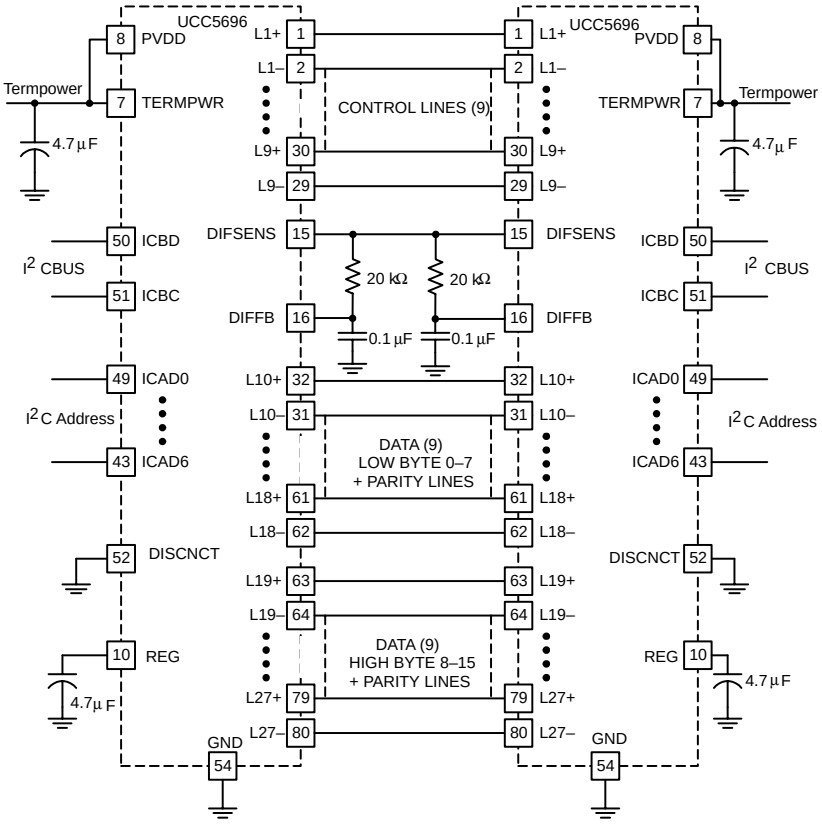
FEATURES

- **Meets Ultra2 (SPI-2 LVD SCSI), Ultra3, Ultra 160 (SPI-3), Ultra320 (SPI-4), and Ultra640 (SPI-5) Standards**
- **2.7-V to 5.25-V Termpwr Operation**
- **Differential Fail-Safe Bias**
- **I²C Bus Adjustable Impedance and Differential Bias Current**
- **80-Pin Low Profile Quad Flat Pack Package (QFP)**

DESCRIPTION

The UCC5696 is a 27-line LVD only SCSI programmable terminator. The nominal settings on power up are compliant to SPI-2 through SPI-4. The programmable settings are used for SPI-5. The UCC5696 uses the I²C to program the differential impedance and the differential bias current. The differential impedance is programmed in 5-Ω increments from 55 Ω to 130 Ω using 4 bits (16 steps). The differential bias current is programmed in 50 µA from 0.7 mA to 1.45 mA using 4 bits (16 steps). The UCC5696 has the SPI-3 mode change delay, the typical value is 200 ms.

APPLICATION DIAGRAM



UDG–01093

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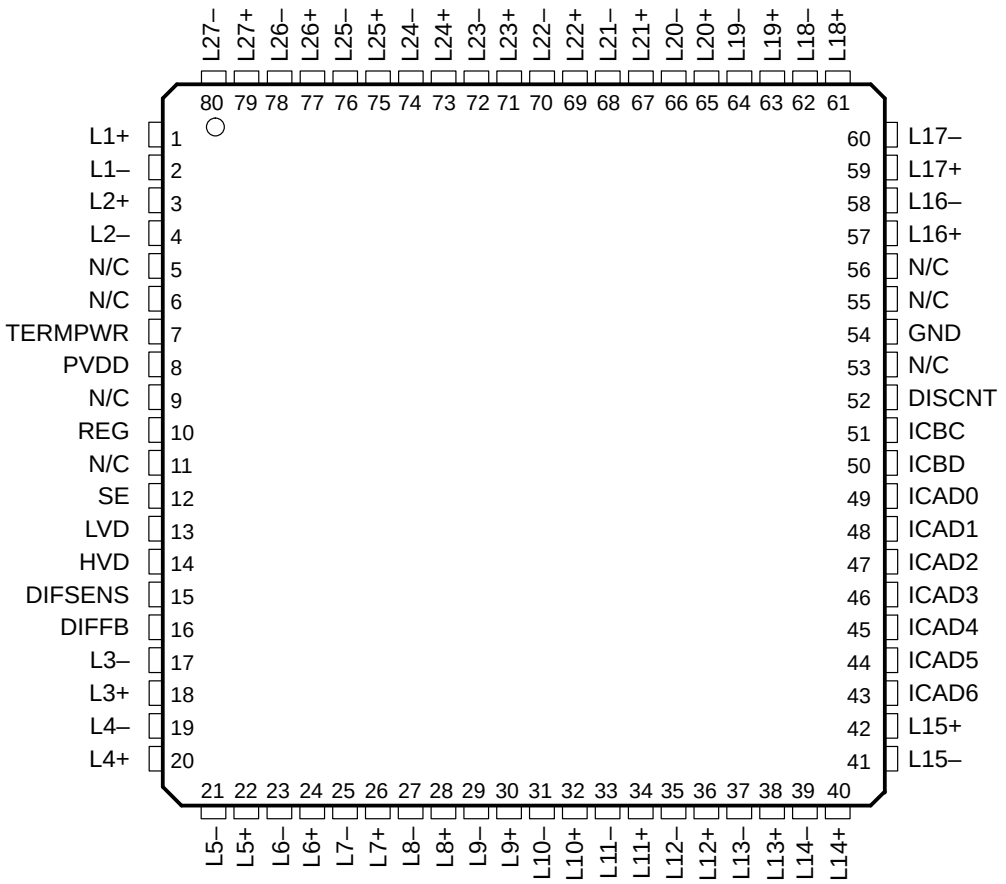
DESCRIPTION (CONTINUED)

The UCC5696 can not be used for single-ended or HVD SCSI, the termination lines will open when it detects either single-ended or HVD devices on the SCSI bus.

ORDERING INFORMATION

PN PACKAGE
(TOP VIEW)



NOTE: N/C No connect

AVAILABLE OPTIONS

T_A	Disconnect Status	Packaged Devices
		LQFP
0°C to 70°C	Regular	UCC5696PN

† LQFP (PN) package is available taped and reeled. Add R suffix to device type (e.g. UCC5696PNR) to order quantities of 1000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)†

Parameter	UCC5696	UNIT
TERMPWR voltage	6	V
Signal line voltage	0 to 6	V
Package power dissipation	1	W
Operating junction temperature, T_J	–55 to 150	°C
Storage temperature, T_{stg}	–65 to 150	°C
Lead temperature (soldering, 10 sec.), T_{sol}	300	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage are with respect to ground. Currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

TERMPWR voltage . . . . . 2.7 V to 5.25 V

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TERMPWR = 2.7 V to 5.25 V, (unless otherwise specified, the measurements are specified at the default impedance and bias current)

TERMPWR supply current

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
TERMPWR supply current	(No load)			65	mA
	Disabled terminator			2.5	
TERMPWR voltage		2.7		5.25	V

regulator

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
1.25-V regulator	LVD mode, 0.5 V ≤ V_{CM} ≤ 2.0 V, all lines loaded	1.15	1.25	1.35	V
1.3-V regulator	Differential sense, –5 mA ≤ $I_{DIFSENS}$ ≤ 50 μA	1.2	1.3	1.4	V
1.25-V regulator source current	LVD mode, V_{REG} = 0 V	–250	–300		mA
1.25-V regulator sink current	LVD mode, V_{REG} = 3.3 V	250	300		mA
1.3-V regulator source current	Differential sense, $V_{DIFSENS}$ = 0 V	–5		–15	mA
1.3-V regulator sink current	Differential sense, $V_{DIFSENS}$ = 2.75 V	50		200	μA

NOTES: 1. At powerup or after the device comes out of disconnect mode.
2. For SPI-2, SPI-3 and SPI-4.
3. Ensured by design and engineering test, but not production tested.
4. Current is the absolute value of current as some addresses are pulled high, while others are pulled low.

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TERMPWR = 2.7 V to 5.25 V, (unless otherwise specified, the measurements are specified at the default impedance and bias current)

differential termination (default)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Differential impedance (1)	Default	100	105	110	Ω
Differential impedance steps	Steps 5, 10, 20, 40 Ω, 14% overall accuracy	55		130	Ω
	55 Ω	47.5	55	62.5	
	130 Ω	112	130	147	
	The difference between all lines at any step			10	
Common mode impedance (1)	Default	100		300	Ω
	Over the impedance adjustment range	75		400	
Differential bias voltage (2)	Default I^2C settings	100		125	mV
Differential bias current (1)	Default	1		1.1	mA
	Steps 0.05, 0.1, 0.2, 0.4 mA, 14% overall accuracy	0.70		1.45	
	0.7 mA	0.6	0.7	0.8	
	1.45 mA	1.25	1.45	1.65	
Output leakage	Disabled, TERMPWR 0 V < 5.25 V			400	nA
Output capacitance (3)	Single ended measurement to ground			3	pF

disconnect and diff sense input

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DISCNT threshold		0.8		2.0	V
Input current DISCNT			10	30	µA
Input current, ICBC, ICBD		–1		1	µA
Input current, ICAD0–6 (4)			10	30	µA
Input current DIFF B	$0 V \le V_{DIFFB} \le 2.75 V$	–1		1	µA
DIFF B single ended to LVD threshold		0.5		0.7	V
DIFF B LVD to HPD threshold		1.9		2.4	V

time delay/filter

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Mode change delay (2)		100	190	310	ms

status line output characteristics

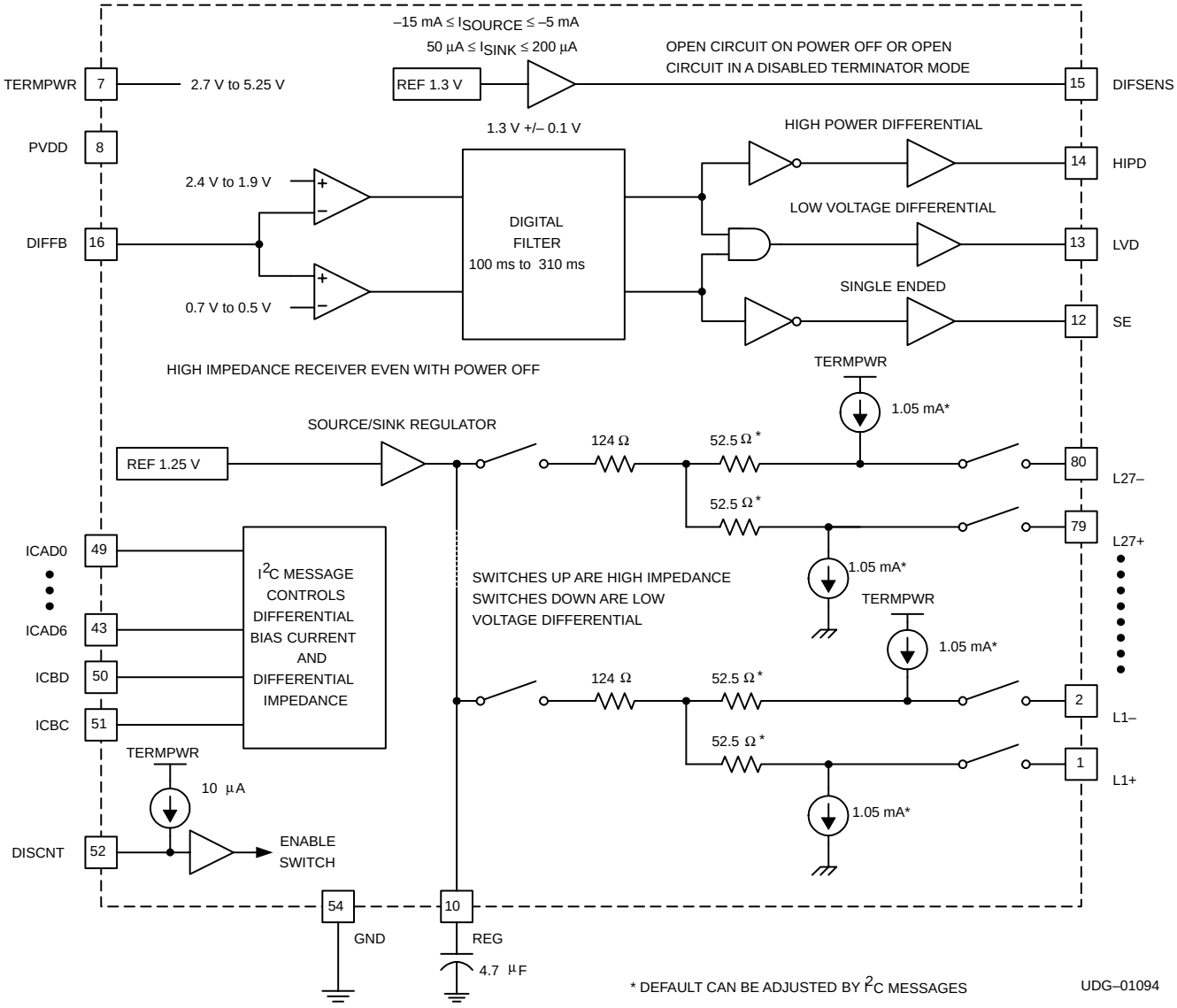
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Source current	V_{LOAD} = 2.4 V	–4	–6		mA
Sink current	V_{LOAD} = 0.4 V	2	5		mA

NOTES: 1. At powerup or after the device comes out of disconnect mode.
2. For SPI-2, SPI-3 and SPI-4.
3. Ensured by design and engineering test, but not production tested.
4. Current is the absolute value of current as some addresses are pulled high, while others are pulled low.

Terminal Functions

TERMINAL			FUNCTION
NAME	NO.	I/O	
DIFSENS	15	O	The SCSI bus DIFF SENSE line detects what types of devices are connected to the SCSI bus.
DISCNT	52	I	The disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.
DIFFB	16	I	Senses the bus mode, a 50-Hz filter is required, 0.1 μF to ground and 20 kΩ to the SCSI bus DIFF SENSE line with internal SPI-3 100-ms to 310-ms delay.
HVD	14	O	A high-voltage differential voltage level has been detected on the DIFF B pin. HVD pin high indicates that the terminator is in high impedance mode.
ICBD	50	I/O	I^2C bus data. Serial control for impedance and bias current adjustments.
ICBC	51	I	I^2C bus clock.
ICAD0–6		I	I^2C address.
Line n–		O	Negative line for differential applications of the SCSI bus.
Line n+		O	Positive line for differential applications of the SCSI bus.
LVD	13	O	A low-voltage differential voltage level has been detected on the DIFF B pin. LVD pin high indicates that the terminator is in LVD mode.
PVDD	8	I	Power supply for the regulator. PVDD should be tied to TERMPWR pin.
REG	10	O	Regulator bypass pin must be bypassed to ground with a 4.7-μF low ESR capacitor.
SE	12	O	A single ended voltage level has been detected on the DIFF B pin. SE pin high indicates that the terminator is in high impedance mode.
TERMPWR	7	I	V_{IN} 2.7-V to 5.25-V supply. TERMPWR should be bypassed to ground with a 4.7-μF low ESR capacitor.

block diagram



APPLICATION INFORMATION

The DIFF SENSE line is driven by the terminator and monitored by the terminator DIFF B input pin. DIFF B has a digital filter and a 100-ms to 310-ms delay before the mode of the terminator is changed to reflect the new DIFF B input level. A set of comparators that allow for ground shifts determines the bus status as follows: any DIFF SENSE signal below 0.5 V is single ended, between 0.7 V and 1.9 V is LVD SCSI, and above 2.4 V is HVD SCSI.

The UCC5696 is high-impedance in SE and HVD SCSI bus modes.

Layout is very critical for Ultra320 and Ultra640 systems. Multilayer boards need to adhere to the impedance 120-Ω standard, including connectors and feed-throughs. This is normally done on the outer layers with 4-mil etch and 4-mil spacing between the runs within a pair, and a minimum of 8-mil spacing to the next pair. The spacing between the pairs reduces potential cross-talk. Beware of feed-throughs and through-hole connectors, each of which adds a lot of capacitance. The standard power and ground plane spacing yields about 1 pF to each plane; each feed-through adds about 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance, and opening up the power and ground planes under the connector can reduce the capacitance for through hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50-Ω not 120-Ω differential systems.

Capacitance balance is critical for Ultra640; the balance capacitance is 0.5 pF per line while the balance between pairs is 2 pF. The components are designed with very tight balance, typically 0.1 pF between pins in a pair and 0.3 pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, and preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application. Materials and components above and below the circuit board effect the capacitance.

The differential impedance is adjustable to match the impedance of the backplane or cable system, adjusting for the loading change when drives are added. The high frequency roll off of the system can reduce the size of the single bit transition to less than the size of the reflected wave on a heavily loaded system. Adjusting the terminator to match the impedance of the system, which changes as drives are added, minimizes the reflection from the terminator. Ultra640 SCSI must have each segment of the bus adjusted to reduce errors, SCSI domain validation (SDV) defines the margining of the segments.

System testing has shown that reducing the terminator impedances to slightly lower than the bus impedance reduces isolated 0 and 1 bit errors and increases system performace for Ultra160, Ultra320 and Ultrra640 speeds.

In 3.3-V Termpwr systems, the UCC3912 or UCC3918 should be used to replace the diode and fuse function. This reduces the voltage drop, allowing for the cable voltage drop for the terminators on the far end of the cable. 3.3-V battery systems have a 10% tolerance, the UCC3912 or UCC3918 has less than 150-mV drop under load, allowing for 150 mV-drop in the cable system. All Texas Instrument LVD and multimode terminators are designed for 3.3-V systems, operating down to 2.7 V.

In 5-V Termpwr systems the UCC3916, UCC3912 or UCC3918 can be used to replace the diode and fuse function. These reduce the voltage drop and protect the systems better than the diode and fuse or polyfuse.

APPLICATION INFORMATION

I²C interface

The two-wire serial interface is used to access the terminator and to independently adjust both the differential impedance and the differential bias current. This interface consists of one clock line, (SCL), and one serial data line, (SDA).

The access cycle consists of the following and is shown in Figure 2:

1. A start condition
2. A slave address cycle
3. A data cycle
4. A stop condition

Figure 1. I²C Start and Stop Condition

The start and stop conditions are shown in Figure 1. The high-to-low transition of SDA while SCL is high defines the start condition. The low-to-high transition of SDA while SCL is high, defines the stop condition. The start and stop conditions are initiated by the master device.

Each cycle, data or address, consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. During the acknowledge clock pulse (the ninth clock) the transmitting device must release the SDA line. The receiving device then pulls down the SDA line so that it remains stable LOW during the HIGH period of the acknowledge clock pulse.

slave address

The slave address of the UCC5696 terminator has 8 bits consisting of 7 bits of address along with 1 bit, the LSB, reserved for the read/write information (1 for read and 0 for write). The 7-bit address is fully programmable.

APPLICATION INFORMATION

write/read

The UCC5696 operates using only a single byte transfer (a byte of address followed by a second byte for data).

Following a start condition and an address byte, the UCC5696 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle, if it is the terminator's address.

In a write cycle, after receiving a data byte, the UCC5696 pulls the SDA low for one clock cycle. A stop condition is initiated by the transmitting device after the acknowledge clock pulse. See Figure 2 for an example of a write cycle.

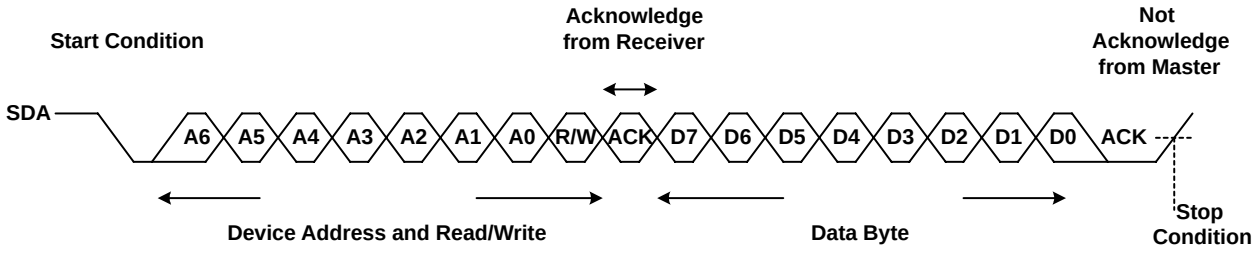


Figure 2. Write Cycle

In a read cycle, following the initial acknowledge for address, the UCC5696 becomes a transmitting device and the master device becomes the receiver. At the end of the data byte, the not acknowledge, A, condition is initiated by the master by keeping the SDA signal high before it asserts the stop condition. See Figure 3 for an example of a read cycle.

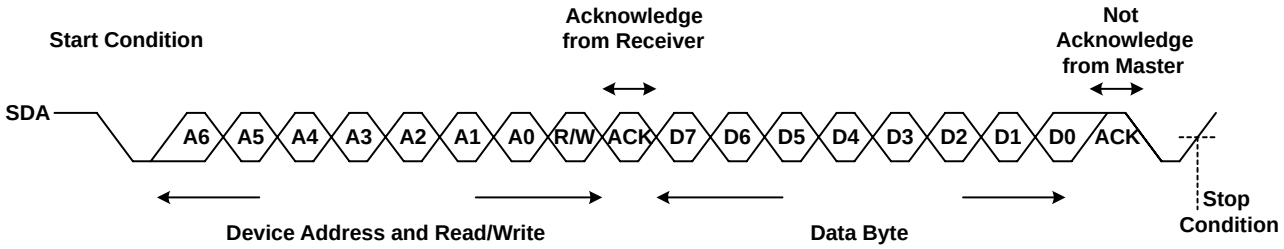


Figure 3. Read Cycle

data

Bit 7 (MSB) to bit 4 of the data byte are used to control the differential bias current. Bit 3 to bit 0 are used to control the differential impedance. At powerup both differential bias current and differential impedance are set to 1.05 mA and 105 Ω, respectively. Reference Table 1 and 2 for other current and impedance settings. All these values are nominal.

APPLICATION INFORMATION

Table 1. Differential Bias Current Settings True

DIFFERENTIAL I_{BIAS} (mA)	BIT7 (MSB)	BIT6	BIT5	BIT4
0.70	0	0	0	0
0.75	0	0	0	1
0.80	0	0	1	0
0.85	0	0	1	1
0.90	0	1	0	0
0.95	0	1	0	1
1.00	0	1	1	0
1.05 (See Note)	0	1	1	1
1.10	1	0	0	0
1.15	1	0	0	1
1.20	1	0	1	0
1.25	1	0	1	1
1.30	1	1	0	0
1.35	1	1	0	1
1.40	1	1	1	0
1.45	1	1	1	1

NOTE: Default settings

Table 2. Differential Impedance Settings True

DIFFERENTIAL IMPEDANCE (Ω)	BIT3	BIT2	BIT1	BIT0
55	0	0	0	0
60	0	0	0	1
65	0	0	1	0
70	0	0	1	1
75	0	1	0	0
80	0	1	0	1
85	0	1	1	0
90	0	1	1	1
95	1	0	0	0
100	1	0	0	1
105 (See Note)	1	0	1	0
110	1	0	1	1
115	1	1	0	0
120	1	1	0	1
125	1	1	1	0
130	1	1	1	1

NOTE: Default settings

APPLICATION INFORMATION

Table 3. Characteristics of the SDA and SCL I/O Stages for Standard/Fast-Mode

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
Termpwr voltage	V_{DD}	2.7	5.25	2.7	5.25	V
Low-level input voltage	V_{IL}	–0.5	0.3 x V_{DD}	–0.5	0.3 x V_{DD}	V
High-level input voltage	V_{IH}	0.7 x V_{DD}		0.7 x V_{DD}		V
Hyst of schmitt-trigger input	V_{HYS}	N/A	N/A	0.15		V
Low-level input at 3-mA sink	V_{OL}	0	0.4	0	0.4	V
Pulse width of spikes which must be suppressed by input filter	t_{SP}	N/A	N/A	0	50	ns

Table 4. Timing Characteristics for I^2C Interface

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
Clock frequency, SCL	f_{SCL}	0	100	0	400	kHz
Pulse duration, SCL high	$t_{W(H)}$	4	–	0.6	–	µs
Pulse duration, SCL low	$t_{W(L)}$	4.7	–	1.3	–	µs
Rise time, SCL to SDA	t_r	–	1000	–	300	ns
Fall time, SCL to SDA	t_f	–	300	–	300	ns
setup time, SDA to SCL	t_{SU1}	250	–	100	–	ns
Hold time, SCL to SDA	t_{h1}	0.30	3.45	0.30	0.90	µs
Bus free time between stop and start condition	t_{buf}	4.7	–	1.3	–	µs
Setup time, SCL to start condition	t_{SU2}	4.7	–	0.6	–	µs
Hold time, start condition to SCL	t_{h2}	4	–	0.6	–	µs
Setup time, SCL to stop condition	t_{SU2}	4	–	0.6	–	µs

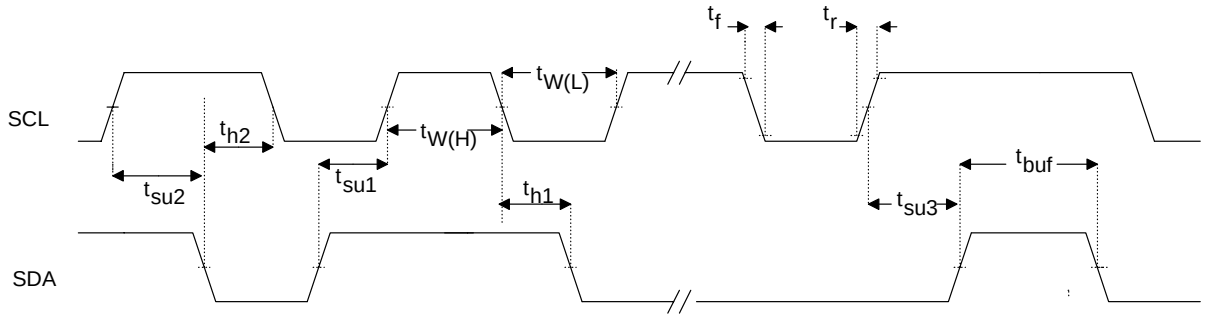


Figure 4. SCL and SDA

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC5696PN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
UCC5696PNG4	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
UCC5696PNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
UCC5696PNRG4	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

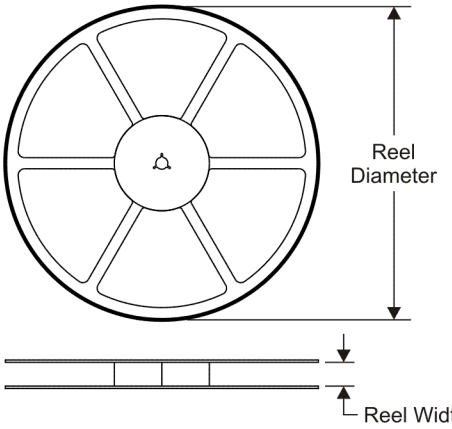
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

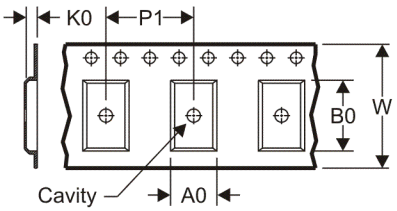
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

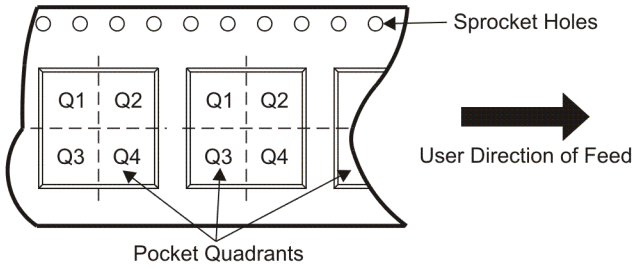


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

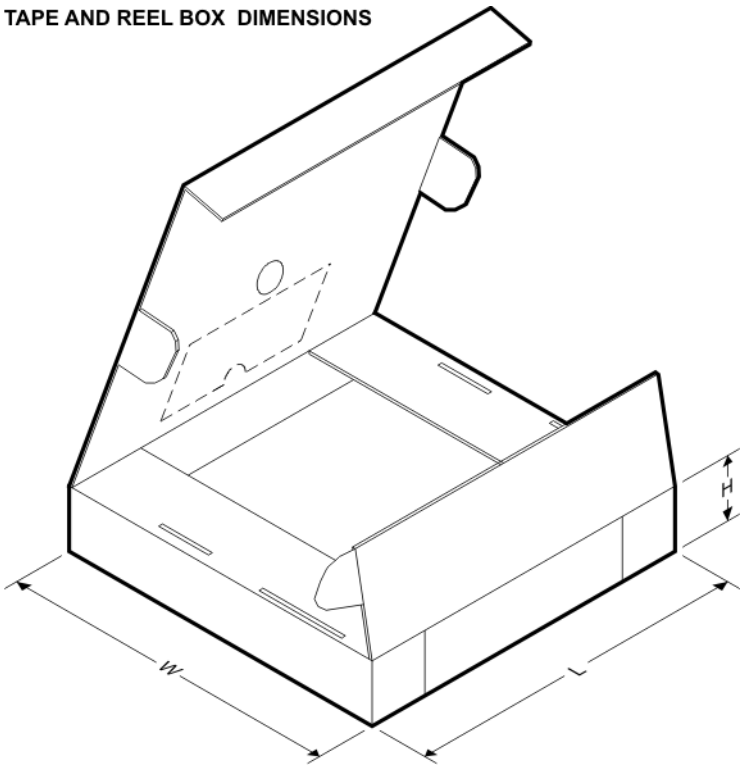
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5696PNR	LQFP	PN	80	1000	330.0	24.4	14.6	14.6	1.9	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

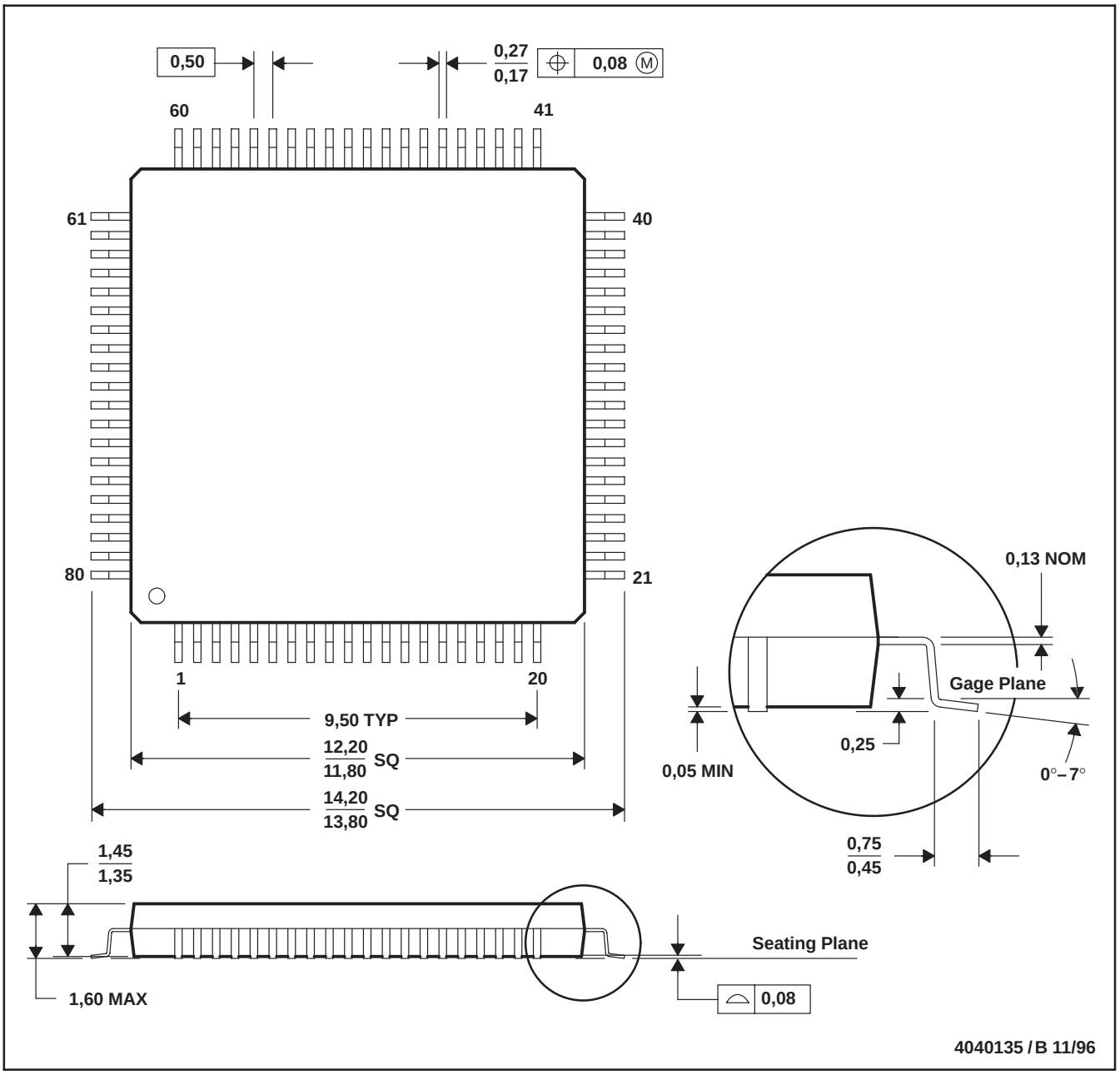


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5696PNR	LQFP	PN	80	1000	367.0	367.0	45.0

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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