- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
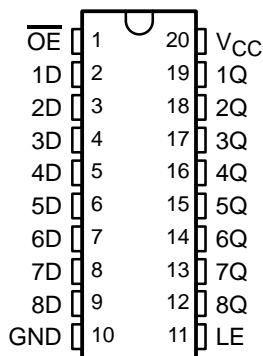
description/ordering information

The 'AHCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.
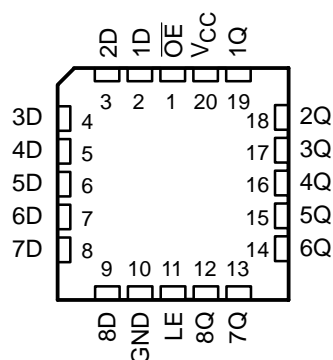
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AHCT573 . . . J OR W PACKAGE
SN74AHCT573 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

Pin			Pin
$\overline{OE}$	1	20	V_{CC}
1D	2	19	1Q
2D	3	18	2Q
3D	4	17	3Q
4D	5	16	4Q
5D	6	15	5Q
6D	7	14	6Q
7D	8	13	7Q
8D	9	12	8Q
GND	10	11	LE

SN54AHCT573 . . . FK PACKAGE
(TOP VIEW)

Top pins (3 2 1 20 19): 2D 1D $\overline{OE}$ V_{CC} 1Q

Pin			Pin
3D	4	18	2Q
4D	5	17	3Q
5D	6	16	4Q
6D	7	15	5Q
7D	8	14	6Q

Bottom pins (9 10 11 12 13): 8D GND LE 8Q 7Q

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74AHCT573N	SN74AHCT573N
	SOIC – DW	Tube	SN74AHCT573DW	AHCT573
		Tape and reel	SN74AHCT573DWR	
	SOP – NS	Tape and reel	SN74AHCT573NSR	AHCT573
	SSOP – DB	Tape and reel	SN74AHCT573DBR	HB573
	TSSOP – PW	Tube	SN74AHCT573PW	HB573
		Tape and reel	SN74AHCT573PWR	
	TVSOP – DGV	Tape and reel	SN74AHCT573DGVR	HB573
−55°C to 125°C	CDIP – J	Tube	SNJ54AHCT573J	SNJ54AHCT573J
	CFP – W	Tube	SNJ54AHCT573W	SNJ54AHCT573W
	LCCC – FK	Tube	SNJ54AHCT573FK	SNJ54AHCT573FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)

To Seven Other Channels
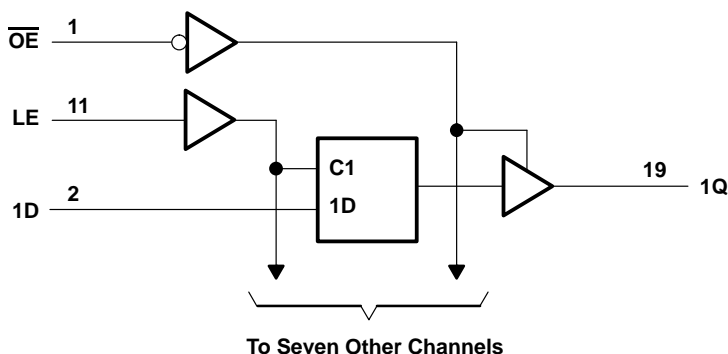
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 70°C/W
                                                        DGV package .... 92°C/W
                                                        DW package .... 58°C/W
                                                        N package .... 69°C/W
                                                        NS package .... 60°C/W
                                                        PW package .... 83°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

TEXAS
INSTRUMENTS

recommended operating conditions (see Note 3)

		SN54AHCT573 MIN	SN54AHCT573 MAX	SN74AHCT573 MIN	SN74AHCT573 MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$ MIN	$T_A = 25°C$ TYP	$T_A = 25°C$ MAX	SN54AHCT573 MIN	SN54AHCT573 MAX	SN74AHCT573 MIN	SN74AHCT573 MAX	UNIT
V_{OH}	$I_{OH} = -50\ \mu A$	4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -8\ mA$		3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8\ mA$				0.36		0.44		0.44	
I_I	$V_I = 5.5\ V$ or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}	$V_I = 5.5\ V$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
$\Delta I_{CC}^\dagger$	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0$ V.
† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25°C$ MIN	$T_A = 25°C$ MAX	SN54AHCT573 MIN	SN54AHCT573 MAX	SN74AHCT573 MIN	SN74AHCT573 MAX	UNIT
t_w	Pulse duration, LE high	5		5		5		ns
t_{su}	Setup time, data before LE↓	3.5		3.5		3.5		ns
t_h	Hold time, data after LE↓	1.5		1.5		1.5		ns

TEXAS INSTRUMENTS

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT573		SN74AHCT573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	C_L = 15 pF		4.2*	6*	1*	6.5*	1	6.5	ns
t_{PHL}					5.1*	7*	1*	9*	1	9	
t_{PLH}	LE	Q	C_L = 15 pF		4.7*	6.5*	1*	7.5*	1	7.5	ns
t_{PHL}					5.6*	7.5*	1*	9*	1	9	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		4.1*	6.5*	1*	7*	1	7	ns
t_{PZL}					5.5*	7.5*	1*	10*	1	10	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5.5*	8*	1*	11*	1	11	ns
t_{PLZ}					5.4*	8*	1*	9.5*	1	9.5	
t_{PLH}	D	Q	C_L = 50 pF		5.2	7	1	7.5	1	7.5	ns
t_{PHL}					6.1	8	1	10	1	10	
t_{PLH}	LE	Q	C_L = 50 pF		5.7	7.5	1	8.5	1	8.5	ns
t_{PHL}					6.6	8.5	1	10	1	10	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		5.1	7.5	1	8	1	8	ns
t_{PZL}					6.5	8.5	1	11	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9	1	12	1	12	ns
t_{PLZ}					6.4	9	1	10.5	1	10.5	
$t_{sk(o)}$			C_L = 50 pF		1.5**					1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
** On products compliant to MIL-PRF-38535, this parameter does not apply.

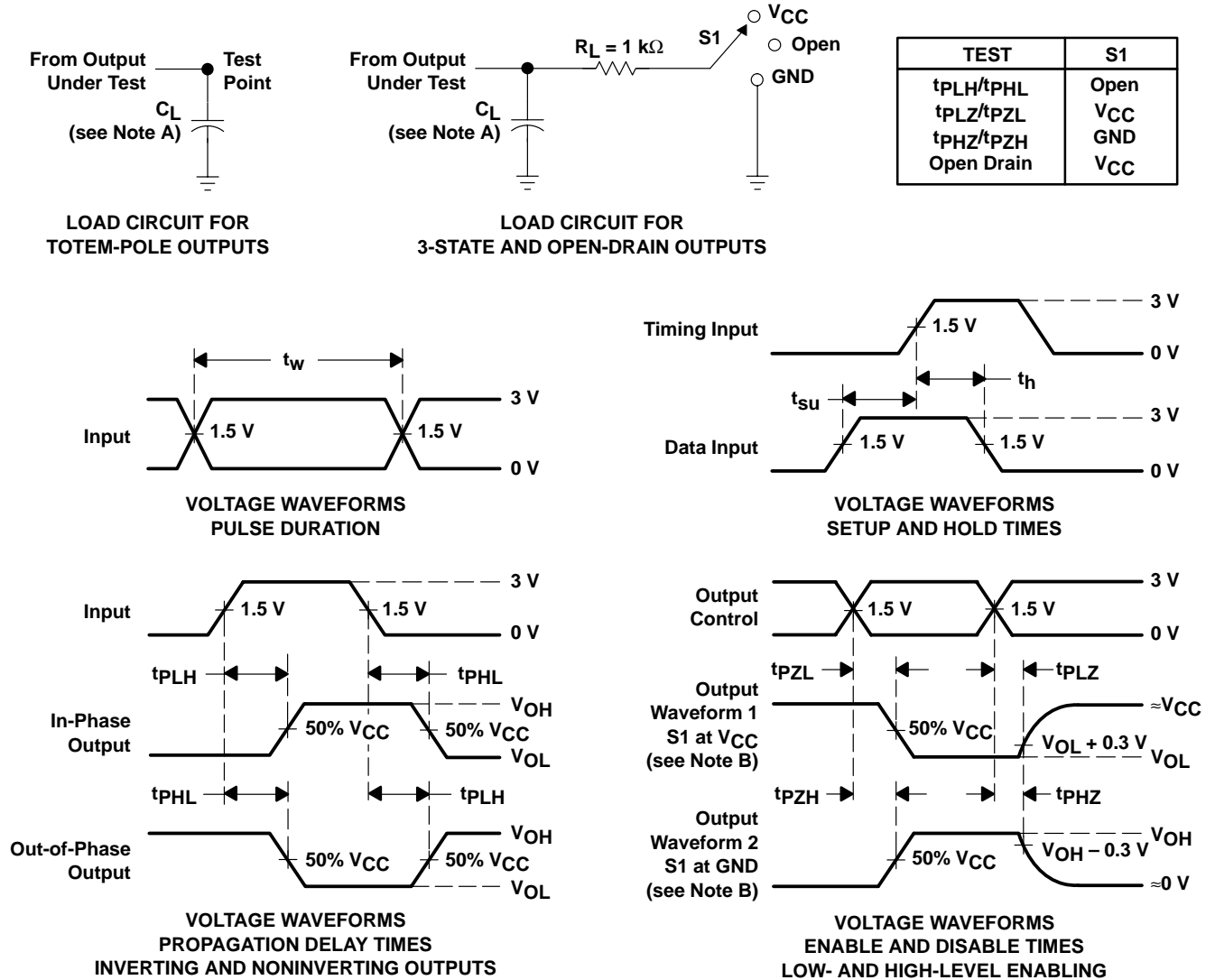**operating characteristics,** V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	16	pF

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PARAMETER MEASUREMENT INFORMATION

From Output Under Test — Test Point

C_L (see Note A)

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

From Output Under Test

$R_L = 1 \text{ k}\Omega$ S1

○ V_{CC}
○ Open
○ GND

C_L (see Note A)

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

Input — t_w — 1.5 V — 1.5 V — 3 V / 0 V

VOLTAGE WAVEFORMS PULSE DURATION

Timing Input — 1.5 V — 3 V / 0 V

t_{su} t_h

Data Input — 1.5 V — 1.5 V — 3 V / 0 V

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

Input — 1.5 V — 1.5 V — 3 V / 0 V

t_{PLH} t_{PHL}

In-Phase Output — 50% V_{CC} — 50% V_{CC} — V_{OH} / V_{OL}

t_{PHL} t_{PLH}

Out-of-Phase Output — 50% V_{CC} — 50% V_{CC} — V_{OH} / V_{OL}

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

Output Control — 1.5 V — 1.5 V — 3 V / 0 V

t_{PZL} t_{PLZ}

Output Waveform 1 S1 at V_{CC} (see Note B) — 50% V_{CC} — $V_{OL} + 0.3$ V — ≈V_{CC} / V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 S1 at GND (see Note B) — 50% V_{CC} — $V_{OH} - 0.3$ V — V_{OH} / ≈0 V

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.
   E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DIM \ PINS **	14	16	18	20
[A]	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

[A]

0°−15°

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package is hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R-GDFP-F20) **CERAMIC DUAL FLATPACK**

Base and Seating Plane

$\dfrac{0.300\ (7,62)}{0.245\ (6,22)}$

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.100\ (2,54)}{0.045\ (1,14)}$

$\dfrac{0.009\ (0,23)}{0.004\ (0,10)}$

0.320 (8,13) MAX

$\dfrac{0.022\ (0,56)}{0.015\ (0,38)}$

0.050 (1,27)

0.540 (13,72) MAX

0.005 (0,13) MIN
4 Places

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$
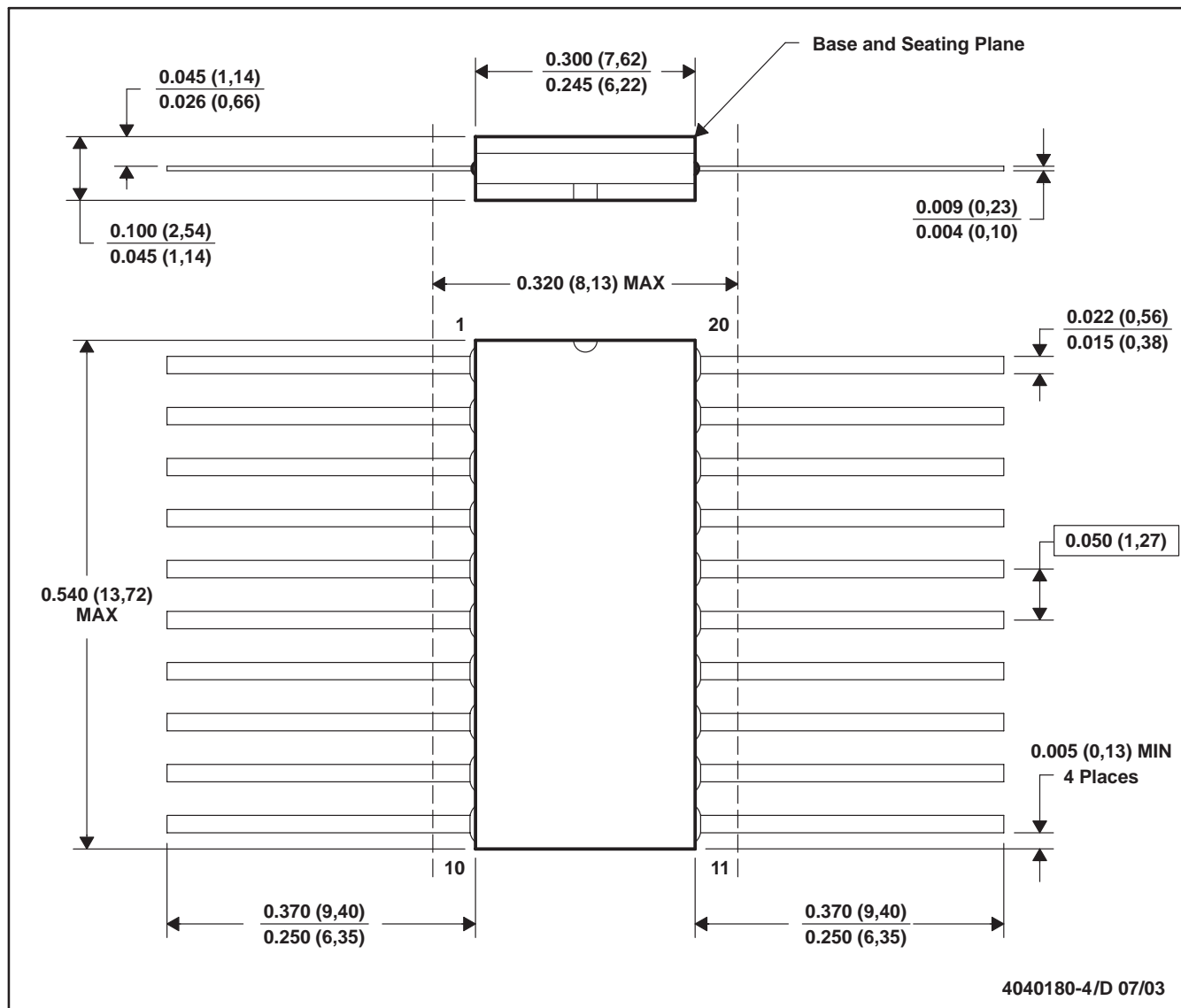
4040180-4/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil-Std 1835 GDFP2-F20

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FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. This package can be hermetically sealed with a metal lid.
   D. The terminals are gold plated.
   E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS

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N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
     △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
     △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

0,23
0,13   ⊕   0,07 Ⓜ

24   13

4,50   6,60
4,30   6,20

0,16 NOM

Gage Plane

0,25

1   12

0°–8°

0,75
0,50

A

1,20 MAX

0,15
0,05

Seating Plane

◁ 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
        D. Falls within JEDEC: 24/48 Pins – MO-153
                                 14/16/20/56 Pins – MO-194

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DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AC.

MECHANICAL DATA

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
    B.   This drawing is subject to change without notice.
    C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
           D. Falls within JEDEC MO-150

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

	PINS **	8	14	16	20	24	28
DIM							
A MAX		3,10	5,10	5,10	6,60	7,90	9,80
A MIN		2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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