8V, 16A Synchronous Step-Down Silent Switcher 2

FEATURES

- **Silent Switcher®2 Architecture**
  - **Ultralow EMI Emissions on Any PCB**
  - **Internal Bypass Capacitors Reduce Radiated EMI**
  - **Optional Spread Spectrum Modulation**
- **High Efficiency at High Frequency**
  - **Up to 94% Efficiency at 2MHz, 3.3V_{IN} to 1.2V_{OUT}**
  - **Up to 93% Efficiency at 2MHz, 5V_{IN} to 1.2V_{OUT}**
- **PV_{IN} Range: 1.5V to 8V, SV_{IN} Range: 2.7V to 8V**
- **V_{OUT} Range: 0.6V to V_{IN}**
- Reference Accuracy: ±0.8% Over Temperature
- PolyPhase® Operation: Up to 12 Phases
- Fast Transient Response with External Compensation
- Forced Continuous Mode Operation
- Low Quiescent Current Burst Mode® Operation
  - 180μA I_Q Regulating 5V_{IN} to 1.2V_{OUT}
  - Output Ripple < 10mV_{P-P}
- Fast Minimum Switch On-Time: 20ns
- Adjustable and Synchronizable: 300kHz to 3.5MHz
- Output Soft-Start and Power Good
- Small 24-Lead 4mm × 4mm LQFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive and Industrial Supplies
- General Purpose Step-Down Conversion

DESCRIPTION

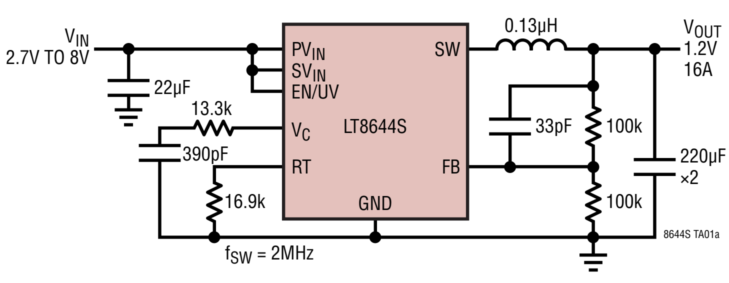
The LT®8644S synchronous step-down regulator features second generation Silent Switcher architecture designed to minimize EMI emissions while delivering high efficiency at high switching frequencies. This includes the integration of bypass capacitors to optimize all the fast current loops inside and make it easy to achieve advertised EMI performance by eliminating layout sensitivity.

The fast, clean, low-overshoot switching edges enable high efficiency operation even at high switching frequencies, leading to a small overall solution size. Peak current mode control with a 20ns minimum on-time allows high step down ratios even at high switching frequencies. External compensation via the V_C pin allows for fast transient response. PolyPhase operation allows multiple LT8644S regulators to run with interleaving phase shift to provide more output current.

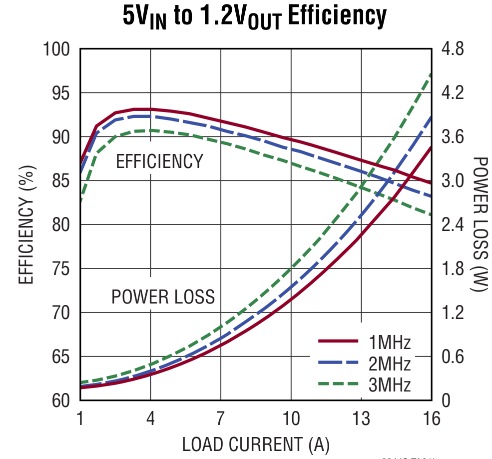
Burst Mode operation enables low standby current consumption, forced continuous mode can control frequency harmonics across the entire output load range, or spread spectrum operation can further reduce EMI emissions. Soft-start and tracking functionality is accessed via the SS pin, and an accurate input voltage UVLO threshold can be set using the EN/UV pin.

TYPICAL APPLICATION

1.2V 16A Step-Down Converter



5V_{IN} to 1.2V_{OUT} Efficiency



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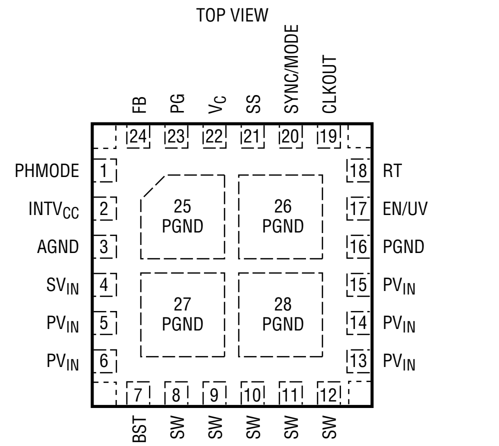
ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, SV_{IN}, EN/UV 10V
PG 8V
FB, SS, PHMODE 4V
SYNC/MODE 6V
Operating Junction Temperature Range (Note 2)
LT8644SI .... –40°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Maximum Reflow (Package Body) Temperature .... 260°C

PIN CONFIGURATION



LQFN PACKAGE
24-LEAD (4mm × 4mm × 0.95mm)
JEDEC BOARD: θ_{JA} = 38°C/W, $\theta_{JC(TOP)}$ = 44°C/W, $\theta_{JC(PAD)}$ = 7°C/W (NOTE 3)
DEMO BOARD: θ_{JA} = 24°C/W, Ψ_{JT} = 0.8°C/W
EXPOSED PAD (PINS 25–28) ARE PGND, SHOULD BE SOLDERED TO PCB

ORDER INFORMATION

TAPE AND REEL (MINI)	TAPE AND REEL	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE**	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
			DEVICE	FINISH CODE			
LT8644SIV#TRMPBF	LT8644SIV#TRPBF	Au (RoHS)	8644S	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
AUTOMOTIVE PRODUCTS* **							
LT8644SIV#WTRMPBF	LT8644SIV#WTRPBF	Au (RoHS)	8644S	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Device temperature grade is identified by a label on the shipping container.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

Parts ending with PBF are RoHS and WEEE compliant. **The LT8644S package has the same dimensions as a standard 4mm × 4mm QFN package.

***Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SV_{IN} Operating Voltage		●	2.7		8	V
PV_{IN} Operating Voltage			1.5		8	V
SV_{IN} Quiescent Current in Shutdown	$V_{EN/UV}$ = 0V, V_{IN} = 5V	●		6	12	µA
SV_{IN} Quiescent Current in Sleep	$V_{EN/UV}$ = 2V, V_{FB} > 0.6V, V_{SYNC} = 0V, V_{IN} = 5V	 ●		125 125	195 245	µA µA
Feedback Reference Voltage	V_{IN} = 5V, V_C = 1.25V V_{IN} = 5V, V_C = 1.25V	 ●	0.598 0.595	0.6 0.6	0.602 0.603	V V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Voltage Line Regulation	V_{IN} = 3.0V to 8V	●		0.025	0.12	%/V
Feedback Pin Input Current	V_{FB} = 0.6V		–20		20	nA
Error Amplifier Transconductance	V_C = 1.25V		1.1	1.45	1.8	mS
Error Amp Gain				650		
V_C Source Current	V_{FB} = 0.4V, V_C = 1.25V			320		µA
V_C Sink Current	V_{FB} = 0.8V, V_C = 1.25V			320		µA
V_C Pin to Switch Current Gain				18		A/V
V_C Clamp Voltage				2.3		V
SV_{IN} Pin Current Consumption	SV_{IN} = 5V, f_{SW} = 2MHz			20		mA
Minimum On-Time	I_{LOAD} = 4A, SYNC = 2V	●		20	35	ns
Minimum Off-Time				75	100	ns
Oscillator Frequency	R_T = 147k R_T = 38.3k R_T = 16.9k	● ● ●	260 0.95 1.95	300 1 2	340 1.05 2.05	kHz MHz MHz
Top Power NMOS On-Resistance				12		mΩ
Bottom Power NMOS On-Resistance	V_{INTVCC} = 3.6V			4.3		mΩ
Top Power NMOS Current Limit		●	25	30	33	A
Bottom Power NMOS Current Limit	V_{INTVCC} = 3.6V		15.5	21	26.5	A
SW Leakage Current	V_{IN} = 8V, V_{SW} = 0V, 8V		–10		10	µA
EN/UV Pin Threshold	EN/UV Rising	●	0.93	0.98	1.03	V
EN/UV Pin Hysteresis				40		mV
EN/UV Pin Current	$V_{EN/UV}$ = 2V		–20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Rising	●	6.25	7.75	9.25	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Falling	●	–9.25	–7.75	–6.25	%
PG Hysteresis				0.4		%
PG Leakage	V_{PG} = 3.3V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		600	2000	Ω
SYNC/MODE Threshold	SYNC/MODE DC and Clock Low Level Voltage SYNC/MODE Clock High Level Voltage SYNC/MODE DC High Level Voltage	● ● ●	0.5 V_{INTVCC} – 1.1		 1.5 V_{INTVCC} – 0.5	V V V
Spread Spectrum Modulation Frequency Range	R_T = 38.3k, V_{SYNC} = 3.3V			25		%
Spread Spectrum Modulation Frequency	V_{SYNC} = 3.3V			3		kHz
SS Source Current		●	1.3	2.0	2.7	µA
SS Pull-Down Resistance	Fault Condition, SS = 0.1V			200		Ω
PHMODE Thresholds	Between 180° and 120° Between 120° and 90°		0.7 V_{INTVCC} – 1.3		1.4 V_{INTVCC} – 0.6	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8644SI is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (PD, in Watts) according to the formula:

$$T_J = T_A + (PD \bullet \theta_{JA})$$

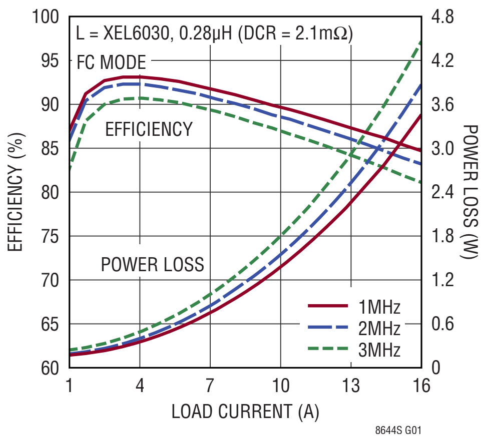
where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: θ values determined per JEDEC 51-7, 51-12. See the Applications Information section for information on improving the thermal resistance and for actual temperature measurements of a demo board in typical operating conditions.

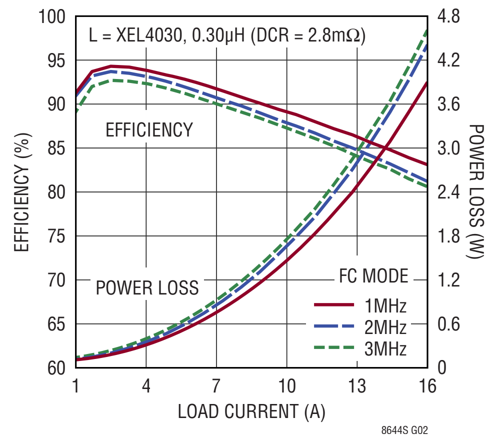
Note 4: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

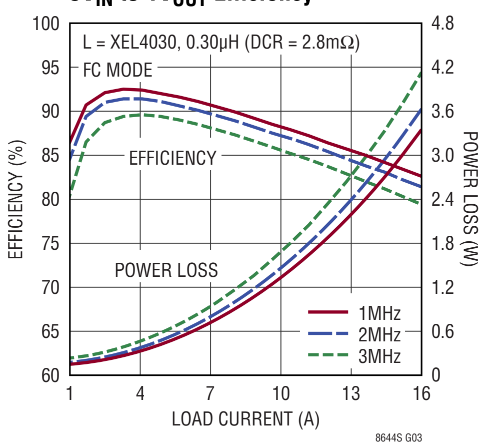
$5V_{IN}$ to $1.2V_{OUT}$ Efficiency



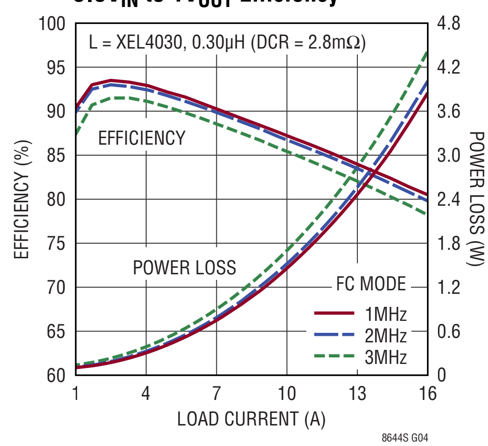
$3.3V_{IN}$ to $1.2V_{OUT}$ Efficiency



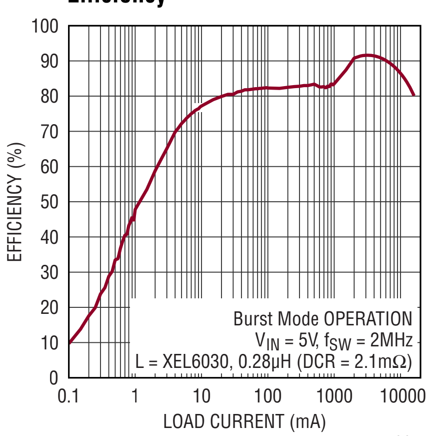
$5V_{IN}$ to $1V_{OUT}$ Efficiency



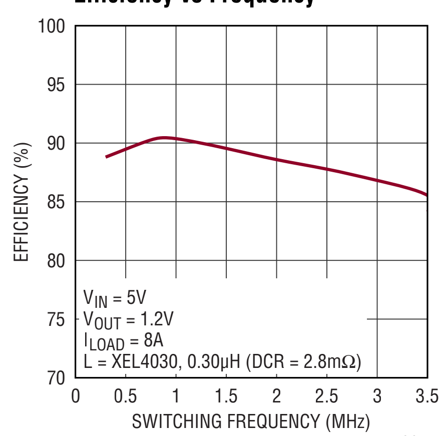
$3.3V_{IN}$ to $1V_{OUT}$ Efficiency



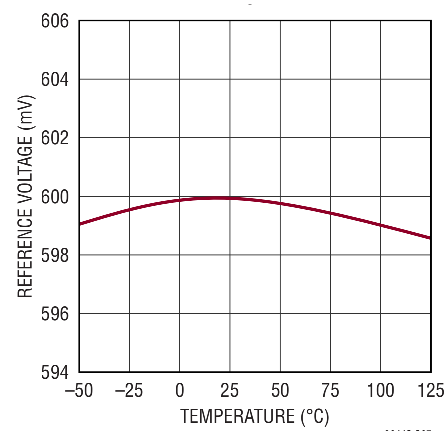
$5V_{IN}$ to $1.2V_{OUT}$ Light Load Efficiency



Efficiency vs Frequency



Reference Voltage



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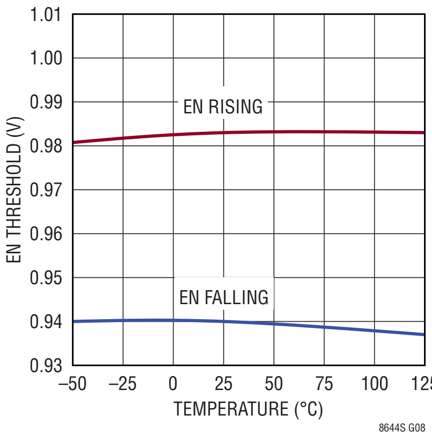
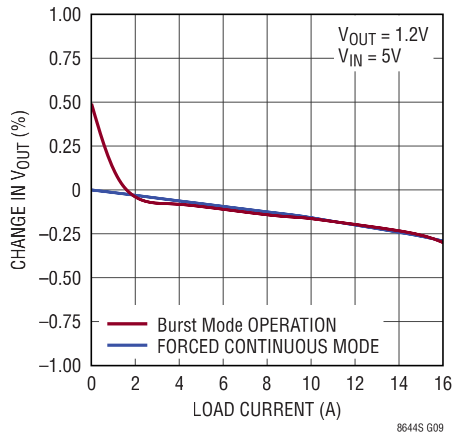
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

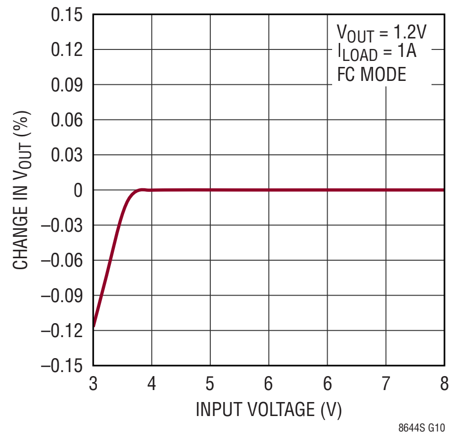
EN Pin Thresholds



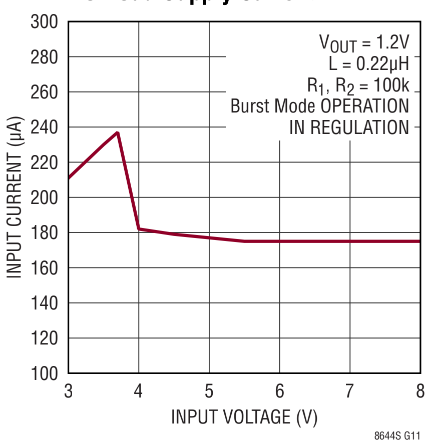
Load Regulation



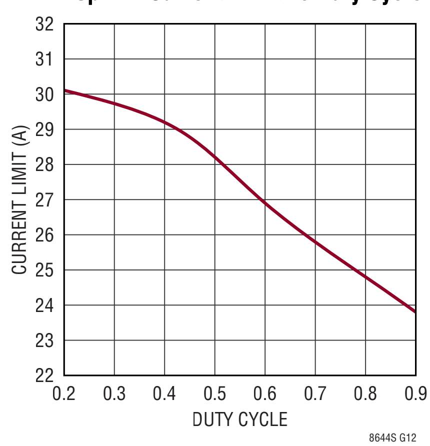
Line Regulation



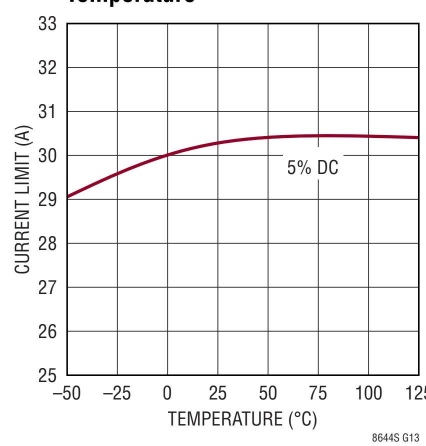
No-Load Supply Current



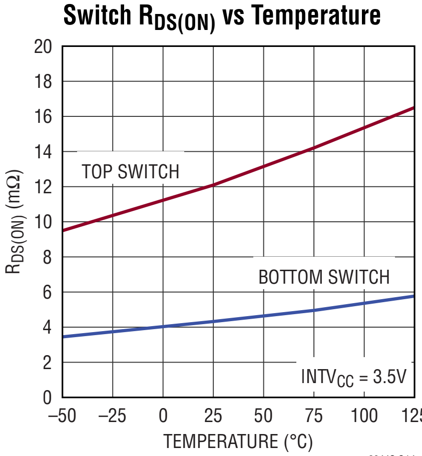
Top FET Current Limit vs Duty Cycle



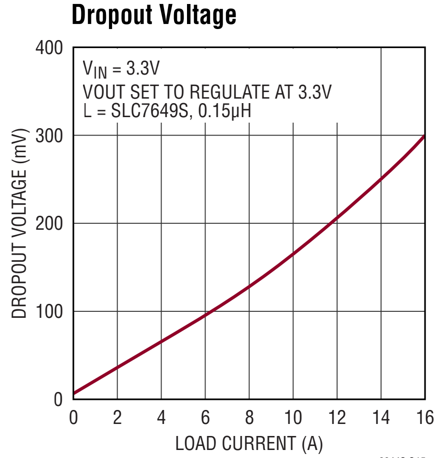
Top FET Current Limit vs Temperature



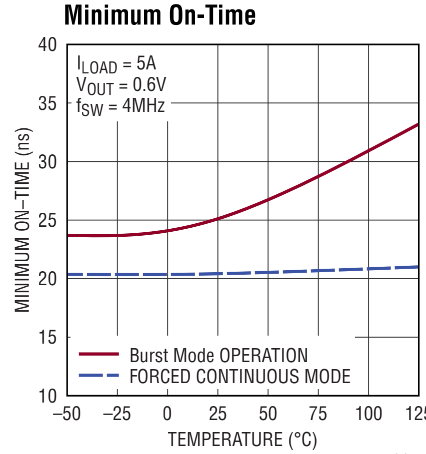
Switch $R_{DS(ON)}$ vs Temperature



Dropout Voltage

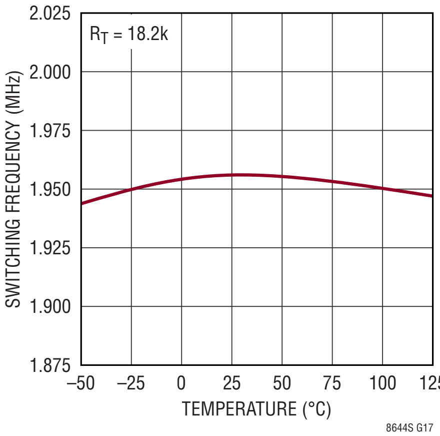


Minimum On-Time

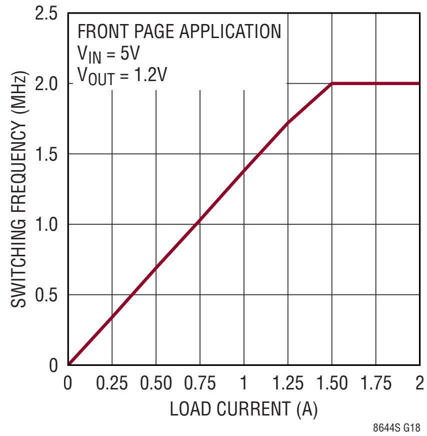


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

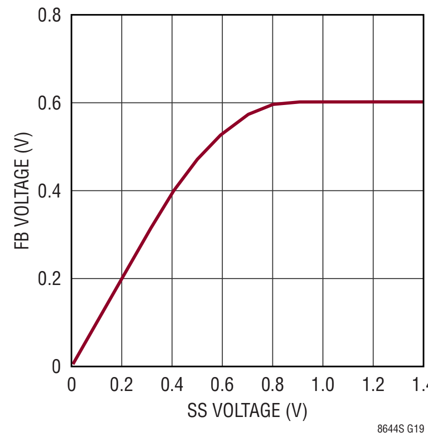
Switching Frequency



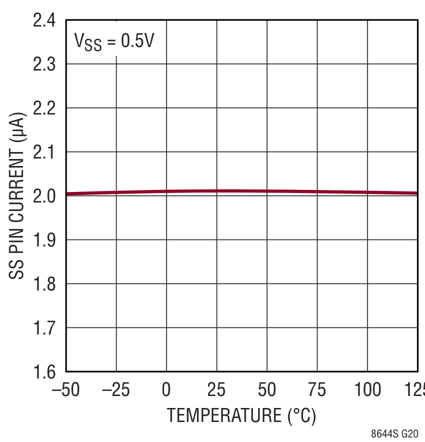
Burst Frequency



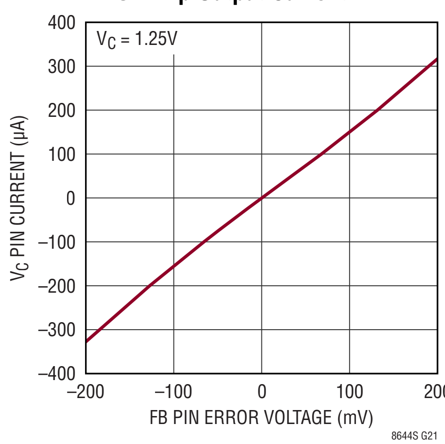
Soft-Start Tracking



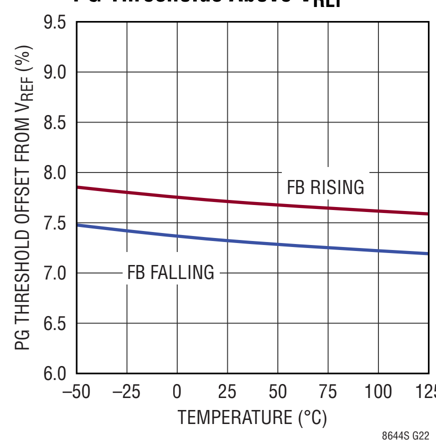
Soft-Start Current



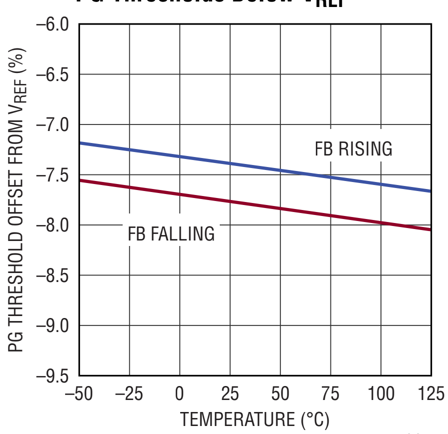
Error Amp Output Current



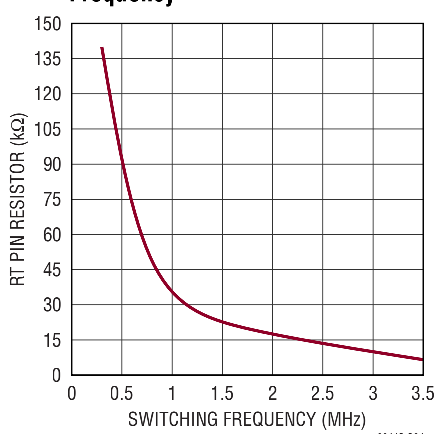
PG Thresholds Above V_{REF}



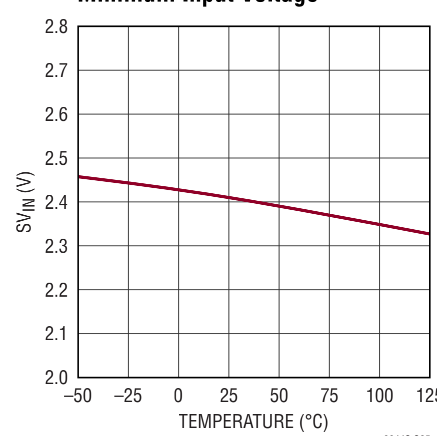
PG Thresholds Below V_{REF}



RT Programmed Switching Frequency



Minimum Input Voltage



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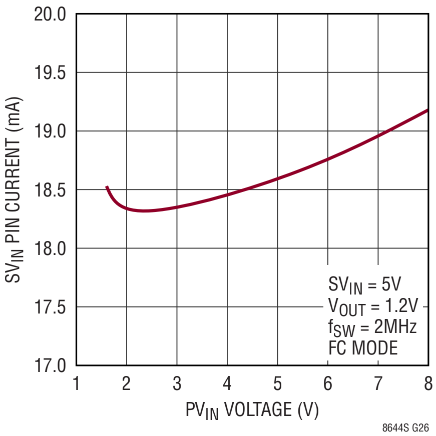
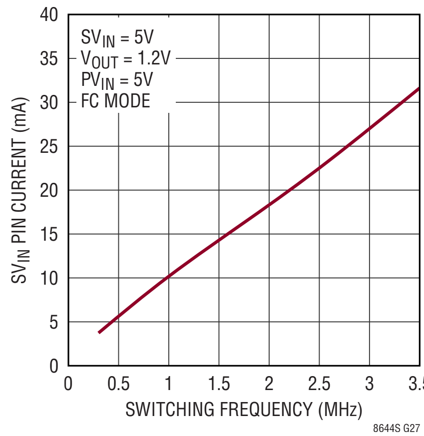
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

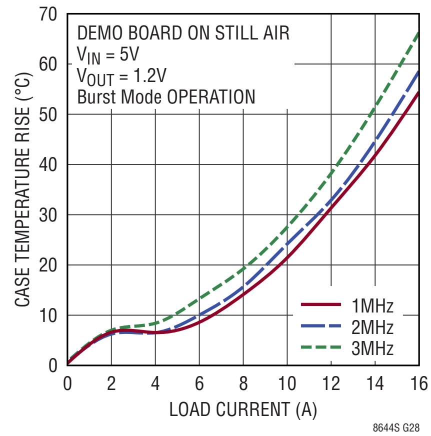
SV_{IN} Pin Current vs PV_{IN}



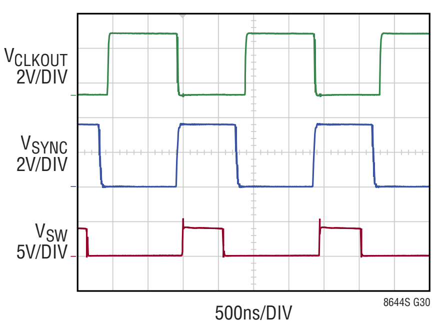
SV_{IN} Pin Current vs Frequency



Case Temperature Rise

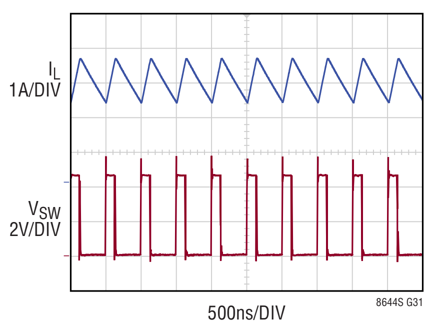


CLKOUT Waveforms



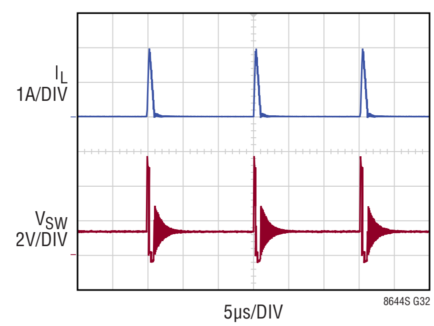
f_{SW} = 500kHz
SYNCHRONIZATION MODE

Switching Waveforms, Full Frequency Continuous Operation



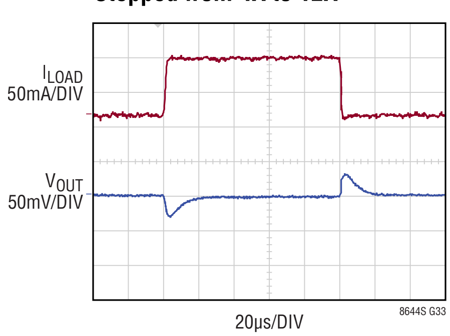
FRONT PAGE APPLICATION
$5V_{IN}$ TO $1.2V_{OUT}$ AT 3A
FC MODE

Switching Waveforms, Burst Mode Operation



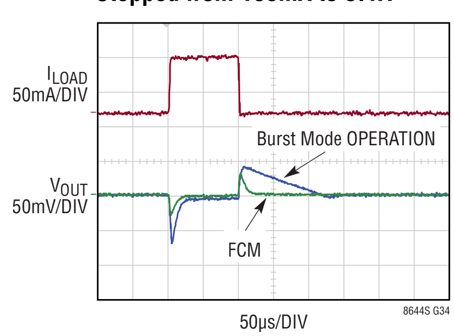
FRONT PAGE APPLICATION
$5V_{IN}$ TO $1.2V_{OUT}$ AT 100mA
Burst Mode OPERATION

Transient Response; Load Current Stepped from 4A to 12A



FRONT PAGE APPLICATION
4A TO 12A TRANSIENT
V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 2MHz
C_C = 390pF, R_C = 13.3k
C_{OUT} = 2 x 220µF, C_{LEAD} = 33pF

Transient Response; Load Current Stepped from 100mA to 8.1A



FRONT PAGE APPLICATION
100mA TO 8.1A TRANSIENT
V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 2MHz
C_C = 390pF, R_C = 13.3k
C_{OUT} = 2 x 220µF, C_{LEAD} = 33pF

PIN FUNCTIONS

PHMODE (Pin 1): Pin determines the phase relationship between the LT8644S's internal clock and CLKOUT. Tie it to ground for 2-phase operation, float the pin for 3-phase operation or tie it to $INTV_{CC}$ for 4-phase operation. See Block Diagram for internal pull-up and pull-down resistance.

$INTV_{CC}$ (Pin 2): Internal 3.6V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current will be supplied from SV_{IN}. Voltage on $INTV_{CC}$ will vary between 2.6V and 3.6V when SV_{IN} is between 2.7V and 3.7V. This pin should be floated.

AGND (Pin 3): The AGND pin is the output voltage remote ground sense. Connect the AGND pin directly to the negative terminal of the output capacitor at the load and to the feedback divider resistor.

SV_{IN} (Pin 4): Signal V_{IN}. Pin supplies current to the internal circuitry and regulator. If tied to a different supply than PV_{IN}, place a 1µF local bypass capacitor on this pin.

PV_{IN} (Pins 5, 6, 13, 14, 15): Power V_{IN}. The PV_{IN} pins supply current to the internal topside power switch. These pins must be tied together and be locally bypassed with a capacitor of 22µF or more. Be sure to place the positive terminal of the input capacitor as close as possible to the PV_{IN} pins, and the negative capacitor terminal as close as possible to the PGND pins.

BST (Pin 7): This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. This pin should be floated.

SW (Pins 8-12): The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor. This node should be kept small on the PCB for good performance and low EMI.

PGND (Pins 16, Exposed Pad Pins 25-28): The PGND pins are the return path to the internal bottom side power switch. Place the negative terminal of the input capacitor as close to the GND pins as possible. The exposed pads should be soldered to the PCB for good thermal performance. If necessary due to manufacturing limitations Pins 25 to 28 may be left disconnected, however thermal performance will be degraded.

EN/UV (Pin 17): The LT8644S is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 0.98V going up and 0.94V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8644S will shut down.

RT (Pin 18): A resistor is tied between RT and AGND to set the switching frequency.

CLKOUT (Pin 19): Output Clock Signal for PolyPhase Operation. In forced continuous mode, spread spectrum and synchronization modes, the CLKOUT pin provides a 50% duty cycle square wave of the switching frequency. The phase of CLKOUT with respect to the LT8644S's internal clock is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to AGND. In Burst Mode operation, the CLKOUT pin will be low. Float this pin if the CLKOUT function is not used.

SYNC/MODE (Pin 20): For the LT8644S, this pin programs four different operating modes: (1) Burst Mode operation. Tie this pin to ground for Burst Mode operation at low output loads—this will result in low quiescent current. (2) Forced Continuous mode (FCM). This mode offers fast transient response and full frequency operation over a wide load range. Float this pin for FCM. When floating, pin leakage currents should be <1µA. See Block Diagram for internal pull-up and pull-down resistance. (3) Spread spectrum mode. Tie this pin to $INTV_{CC}$ for forced continuous mode with spread-spectrum modulation. 4) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in forced continuous mode.

SS (Pin 21): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A SS voltage below 1V forces the LT8644S to regulate the FB pin to a function of the SS pin voltage. See plot in the Typical Performance Characteristics section. When SS is above 1V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and

PIN FUNCTIONS

fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the soft-start feature is not being used.

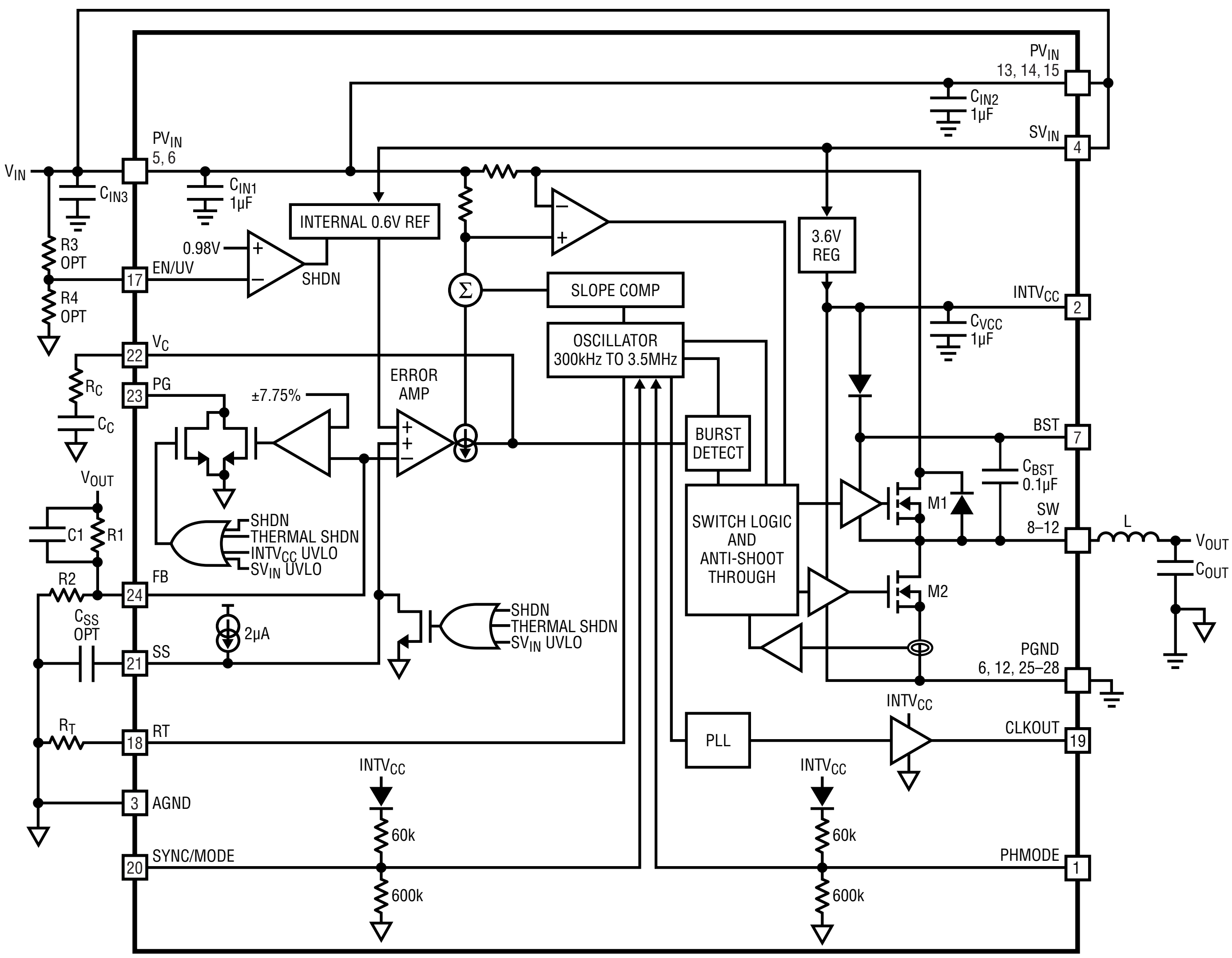
V_C (Pin 22): The V_C pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an RC network from this pin to AGND to compensate the control loop.

PG (Pin 23): The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±7.75% of the final regulation voltage, and there are no fault conditions. PG is also pulled low when EN/UV is below 0.98V, $INTV_{CC}$ has fallen too low, SV_{IN} is too low, or thermal shutdown. PG is valid when SV_{IN} is above 2.7V.

FB (Pin 24): The LT8644S regulates the FB pin to 0.6V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is 4.7pF to 47pF.

Corner Pins: These pins are for mechanical support only and can be tied anywhere on the PCB, typically ground.

BLOCK DIAGRAM



OPERATION

The LT8644S is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the V_C pin. The error amplifier servos the V_C node by comparing the voltage on the V_{FB} pin with an internal 0.6V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 21A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The "S" in LT8644S refers to the second generation silent switcher technology. This technology allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI performance. This includes the integration of ceramic capacitors into the package for PV_{IN}, BST, and $INTV_{CC}$ (see Block Diagram). These caps keep all the fast AC current loops small, which improves EMI performance.

If the EN/UV pin is low, the LT8644S is shut down and draws 6μA from the input. When the EN/UV pin is above 0.98V, the switching regulator will become active.

To optimize efficiency at light loads, the LT8644S operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 125μA. In a typical application, 180μA will be consumed from the input supply when regulating with no load. The SYNC/MODE pin is tied low to use Burst Mode operation and can be floated to use forced continuous mode (FCM). If a clock is applied to the SYNC/MODE pin, the part will synchronize to an external clock frequency and operate in FCM.

The LT8644S can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is allowed. The LT8644S can sink current from the output and return this charge to the input in this mode, improving load step transient response.

To improve EMI, the LT8644S can operate in spread spectrum mode. This feature varies the clock with a triangular frequency modulation of +25%. For example, if the LT8644S's frequency is programmed to switch at 2MHz, spread spectrum mode will modulate the oscillator between 2MHz and 2.5MHz. The SYNC/MODE pin should be tied to $INTV_{CC}$ to enable spread spectrum modulation with forced continuous mode.

The V_C pin allows the loop compensation of the switching regulator to be optimized based on the programmed switching frequency, allowing for a fast transient response. The V_C and CLKOUT pins enable multiple LT8644S regulators to run with interleaving phase shift, reducing the amount of required input and output capacitors. The PHMODE pin selects the phasing of CLKOUT for different multiphase applications.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more than ±7.75% (typical) from the set point, or if a fault condition is present.

In Burst Mode operation, the oscillator reduces the LT8644S's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value which occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC/MODE pin, the SYNC/MODE pin is floated, or held DC high, the frequency foldback is disabled and the switching frequency will slow down only during overcurrent conditions.

APPLICATIONS INFORMATION

Low EMI PCB Layout

The LT8644S is specifically designed to minimize EMI emissions and also to maximize efficiency when switching at high frequencies. For optimal performance the LT8644S should use multiple V_{IN} bypass capacitors.

Two small <1µF capacitors can be placed as close as possible to the LT8644S, one capacitor on each side of the device (C_{OPT1}, C_{OPT2}). A third capacitor with a larger value, 22µF or higher, should be placed near C_{OPT1} or C_{OPT2}.

See Figure 1 for a recommended PCB layout.

For more detail and PCB design files refer to the Demo Board guide for the LT8644S.

Note that large, switched currents flow in the LT8644S PV_{IN} and PGND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the PV_{IN} and PGND pins. Capacitors with small case size such as 0402 or 0603 are optimal due to lowest parasitic inductance.

The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes.

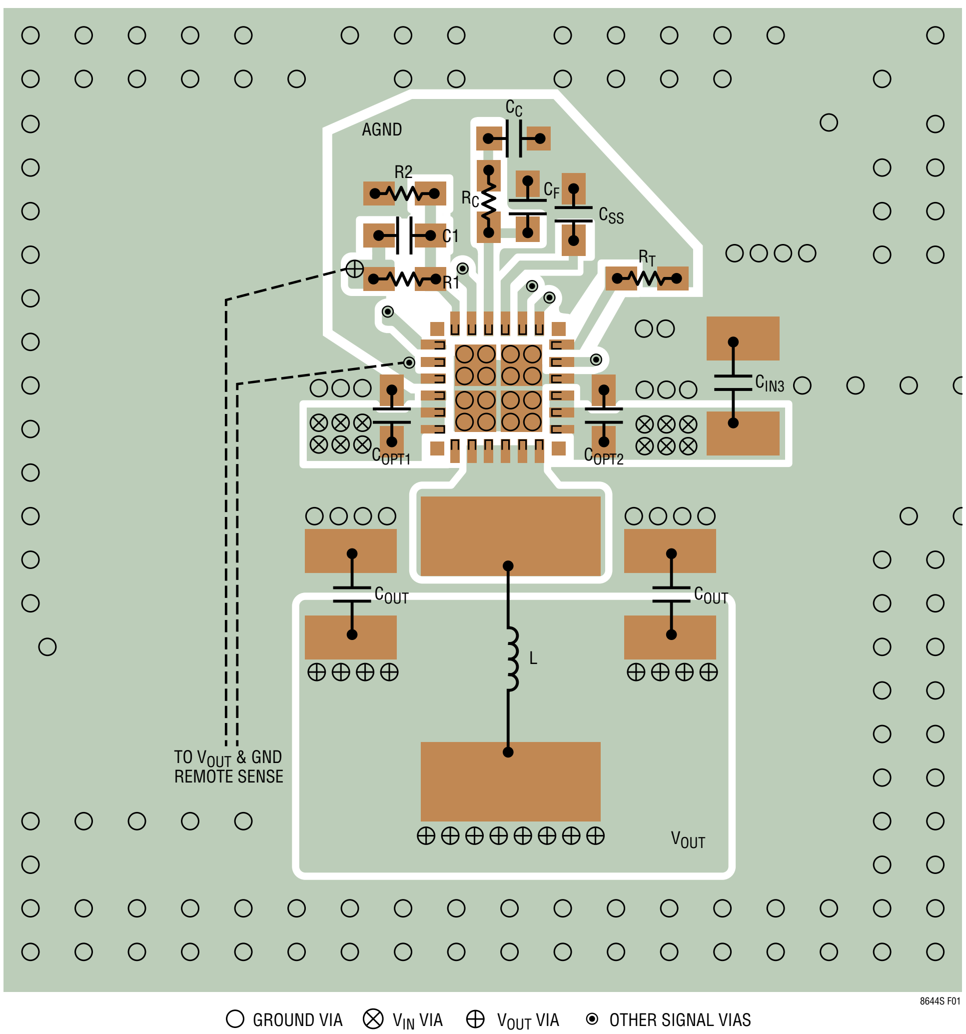


Figure 1. Recommended PCB Layout for the LT8644S

Rev. A

APPLICATIONS INFORMATION

The exposed pads on the bottom of the package should be soldered to the PCB to reduce thermal resistance to ambient. To keep thermal resistance low, extend the ground plane from PGND as much as possible, and add thermal vias to additional ground planes within the circuit board and on the bottom side.

Burst Mode Operation

To enhance efficiency at light loads, the LT8644S operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation the LT8644S delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8644S consumes 125µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 2) and the percentage of time the LT8644S is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 180µA for a typical application when there is no output load. Note that the current in the feedback resistor divider appears to the output as load current.

While in Burst Mode operation the current limit of the top switch is approximately 2.5A (as shown in Figure 3), resulting in low output voltage ripple. Increasing the output capacitance will decrease output ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 2.

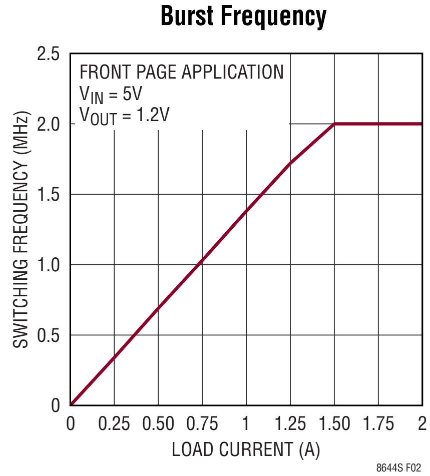


Figure 2. SW Frequency vs Load Information in Burst Mode Operation

The output load at which the LT8644S reaches the programmed frequency varies based on input voltage, output voltage and inductor choice. To select low ripple Burst Mode operation, tie the SYNC/MODE pin below 0.4V (this can be ground or a logic low output).

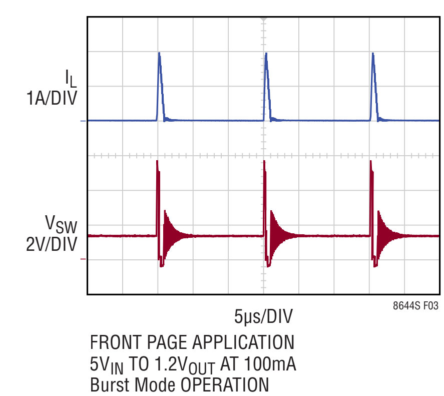


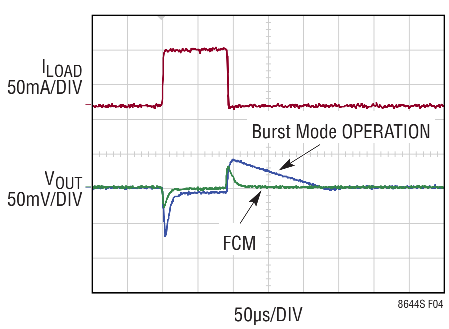
Figure 3. Burst Mode Operation

APPLICATIONS INFORMATION

Forced Continuous Mode

The LT8644S can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is allowed at light loads or under large transient conditions. The LT8644S can sink current from the output and return this charge to the input in this mode, improving load step transient response (see Figure 4). At light loads, FCM operation is less efficient than Burst Mode operation, but may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. FCM must be used if the output is required to sink current. To enable FCM, float the SYNC/MODE pin. Leakage current on this pin should be <1μA. See Block Diagram for internal pull-up and pull-down resistance.

FCM is disabled if the PV_{IN} pin is held above 8.5V or if the FB pin is held greater than 8% above the feedback reference voltage. FCM is also disabled during soft-start until the soft-start capacitor is fully charged (~2V). When FCM is disabled in these ways, negative inductor current is not allowed and the LT8644S operates in pulse-skipping mode.



FRONT PAGE APPLICATION
100mA TO 8.1A TRANSIENT
V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 2MHz
C_C = 390pF, R_C = 13.3k
C_{OUT} = 2 x 220μF, C_{LEAD} = 33pF

Figure 4. Load Step Transient Response with and without Forced Continuous Mode

Spread Spectrum Mode

The LT8644S features spread spectrum operation to further reduce EMI emissions. To enable spread spectrum operation, the SYNC/MODE pin should be tied to $INTV_{CC}$. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by RT to approximately 25% higher than that value. The modulation frequency is approximately 3kHz. For example, when the LT8644S is programmed to 2MHz, the frequency will vary from 2MHz to 2.5MHz at a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part will run in forced continuous mode.

Synchronization

To synchronize the LT8644S oscillator to an external frequency, connect a square wave to the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

The LT8644S will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will run forced continuous mode to maintain regulation. The LT8644S may be synchronized over a 300kHz to 3.5MHz range. The RT resistor should be chosen to set the LT8644S switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the RT should be selected for 500kHz. The slope compensation is set by the RT value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by RT, then the slope compensation will be sufficient for all synchronization frequencies.

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FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 1.

$$R1 = R2\left(\frac{V_{OUT}}{0.60V} - 1\right) \quad (1)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

When using large FB resistors, a 4.7pF to 47pF phase-lead capacitor should be connected from V_{OUT} to FB.

Output Voltage Sensing

The AGND pin is the ground reference for the internal analog circuitry, including the feedback reference voltage. In high current operation, a ground offset may be present between the LT8644S local ground and ground at the load. To achieve good load regulation, connect the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. A drop in the high current power ground return path will be compensated. All of the signal components, such as the FB resistor divider and R_T resistor, should be referenced to the AGND node. The AGND node carries very little current and, therefore, can be a minimal size trace. The LT8644S allows for remote output ground deviations as much as 100mV with respect to local ground.

Setting the Switching Frequency

The LT8644S uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 3.5MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 1.

The R_T resistor required for a desired switching frequency can be calculated using Equation 2.

$$R_T = \frac{44.8}{f_{SW}} - 5.9 \quad (2)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	143
0.4	105
0.5	82.5
0.6	66.5
0.7	56.2
0.8	48.7
1.0	38.3
1.2	31.6
1.4	26.1
1.6	22.1
1.8	19.1
2.0	16.9
2.2	15.4
3.0	10.5

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated using Equation 3.

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (3)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.2V, ~0.07V, respectively at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see the Electrical Characteristics). Equation 3 shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

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For transient operation, V_{IN} may go as high as the absolute maximum rating regardless of the R_T value, however the LT8644S will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8644S is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the LT8644S skips switch cycles, resulting in a lower switching frequency than programmed by RT. The top switch has a maximum on-time of approximately 30µs, after which a switch cycle will occur to recharge the boost capacitor.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios use Equation 4 to set switching frequency.

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (4)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.2V, ~0.07V, respectively at maximum load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8644S is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8644S safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is given by Equation 5.

$$L = \left(\frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}}\right) \bullet 0.3 \quad (5)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.07V) and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current (Equation 6).

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (6)$$

where ΔI_L is the inductor ripple current as calculated in Equation 8 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 3A output should use an inductor with an RMS rating of greater than 3A and an I_{SAT} of greater than 4A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 5mΩ, and the core material should be intended for high frequency applications.

The LT8644S limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 30A at low duty cycles and decreases linearly to 24A at DC = 0.9. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current (Equation 7).

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (7)$$

The peak-to-peak ripple current in the inductor can be calculated by Equation 8.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (8)$$

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where f_{SW} is the switching frequency of the LT8644S, and L is the value of the inductor. Therefore, the maximum output current that the LT8644S will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8644S may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see ADI Application Note 44.

For duty cycles greater than 50% (V_{OUT}/V_{IN} > 0.5), a minimum inductance is required to avoid sub-harmonic oscillation (see Equation 9). See Application Note 19 for more details.

$$L_{MIN} = \frac{PV_{IN}\left(2 \bullet DC - 1\right)}{6 \bullet f_{SW}} \quad (9)$$

where DC is the duty cycle ratio (V_{OUT}/V_{IN}) and f_{SW} is the switching frequency.

Input Capacitors

The V_{IN} of the LT8644S should be bypassed with at least three ceramic capacitors for best performance. Two small ceramic capacitors of <1µF can be placed close to the part; one on each side of the device (C_{OPT1}, C_{OPT2}). These capacitors should be 0402 or 0603 in size. For automotive applications requiring 2 series input capacitors, two small 0402 or 0603 may be placed at each side of the LT8644S near the PV_{IN} and PGND pins.

A third, larger ceramic capacitor of 22µF or larger should be placed close to C_{OPT1} or C_{OPT2}. See layout section for more detail. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations.

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8644S circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8644S's voltage rating. This situation is easily avoided (see ADI Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8644S to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8644S's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Application section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Application in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage

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bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8644S due to their piezoelectric nature. When in Burst Mode operation, the LT8644S's switching frequency depends on the load current, and at very light loads the LT8644S can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8644S operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8644S. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT8644S circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8644S's rating. This situation is easily avoided (see ADI Application Note 88).

Enable Pin

The LT8644S is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 0.98V, with 40mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN programs the LT8644S to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy Equation 10.

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1\right) \bullet 0.98V \qquad (10)$$

where the LT8644S will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8644S. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.6V supply from SV_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8644S's circuitry. Voltage on $INTV_{CC}$ will vary between 2.6V and 3.6V when SV_{IN} is between 2.7V and 3.7V. If SV_{IN} is connected to a different supply than PV_{IN}, be sure to bypass with a local ceramic capacitor. Do not connect an external load to the $INTV_{CC}$ pin.

Frequency Compensation

Loop compensation determines the stability and transient performance, and is provided by the components tied to the V_C pin. Generally, a capacitor (C_C) and a resistor (R_C) in series to ground are used. Designing the compensation network is a bit complicated and the best values depend on the application. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. LTpowerCAD® simulations can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

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Figure 5 shows an equivalent circuit for the LT8644S control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switches, and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. A zero is required and comes from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider can be used to improve the transient response and is required to cancel the parasitic pole caused by the feedback node to ground capacitance.

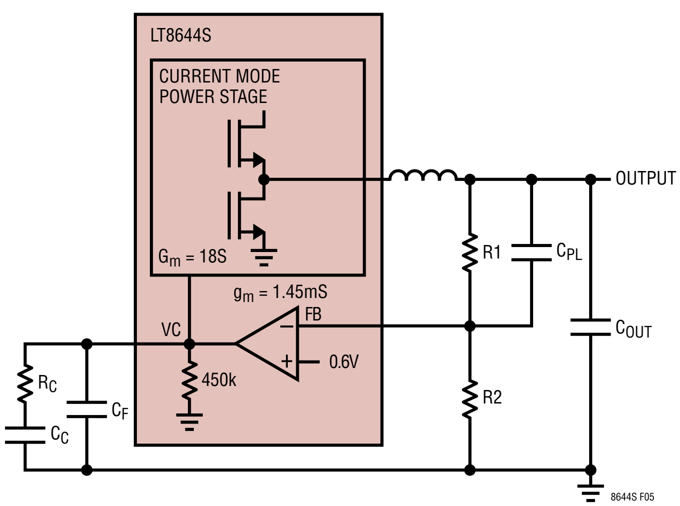


Figure 5. Model for Loop Response

Output Voltage Tracking and Soft-Start

The LT8644S allows the user to program its output voltage ramp rate by means of the SS pin. An internal 2μA pulls up the SS pin to $INTV_{CC}$. Putting an external capacitor on SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the SS pin voltage. For output tracking applications, SS can be externally driven by another voltage source. From 0V to 1V, the SS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the FB pin voltage to a function of the SS pin. See plot in Typical Performance Characteristics section. When SS is above 1V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8644S's output voltage is within the ±7.75% window of the regulation point, the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching, both the upper and lower thresholds include 0.4% of hysteresis. PG is valid when SV_{IN} is above 2.7V.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 0.98V, $INTV_{CC}$ has fallen too low, SV_{IN} is too low, or thermal shutdown.

Multiphase Operation

For output loads that demand more current, multiple LT8644Ss can be connected in parallel to the same output. To do this, the V_C, FB and SS pins are connected together, and each LT8644S's SW node is connected to the common output through its own inductor. The CLKOUT signal can be connected to the SYNC/MODE pin of the following LT8644S to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to ground, $INTV_{CC}$, or floating the pin generates a phase difference between the LT8644S's internal clock and CLKOUT of 180 degrees, 90 degrees, or 120 degrees respectively, which corresponds to 2-phase, 4-phase, or 3-phase operation. A total of 12 phases can be paralleled to run simultaneously with interleaving phase shift with respect to each other by programming the PHMODE pin of each LT8644S to

APPLICATIONS INFORMATION

different voltage levels. During FCM, Spread Spectrum, and Synchronization modes, all devices will operate at the same frequency. Figure 6 shows a 2-phase application where two LT8644Ss are paralleled to get one output capable of up to 32A.

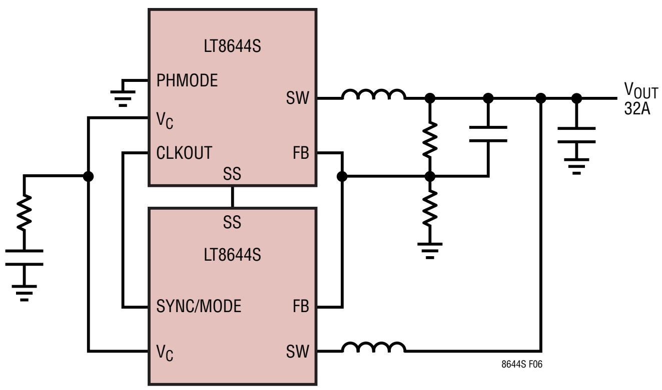


Figure 6. Paralleling Two LT8644Ss

Shorted and Reversed Input Protection

The LT8644S will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels.

Frequency foldback behavior depends on the state of the SYNC pin: If the SYNC pin is low the switching frequency will slow while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source, floated or tied high, the LT8644S will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output will be held high when the input to the LT8644S is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is diode ORed with the LT8644S's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8644S's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate current draw in this state. If the EN pin is grounded the SW pin current will drop to near 6μA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8644S can pull current from the output through the SW pin and the V_{IN} pin. Figure 7 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8644S to run only when the input voltage is present and that protects against a shorted or reversed input.

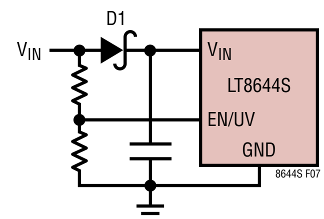


Figure 7. Reverse V_{IN} Protection

Thermal Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8644S. The ground pins on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8644S. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8644S can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8644S power dissipation by the thermal resistance from junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT8644S. If the junction temperature reaches approximately 165°C, the LT8644S will stop switching and indicate a fault condition until the temperature drops about 5°C cooler.

APPLICATIONS INFORMATION

Temperature rise of the LT8644S is worst when operating at high load, high PV_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either PV_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. Figure 8 shows examples of how case temperature rise can be managed by reducing switching frequency or load.

The LT8644S's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the output current the LT8644S can deliver for a given application. See curve in Typical Performance Characteristics.

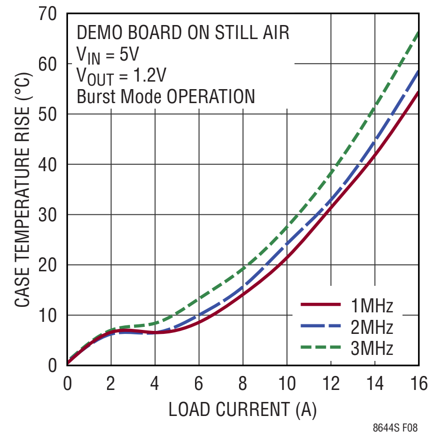


Figure 8. Case Temperature Rise

TYPICAL APPLICATIONS

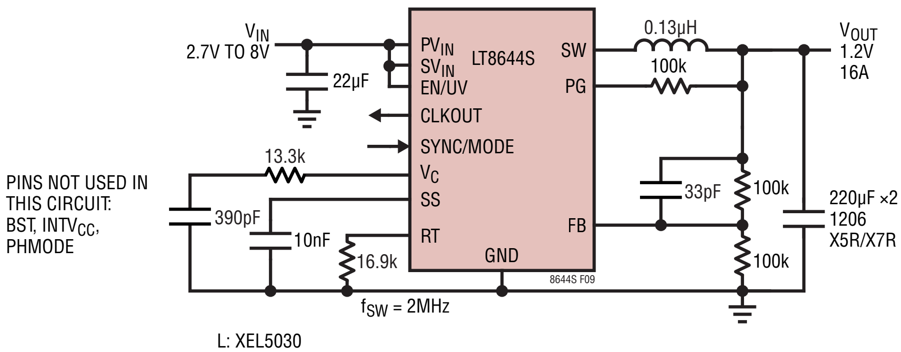


Figure 9. 2MHz 1.2V, 16A Step-Down Converter with Soft-Start and Power Good

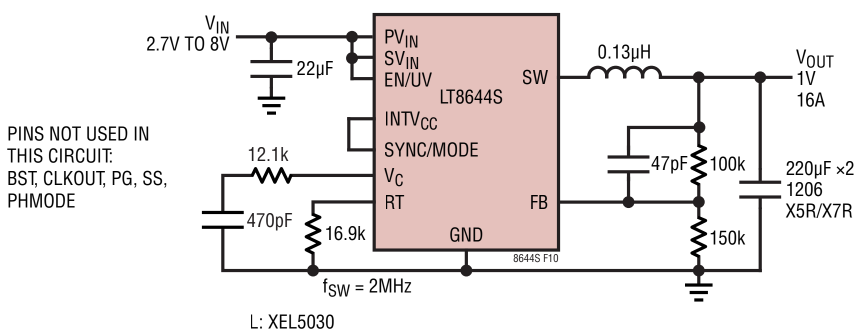
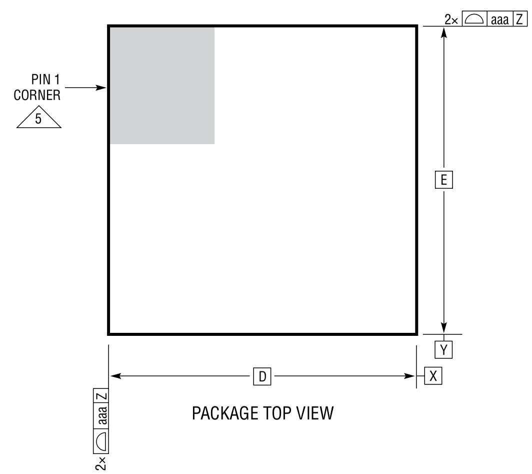
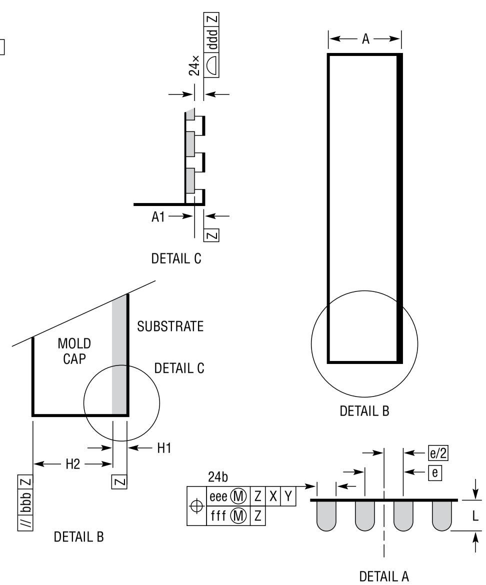


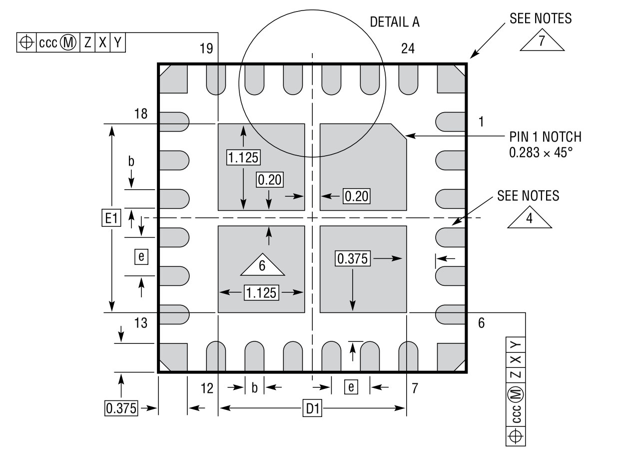
Figure 10. 2MHz 1V, 16A Step-Down Converter with Spread Spectrum

PACKAGE DESCRIPTION

LQFN Package
24-Lead (4mm × 4mm × 0.95mm)
(Reference LTC DWG # 05-08-7008 Rev Ø)

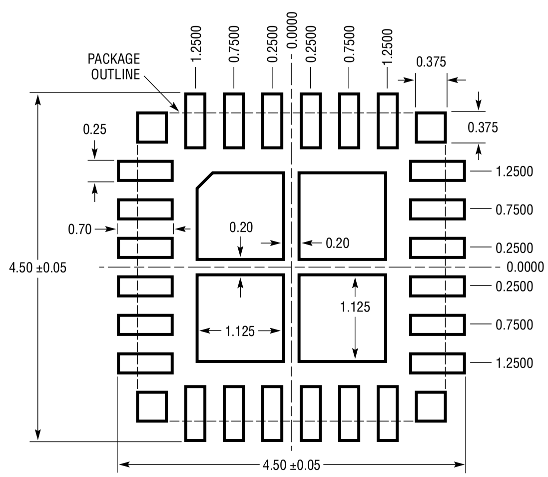






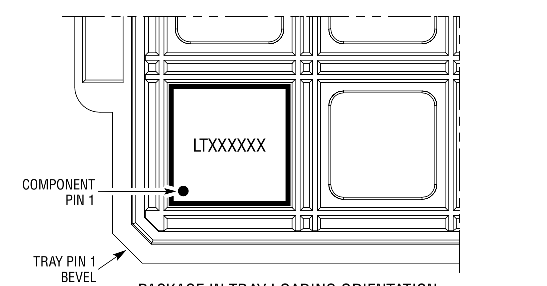
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		4.00		
D1		2.45		
E1		2.45		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	



PACKAGE IN TRAY LOADING ORIENTATION

LQFN 24 0819 REV Ø

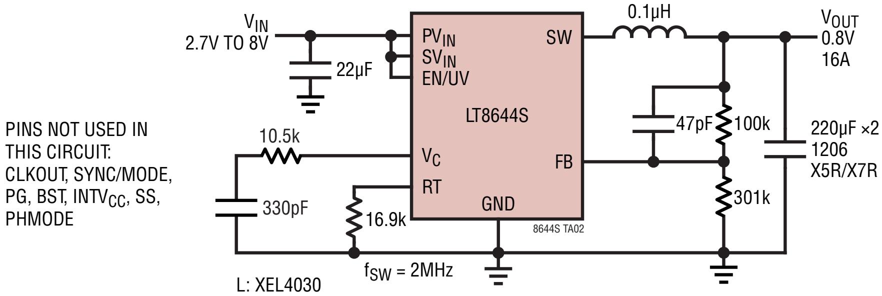
Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/21	Updated AEC-Q100 Statement	1

TYPICAL APPLICATION

0.8V, 16A Step-Down Converter



RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT8642S	18V, 10A Synchronous Step-Down Silent Switcher 2	V_{IN} = 2.8V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 240µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24
LTC3311/LTC3311S	5V, 12.5A, 5MHz Synchronous Step-Down Silent Switcher/Silent Switcher 2	V_{IN} = 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.5V, I_Q = 1.7mA, I_{SD} = 1µA, 3mm × 3mm LQFN-18
LTC3310/LTC3310S	5V, 10A, 5MHz Synchronous Step-Down Silent Switcher/Silent Switcher 2	V_{IN} = 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.5V, I_Q = 1.7mA, I_{SD} = 1µA, 3mm × 3mm LQFN-18
LTC3309A/LTC3309B	5V, 6A, 3MHz/10MHz Synchronous Step-Down Silent Switcher	V_{IN} = 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.5V, I_Q = 40µA, I_{SD} = 1µA, 2mm × 2mm LQFN-12
LT8648S	42V, 15A, 2.2MHz Synchronous Step-Down Silent Switcher 2	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 100µA, I_{SD} = 6µA, 7mm × 4mm LQFN-36
LT8636	42V, 5A, 3MHz Synchronous Step-Down Silent Switcher with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 4mm × 3mm LQFN-20
LT8650S	42V, Dual 4A, 3MHz Synchronous Step-Down Silent Switcher 2 with I_Q = 6.2µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.2µA, I_{SD} = 1.7µA, 4mm × 6mm LQFN-32
LT8653S	42V, Dual 2A, 3MHz Synchronous Step-Down Silent Switcher 2 with I_Q = 6.2µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.2µA, I_{SD} = 1.7µA, 4mm × 3mm LQFN-20
LT8652S	18V, Dual 8.5A, 3MHz Synchronous Step-Down Silent Switcher 2 with I_Q = 16µA	V_{IN} = 3V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 16µA, I_{SD} = 6µA, 4mm × 7mm LQFN-36
LT8640S/LT8643S	42V, 6A Synchronous Step-Down Silent Switcher 2 with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24
LT8645S/LT8646S	65V, 8A, Synchronous Step-Down Silent Switcher 2 with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 6mm × 4mm LQFN-32
LT8640/LT8640-1	42V, 5A, 3MHz Synchronous Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.99V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18
LT8641	65V, 3.5A, 3MHz Synchronous Step-Down Silent Switcher with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.81V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18
LT8609/LT8609A	42V, 2A, 2.2MHz Synchronous Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-10E