

# IS32SE5117

## 16-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

July 2023

### GENERAL DESCRIPTION

IS32SE5117 is an ultra-low-power, 16-channel capacitive touch controller. The controller allows sleep mode (under 10uA) and uses auto-detection for wakeup. It also provides a shield output to increase moisture immunity. The built-in hardware monitor and calibration for the environment is to prevent false triggers.

A host MCU is required to communicate with IS32SE5117. An on-chip I<sup>2</sup>C slave controller with 100kHz capability serves as the communication port for the host MCU. An interrupt, INT, can be configured and it is generated when a touch trigger event occurs. Trigger conditions can be configured by setting the interrupt register. IS32SE5117 can support proximity sensing.

IS32SE5117 is available in the wettable flank WQFN-24 package. It operates from 2.7V to 5.5V over the temperature range from -40°C to +125°C.

- Optional multiple-key function
- GPIO toggle/invert function
- Automatic calibration
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- Shield output shared with touch key channels
- Buzzer/Melody Generator shared with touch key channels
- 100kHz fast-mode I<sup>2</sup>C interface
- Operating temperature between -40°C ~ +125°C
- Wettable flank WQFN-24
- RoHS & Halogen-Free compliant package
- AEC-Q100 qualification
- TSCA compliance

### FEATURES

- 16-channel capacitive touch controller with readable key value
- Touch threshold setting for individual key

### APPLICATIONS

- Touch keys for home appliances
- Touch keys for industrial control
- Touch keys for automotive control

### TYPICAL APPLICATION CIRCUIT (Wettable flank WQFN-24)

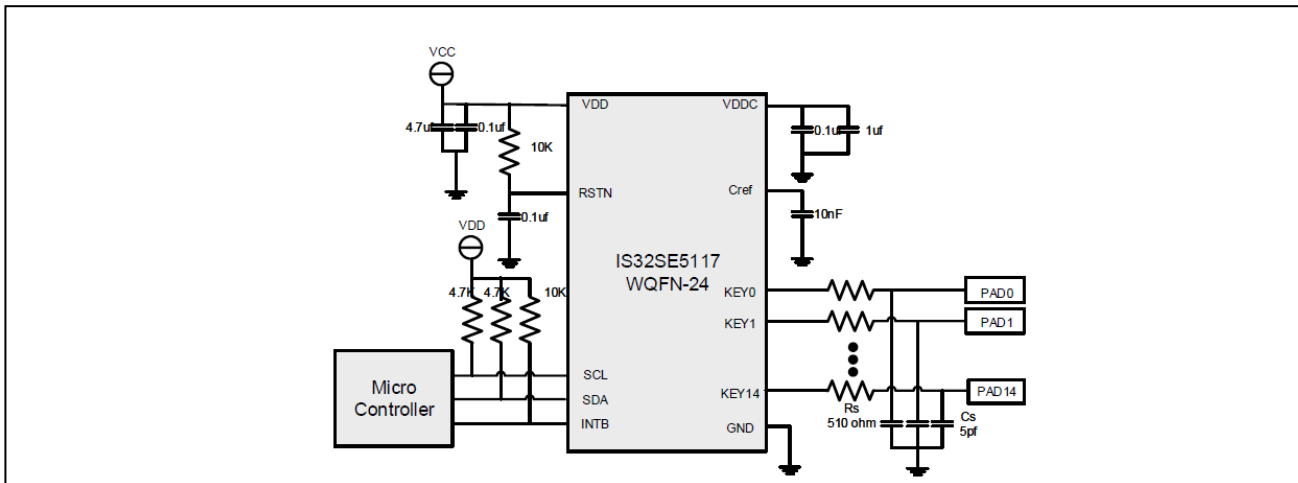


Figure 1 Typical Application Circuit (Wettable flank WQFN-24)

**Note 1:** The IC should be placed far away from the noise source to prevent EMS.

**Note 2:** The R<sub>S</sub> and C<sub>S</sub> should be placed as close to IC as possible to reduce EMI.

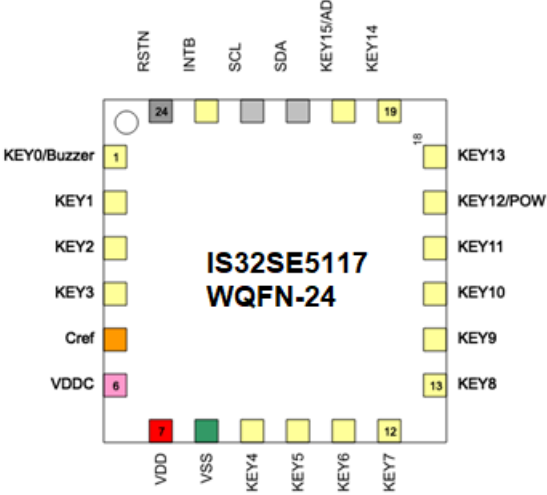
**Note 3:** The AD pin can be configured as KEY15.

**Note 4:** The capacitors connected to VDD and VDDC should be as close to the chip as possible to reduce EMI.

**Note 5:** The capacitor 1uF connected to VDDC might need to be removed for quick VDD rising time application.

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## PIN CONFIGURATION

Package	Pin Configuration (Top View)
Wettable flank WQFN-24	

## PIN DESCRIPTION

No.	Pin	Description
1	KEY0/Buzzer	Multiple function key. Can be configured to input sense channel 0, or Buzzer output.
2 - 4	KEY1 – KEY3	Input sense channel 1 – 3
5	Cref	External reference Capacitor for touch sense
6	VDDC	Internal 1.5V power supply. Typical decoupling capacitors of 0.1µF and 1µF should be connected. between VDDC and GND.
7	VDD	Power supply
8	VSS	Ground
9 – 16	KEY4 – KEY11	Input sense channel 4 - 11
17	KEY12/POW	Multiple function key. Can be configured to input sense channel 12, or Melody power control.
18 – 19	KEY13 – KEY14	Input sense channel 13 - 14
20	AD/KEY15	Multiple function key. Can be configured to I2C address or input sense channel 15.
21	SDA	I2C serial data
22	SCL	I2C serial clock
23	INTB	Interrupt output (active low)
24	RSTN	Reset Low Active

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## ORDERING INFORMATION

**Industrial Range: -40°C to +125°C**

Order Part No.	Package	QTY
IS32SE5117- QWLA3 -TR	Wettable flank WQFN-24, Lead-free	2500/Reel

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## ABSOLUTE MAXIMUM RATINGS

Supply voltage, VDD	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ VDD+0.3V
Maximum junction temperature, T <sub>JMAX</sub>	+150°C
Storage temperature range, T <sub>STG</sub>	-65°C ~ +150°C
Operating temperature range T <sub>A</sub>	-40°C ~ +125°C
Junction Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), $\theta_{JA}$ (Wettable flank WQFN-24)	29°C/W
ESD (HBM)	±2kV
ESD (CDM)	±750V

**Note 6:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25°C, VDD = 2.7V ~ 5.5V, unless otherwise noted. Typical values are T<sub>A</sub> = 25°C, VDD = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage		2.7		5.5	V
IDD Normal	Total IDD through VDD at 16MHz			7		mA
IDD versus Frequency	Total IDD Core Current versus Frequency	VDD = 5.5V		150		μA/ MHz
IDD, Stop	IDD, stop mode	VDD = 5.5V		150		μA
IDD, Sleep	IDD, sleep mode, 25°C	Main regulator off		1	3	μA
	IDD, sleep mode, 125°C	Main regulator off		15	30	μA
ΔC <sub>s</sub>	Minimum detectable capacitance	C <sub>s</sub> = 5pF (Note 7)		0.2		pF
<b>GPIO DC Characteristics</b>						
VOH,4.5V	Output High Voltage 1 mA	Reference to VDD		-0.2	-0.4	V
VOL,4.5V	Output Low Voltage 8 mA	Reference to VSS		0.3	0.5	V
VOH,3.0V	Output High Voltage 1 mA	Reference to VDD		-0.3	-0.5	V
VOL,3.0V	Output Low Voltage 8 mA	Reference to VSS		0.3	0.5	V
I <sub>IOT</sub>	Total IO Sink and Source Current		-100		100	mA
VIH	Input High Voltage		$\frac{3}{4}VDD$			V
VIL	Input Low Voltage				$\frac{1}{4}VDD$	V
VIHYS	Input Hysteresis			600		mV
RPU	Equivalent Pull-Up resistance			5K		Ohm
RPU,RSTN	RSTN Pull-Up resistance			5K		Ohm
RPD	Equivalent Pull-Down Resistance			5K		Ohm
REQAN1	Equivalent ANIO Switch Resistance, 3.3V	ANIO1 Switch		220		Ohm
	Equivalent ANIO Switch Resistance, 5V	ANIO1 Switch		70		Ohm
REQAN2	Equivalent ANIO Switch Resistance, 3.3V	ANIO2 Switch		220		Ohm

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	Equivalent ANIO Switch Resistance, 5V	ANIO2 Switch		70		Ohm
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## DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 7)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f <sub>SCL</sub>	Serial-Clock frequency				100	kHz
t <sub>BUF</sub>	Bus free time between a STOP and a START condition		1.3			μs
t <sub>HD, STA</sub>	Hold time (repeated) START condition		0.6			μs
t <sub>SU, STA</sub>	Repeated START condition setup time		0.6			μs
t <sub>SU, STO</sub>	STOP condition setup time		0.6			μs
t <sub>HD, DAT</sub>	Data hold time				0.9	μs
t <sub>SU, DAT</sub>	Data setup time		100			ns
t <sub>LOW</sub>	SCL clock low period		1.3			μs
t <sub>HIGH</sub>	SCL clock high period		0.7			μs
t <sub>R</sub>	Rise time of both SDA and SCL signals.	(Note 8)		20+0.1C <sub>b</sub>	300	ns
t <sub>F</sub>	Fall time of both SDA and SCL signals.	(Note 8)		20+0.1C <sub>b</sub>	300	ns

**Note 7:** Guaranteed by design.

**Note 8:** C<sub>b</sub> = total capacitance of one bus line in pF. I<sub>SINK</sub> ≤ 6mA. t<sub>R</sub> and t<sub>F</sub> measured between 0.3 × V<sub>DD</sub> and 0.7 × V<sub>DD</sub>.

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## FUNCTION BLOCK DIAGRAM

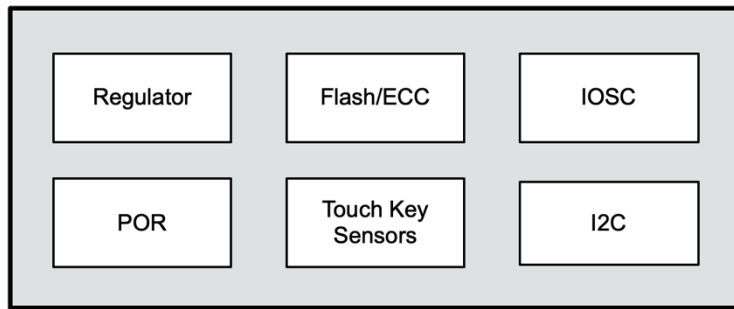


Figure 2: Function Block Diagram

### Basic introduction for touch sense data process flow

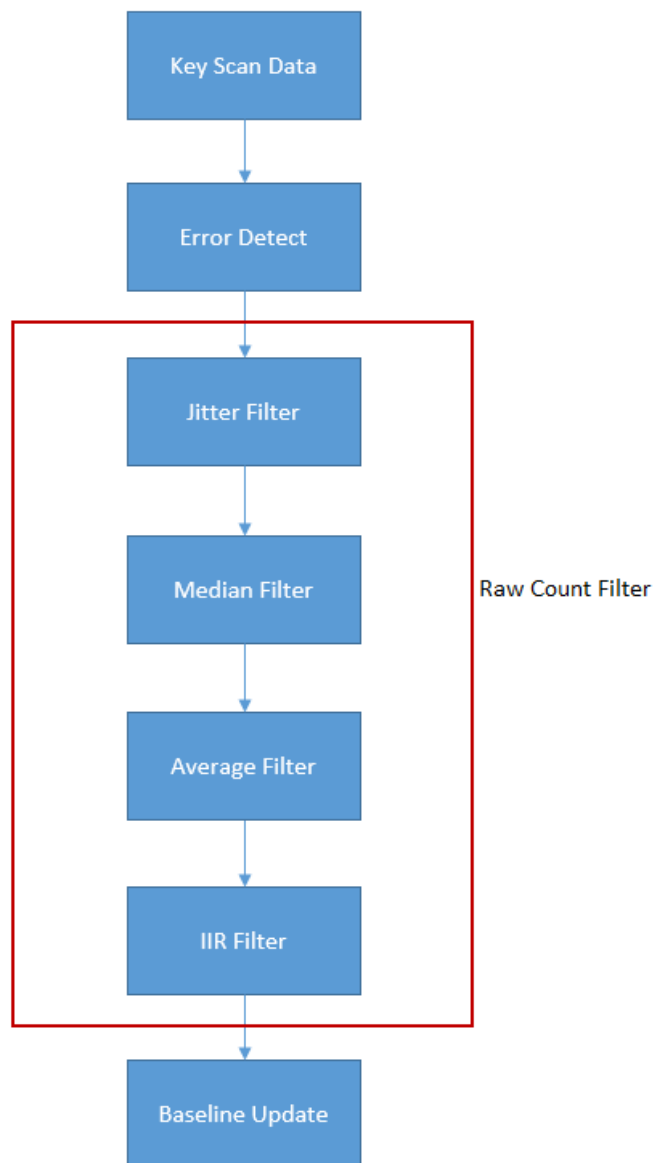


Figure 3: Touch Sense Data Process Flow

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## Baseline process based on the difference of baseline and raw count

Baseline will be updated to the current raw count based on the below factors. For detailed information about baseline, please refer to Section 4.4.2 Key parameter in “IS31SE5117A Eval Board User’s Manual with Safety Self-Test” application note.

### Positive noise threshold

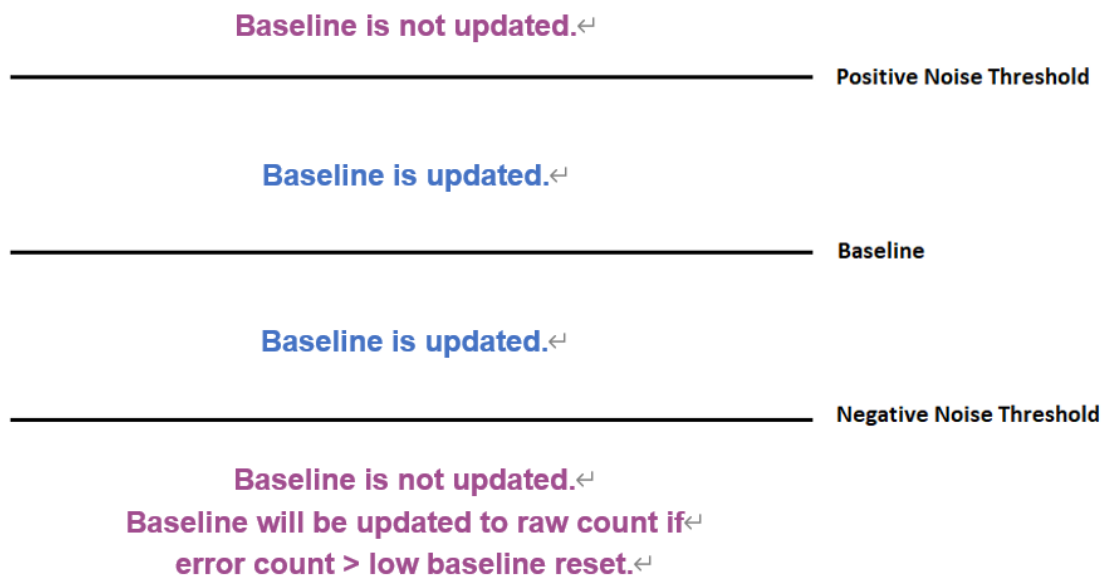
Baseline is updated if the difference count of baseline count and raw count is below the positive noise threshold.

### Negative noise threshold

It is used with the low baseline reset count to reset baseline count to the current raw count. Please refer to the description of **Low baseline reset**.

### Low baseline reset

Low baseline reset count of each key. A reset count increases one if the absolute  $|raw\ count - baseline| > negative\ noise\ threshold$ . Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute  $|raw\ count - baseline| \leq negative\ noise\ threshold$ .



**Figure 4: Baseline Process based on the difference of baseline and raw count**

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## Touch sense data identification

Ignore the touch key scan if the signal exceeds the lock threshold.

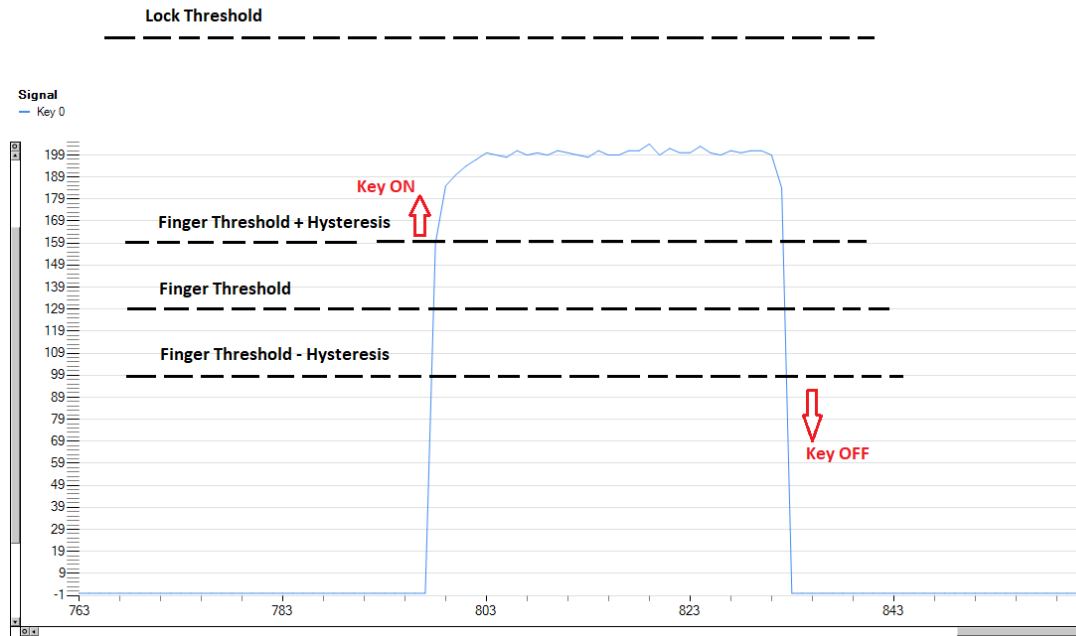


Figure 5: Touch Sense Data Identification



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## DETAILED DESCRIPTION

### I2C INTERFACE

The IS32SE5117 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. IS32SE5117 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 "0" for a write command and set A0 "1" for a read command. The value of bits A1 and A2 are determined by the connection of the AD pin, to GND, VDD, or Floating.

The complete slave address is:

Bit	A7:A3	A2:A1	A0
Value	01111	AD	1/0

AD floating, AD = 00;

AD connected to GND, AD = 01;

AD connected to VDD, AD = 10;

AD pin can also be configured as a Touch Key channel. When AD pin is used for a Touch Key channel, A2: A1 = 00.

The SCL line is uni-directional. The SDA line is bi-directional (open collector) with a pull-up resistor (typically 4.7kΩ). During communication, microcontroller is the master and IS32SE5117 is the slave.

The timing diagram for the I2C is shown in Figure 6. The SDA is latched on to the stable high level of the SCL. When there is no bus activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, and the most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for IS32SE5117 acknowledgement. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If IS32SE5117 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32SE5117, the register address byte is sent, and the most significant bit first. IS32SE5117 must generate another acknowledgment indicating that the register address has been received.

Then 8-bit of data bytes are sent next, the most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, IS32SE5117 must generate another acknowledgment to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

### READING PORT REGISTERS

To read the device data, the bus master must first send the address of IS32SE5117 with the R/W bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must send IS32SE5117 address with the R/W bit set to "1". Data from the register defined by the command byte is sent from IS32SE5117 to the master (Figure 9).

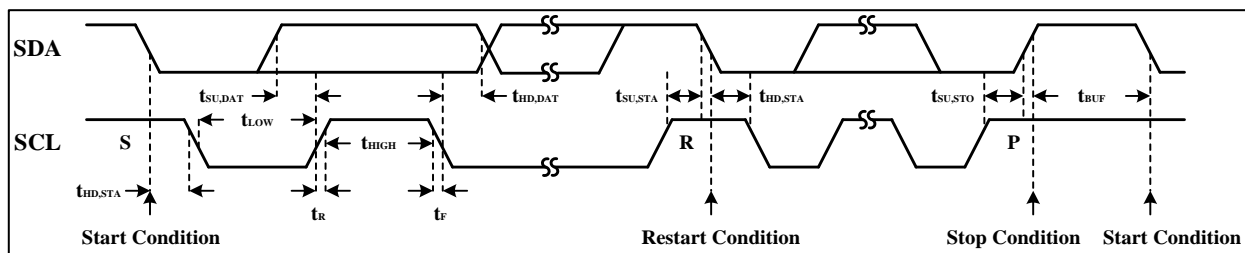


Figure 6: Interface Timing

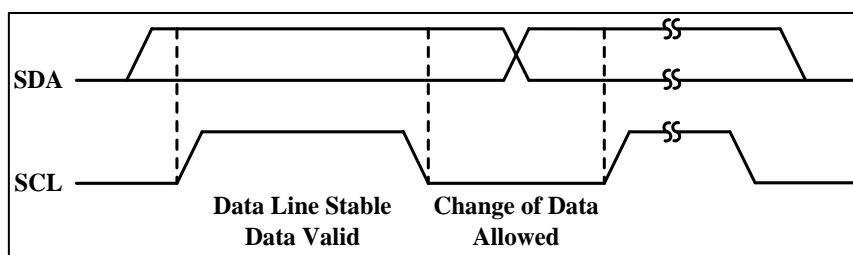
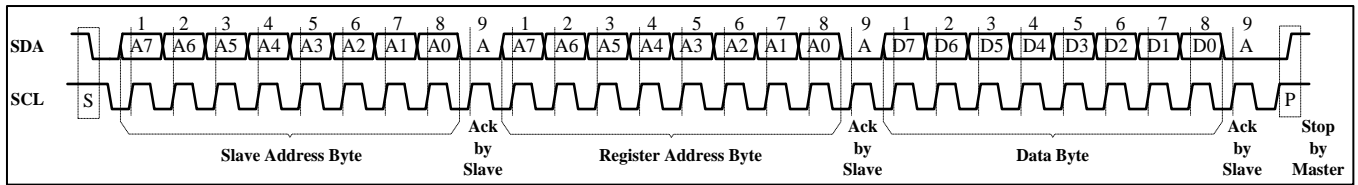
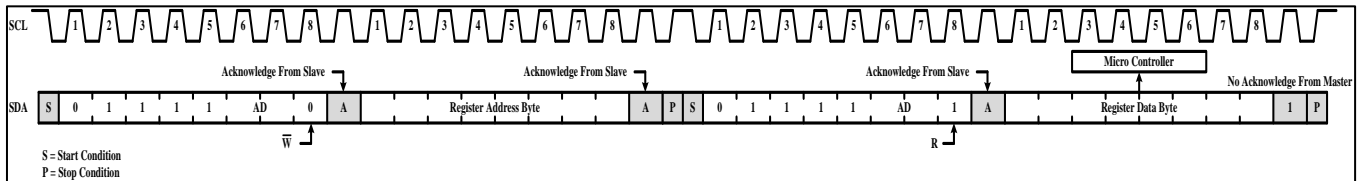


Figure 7: Bit Transfer

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**Figure 8: Writing to IS32SE5117**



**Figure 9: Reading from IS32SE5117**

**Note:** Successive read or write protocol is supported.

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## REGISTER DEFINITION

### Page 0 register

Address	Name	Definition	R/W	Default
00h	Chip Part Number	Chip's part number	R	17h
01h-02h	Chip Version	Chip's version	R	-
03h	Firmware Version	Firmware version	R	40h
04h	Main Control	System reset, power saving and parameters management	W	00h
05h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
06h-07h	Key Status	Key 0-Key 15 status bits	R	00h
08h	BM	Buzzer data or stop command	W	-
08h	BM	Available buzzer buffer size	R	0Ah
09h-18h	Key Signal	Key 0-Key 15 signal value	R	00h
19h-38h	Key Raw Count	Key 0-Key 15 raw count value	R	00h
39h-58h	Key Baseline	Key 0-Key 15 baseline value	R	00h
59h-68h	Key Finger Threshold	Key 0-Key 15 finger threshold setting	R/W	50h
69h-78h	Key Noise Threshold	Key 0-Key 15 noise threshold setting	R/W	28h
79h-88h	Key Negative Noise Threshold	Key 0-Key 15 negative noise threshold setting	R/W	28h
89h-98h	Key Low Baseline Reset	Key 0-Key 15 low baseline reset setting	R/W	1Eh
99h-A8h	Key Hysteresis	Key 0-Key 15 hysteresis setting	R/W	09h
A9h-B8h	Key ON Debounce	Key 0-Key 15 debounce setting	R/W	03h
B9h-BAh	Key Interrupt Enable	Key 0-Key 15 enables Interrupts associated with capacitive touch sensor inputs	R/W	00h
BBh	Raw Count Filter	Raw count filter setting	R/W	00h
BCh	Baseline IIR Ratio	Baseline IIR ratio setting	R/W	01h
BDh-BEh	Lock Threshold	Lock threshold setting	R/W	03E8h
BFh	Lock Scan Cycle	Lock scan cycle setting	R/W	08h
C0h	Raw Count Difference Limit	Raw count difference limit setting	R/W	64h

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C1h	Multi Touch Key Configure	Multiple touch key function setting	R/W	03h
C2h	Max Duration Time	Maximum duration time setting	R/W	1Ah
C3h	Interrupt Configuration	Interrupt configuration	R/W	0Ah
C4h	Interrupt Repeat Time	Repeat cycle for pressing key interrupt setting	R/W	00h
C5h	Key Pin Select	Select pins as Key0-Key7	R/W	00h
C6h	Key Pin Select	Select pins as Key8-Key15	R/W	00h
C7h-C8h	Shield Pin Select	Select pin as shield	R/W	0040h
C9h-CAh	INT Pin Select	Select pin as INT	R/W	0000h
CBh-CCh	Buzzer Pin Select	Select pin as buzzer	R/W	0100h
CDh-CEh	POW Pin Select	Select pin as buzzer power	R/W	0000h
CFh	GPIO Pin Select	Sets the GPIO enable KEY0~KEY7	R/W	0Eh
D0h	GPIO Pin Select	Sets the GPIO enable KEY8~KEY15	R/W	00h
D1h	Slider 1 Pin Select	Max 6 keys	R/W	00h
D2h	Slider 1 Pin Select	Max 6 keys	R/W	3Fh
D3h-D4h	Slider 2 Pin Select	Max 6 keys	R/W	0000h
D5h	TKIII Control register 1	Repeat sequence, initial setting delay, auto mode start delay, and low frequency noise filter	R/W	13h
D6h	TKIII Control register 2	Pseudo random sequence setting	R/W	20h
D7h	TKIII Control register 3	Multi frequency scan/cycle count setting	R/W	03h
D8h	TKIII CCHG	Internal charge capacitance setting	R/W	60h
D9h	TKIII PUD	Pull-up current/ pull-up resistors setting	R/W	00h
DAh	System Clock Select	System clock setting	R/W	00h
DBh	Spread Spectrum	Spread spectrum setting	R/W	0Ch
DCh	Auto Sleep Mode	Auto enter sleep mode time setting	R/W	0Fh

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DDh	Sleep Mode Control	Sleep mode control setting	R/W	00h
DEh-DFh	Wake Up Key Select	Select Key0~Key15 to exit sleep mode	R/W	0000h
E0h	Wake Up Threshold	Wake up threshold setting	R/W	08h
E1h	TKIII Sleep Mode CCHG	Sleep mode internal charge capacitance setting	R/W	60h
E2h	TKIII Sleep Mode PUD	Sleep mode pull-up current/ pull-up resistors setting	R/W	00h
E3h-E4h	SLP_RAW	Sleep mode raw count value	R	0000h
E5h-E6h	SLP_Baseline	Sleep mode baseline value	R	0000h
E7h-ECh	Slider 1-2 status	3 slider status registers for each slider	R/W	E9h 80h, others 00h
EDh	Slider 1 Mapping	Slider 1 Key position	R/W	89h
EEh	Slider 1 Mapping	Slider 1 Key position	R/W	ABh
EFh	Slider 1 Mapping	Slider 1 Key position	R/W	CDh
F0h-F2h	Slider 2 Mapping	Slider 2 Key position	R/W	00h
F3h-FEh	Slider 1-2 Calibration	Slider 1-2 Calibration	R/W	28h

## Page 1 Register list (extension memory)

Address	Name	Definition	R/W	Default
0100h	Chip Part Number	Chip's part number	R	17h
0101h-0102h	Chip Version	Chip's version	R	-
0103h	Firmware Version	Firmware version	R	40h
0104h	Main Control	System reset, power saving and parameters management	W	00h
0105h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
0106h-0107h	Key Status	Key 0-Key 15 status bits	R	00h
0108h	BM	Buzzer data or stop command	W	-
0108h	BM	Available buzzer buffer size	R	0Ah
0109h	GPIO Value 1	Sensing the GPIO values for KEY0 – KEY7	R/W	0Eh

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010Ah	GPIO Value 2	Sensing the GPIO values for KEY8 – KEY15	R/W	00h
010Bh	GPIO Enable 1	Enable key KEY0 – KEY7 for GPIO	R/W	70h
010Ch	GPIO Enable 2	Enable key KEY8 – KEY15 for GPIO	R/W	00h
010Dh	GPIO Mapping 1	Key to GPIO mapping; see register for details	R/W	00h
010Eh	GPIO Mapping 2	Key to GPIO mapping; see register for details	R/W	00h
010Fh	GPIO Mapping 3	Key to GPIO mapping; see register for details	R/W	12h
0110h	GPIO Mapping 4	Key to GPIO mapping; see register for details	R/W	03h
0111h-0114h	GPIO Mapping 5-8	Key to GPIO mapping; see register for details	R/W	00h
0115h	GPIO Toggle EN 1	Enable GPIO Toggle mode for KEY0 – KEY7	R/W	10h
0116h	GPIO Toggle EN 2	Enable GPIO Toggle mode for KEY8 – KEY15	R/W	00h
0117h	Key Scan Once	I2C control key scan	R/W	00h
0118h	Table Ready Mark	Mark for flash data ready	R	00h

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## Page 0 Registers

### 00h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0001 0111

#### CPN Chip Part Number

Chip's part number 17h

### 01h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

#### CV1 Chip Version information 1

### 02h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

#### CV2 Chip Version information 2

CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

### 03h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	010	000	00

#### FV Firmware Version

Default version is 2.0.0

FV1[2:0] Major version

FV2[2:0] Minor version

FV3[1:0] Patch version

### 04h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	SR	RD	-	SP	SS	-
Default	0	0	0	0	0	000

#### SR System Reset

1 System reset

#### RD Reset All Parameters to Manufacturer Default Setting.

1 Reset all user defined parameters to manufacture default setting.

#### SP Sleep Mode

1 Sleep mode

#### SS Save User Defined Parameters

1 Save current parameters into flash.

### 05h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)

FLAG=1 Page 1 (Address: 0x100~0x1FF)

### 06h Key Status Register 1 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

#### KSx Key0~Key7 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

### 07h Key Status Register 2 (RO)

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

#### KSx Key8~Key15 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

### 08h Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

#### BM Buzzer Register Write

Buzzer data or stop command

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## 08h Buzzer Register (R)

Bit	D7:D0
Name	BM[7:0]
Default	0000 1010

### BM Buzzer Register Read

It shows the available tone buffer size. IS32SE5117 has 10 built-in note buffers.

## 09h~18h KEY0~KEY15 Signal Register (RO)

Bit	D7:D0
Name	KEYx_SIGNAL[7:0]
Default	0000 0000

### KEYx\_SIGNAL Key Signal Count

The difference between baseline and raw count. The maximum value is 254. It will keep 254 if the value is over 254. Value 255 means noise existence.

## 19h, 1Bh..., 35h, 37h KEY0~KEY15 Raw Count High Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[15:8]
Default	0000 0000

## 1Ah, 1Ch..., 36h, 38h KEY0~KEY15 Raw Count Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[7:0]
Default	0000 0000

### KEYx\_RAWCOUNT

The raw count of each key provides an indication of the magnitude of the sensor's capacitance.

## 39h, 3Bh ..., 55h, 57h KEY0~KEY15 Baseline High Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[15:8]
Default	0000 0000

## 3Ah, 3Ch ..., 56h, 58h KEY0~KEY15 Baseline Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[7:0]
Default	0000 0000

### KEYx\_Baseline

Baseline of each key

## 59h~68h KEY0~KEY15 Finger Threshold Register (RW)

Bit	D7:D0
Name	KEYx_TH[7:0]
Default	0101 0000

### KEYx\_TH

Finger threshold of each key. It is used with hysteresis to determine the key state.

## 69h~78h KEY0~KEY15 Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NTH[7:0]
Default	0010 1000

### KEYx\_NTH

Noise threshold of each key. Baseline needs to be updated if the difference (baseline and raw count) is less than the noise threshold.

## 79h~88h KEY0~KEY15 Negative Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NNTH[7:0]
Default	0010 1000

### KEYx\_NNTH

Negative noise threshold of each key.

## 89h~98h KEY0~KEY15 Low Baseline Reset Register (RW)

Bit	D7:D0
Name	RCx[7:0]
Default	0001 1110

### RCx Reset Count

Low baseline reset count of each key. A reset count increases one if the absolute  $|raw\ count - baseline| > absolute\ |negative\ noise\ threshold|$ . Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute  $|raw\ count - baseline| \leq absolute\ |negative\ noise\ threshold|$ .



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## 99h~A8h KEY0~KEY15 Hysteresis Register (RW)

Bit	D7:D0
Name	HYSTERESISx[7:0]
Default	0000 1001

### HYSTERESISx

Hysteresis of each key

## A9h~B8h KEY0~KEY15 On Debounce Register (RW)

Bit	D7:D0
Name	DEBOUNCEx[7:0]
Default	0000 0011

### DEBOUNCEx

Debounce number of each key. When the acquired number > debounce setting value, then the key is granted as on.

## B9h~BAh Key Interrupt Enable Register (RW)

Bit	D7:D0
Name	INTEN[7:0]
Default	0000 0000

The Interrupt Enable Register determines whether a key causes the interrupt pin to be asserted when it is detected touched with the key's interrupt enable bit set.

### INTEN Key Interrupt Enable

0	Disable
1	Enable

The default value for Interrupt Enable Registers is interrupt disable. Setting INE bit of Interrupt Configuration Register (C3h) to "1", INTB pin will generate interrupt signal.

## BBh Raw Count Filter Register (RW)

Bit	D7	D6	D5:D4	D3	D2:D1	D0
Name	MF	AF	IIR[1:0]	JF	JD[1:0]	-
Default	0	0	00	0	00	0

### MF Median Filter

0	Disable
1	Enable

### AF Average Filter

0	Disable
1	Enable

### IIR IIR Filter

00	Disable
01	1/2
10	1/4
11	1/8

### JF Jitter Filter

0	Disable
1	Enable

### JD Jitter Delta

00	1
01	2
10	4
11	8

## BCh Baseline IIR Ratio Register (RW)

Bit	D7:D0
Name	RATIO[7:0]
Default	0000 0001

### RATIO

Range 1 ~ 255

## BDh Lock Threshold High Byte Register (RW)

Bit	D7:D0
Name	LT[15:8]
Default	0000 0011

## BEh Lock Threshold Low Byte Register (RW)

Bit	D7:D0
Name	LT[7:0]
Default	1110 1000

### LT Lock Threshold

## BFh Lock Scan Cycle Register (RW)

Bit	D7:D0
Name	LSC[7:0]
Default	0000 1000

### LSC Lock Scan Cycle

Ignore the key scan data for the setting Lock scan cycle if the |raw count – baseline| > Lock threshold.

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## C0h Raw Count Difference Limit Register (RW)

Bit	D7:D0
Name	RCDL[7:0]
Default	0110 0100

### RCDL Raw Count Difference Limit

Ignore the key scan data if the difference between previous raw count and current raw count exceeds the limit.

## C1h Multiple Touch Key Configure Register (RW)

Bit	D7:D2	D1:D0
Name	-	MTK[1:0]
Default	000000	11

### MTK Multi Touch Key

- 01 Allow one key triggered at one time.
- 10 Allow two keys triggered at one time.
- 11 Allow three keys triggered at one time.

## C2h Max Duration Time Register (RW)

Bit	D7	D6	D5	D4	D3:D0
Name	-	-	-	MDEN	MDT[3:0]-
Default	0	0	0	1	1010

### MDEN Maximum Duration Time Enable

- 0 Disable
- 1 Enable

### MDT Maximum Duration Time

- 0000 0.5s
- 0001 1s
- 0010 2s
- 0011 3s
- 0100 4s
- 0101 5s
- 0110 6s
- 0111 7s
- 1000 8s
- 1001 9s
- 1010 10s
- 1011 11s
- 1100 12s
- 1101 13s
- 1110 14s
- 1111 15s

MDT bits set the pressed time. When key pressed duration exceeds the programmed time (MDT), device will be forced to calibrate the pressed key. Set MDEN to "1" will enable this function.

## C3h Interrupt Configuration Register (RW)

Bit	D7	D6:D4	D3	D2:D0
Name	INE	-	ACEN	ACT[2:0]
Default	0	000	1	010

### INE Interrupt Function Enable

- 0 Disable
- 1 Enable

### ACEN Auto-Clear Interrupt Enable

- 0 Disable
- 1 Enable

### ACT Auto-Clear Interrupt Time

- 000 10ms
- 001 20ms
- 010 30ms
- 011 40ms
- 100 50ms
- 101 100ms
- 110 150ms
- 111 200ms

When ACEN=0, the INT will keep low until device 06h or 07h register is read, or the key is released. When ACEN=1, the INT will be released after ACT setting time is expired even 06h or 07h register is not read, or key is still pressed.

## C4h Interrupt Repeat Time Register (RW)

Bit	D7:D4	D3:D0
Name	-	INTRT[3:0]
Default	0000	0000

### INTRT Interrupt Repeat Time

- 0000 disable
- 0001 50ms
- 0010 100ms
- 0011 150ms
- 0100 200ms
- 0101 250ms
- 0110 300ms
- 0111 350ms
- 1000 400ms

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1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

After INTRT is set, a second interrupt will be generated after the interrupt repeat time is expired if there is a key keeping pressed.

## C5h~C6h Key Pin Select Register (RW)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

## KS Key Pin Selection Setting

0	Disable
1	Enable

## C7h~C8h Shield Pin Select Register (RW)

Bit	D7:D0
Name	SHDE[7:0]
Default	0000 0000

Bit	D7:D0
Name	SHDE[15:8]
Default	0100 0000

## SHDE Shield Enable (default for SHDE[14])

0	Disable shield driver
1	Enable shield driver

## C9h~CAh INT Pin Select Register (RW)

Bit	D7:D0
Name	IPS1[7:0]
Default	0000 0000

Bit	D7:D0
Name	IPS1[15:8]
Default	0000 0000

IS32SE5117 interrupt Pin has been fixed at Pin 23 INTB and it doesn't work to set INT Pin Select Register C9h and CAh.

## CBh~CCh Buzzer Pin Select Register 1 (RW)

Bit	D7:D0
Name	BPS1[7:0]
Default	---- --- 1

Bit	D7:D0
Name	BPS2[7:0]
Default	---- ----

## BPS1/2 Buzzer output Select 1/2

Enable BPS1[0] will set Pin1 as Buzzer output pin.

BPS1[7:1] & BPS2[7:0] unused register bits.

## CDh Enable Buzzer Power Register 1 (RW)

Bit	D7:D0
Name	EBP1 [7:0]
Default	---- ----

## CEh Enable Buzzer Power Register 2 (RW)

Bit	D7:D0
Name	EBP2 [0]
Default	--- 0 ----

## EBP1/2 Buzzer Power Select 1/2

EBP1[7:0] unused register bits.

EBP2[4] maps to KEY12, write 1 will enable KEY12 as Buzzer Power. Setting other EBP2 bits doesn't work.

## CFh~D0h GPIO Pin Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 1110

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Bit	D7:D0
Name	GPIO[15:8]
Default	0000 0000

GPIO pin select will go with register 109h GPIO Value 1 and register 10Ah GPIO Value 2 to have GPIO pin high or low.

## D1h~D2h Slider1 Pin Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 0000

Bit	D7:D0
Name	GPIO[15:8]
Default	0011 1111

## D3h~D4h Slider2 Pin Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 0000

Bit	D7:D0
Name	GPIO[15:8]
Default	0000 0000

## D5h TKIII Control Register 1 (RW)

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	RPT	INI	ASTDLY	LFNF
Default	00	01	00	11

### RPT Repeat Sequence Count

00	No repeat
01	Repeat 4 times
10	Repeat 8 times
11	Repeat 16 times

### INI Initial Setting Delay

INI[1-0] defines the number of TKCLK period for initial settling of pin Cref. The delay is (INI[1-0] + 1) \* 4 \* TKCLK.

### ASTDLY Auto Mode Start Delay

ASTDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0] + 1) \* 256 TKCLK at each sequence start. This delay allows the stabilization time from normal mode to sleep mode.

### LFNF Low Frequency Noise Filter Setting

Low Frequency Noise Filter Setting

00 Disable LFNE

If the scan count with noise injection detection is larger than (LFNF [1-0] \* 8), the scan result is ignored.

## D6h TKIII Control Register 2 (RW)

Bit	D3	D2:D1	D0	
Name	-	-	-	
Default	0	00	0	
Bit	D7	D6	D5	D4
Name	-	-	PRS	-
Default	0	0	1	0

### PRS Pseudo Random Sequence

0	Disable PRS
1	Enable PRS

## D7h TKIII Control Register 3 (RW)

Bit	D7:D4	D3	D2:D0
Name	-	MFEN	CCNT[2:0]
Default	0000	0	011

### MFEN Multi Frequency Scan

0	Disable MF
1	Enable MF

### CCNT Cycle Count of Each Conversion Sequence

000	1024
001	2048
010	4096
011	8192
100	12288
101	16384
110	32768
111	65536

## D8h TKIII CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-

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Default	011	00000
---------	-----	-------

## CCHG Internal Reference Capacitance Select

000	10pF
001	20pF
010	30pF
011	40pF
100	50pF
101	60pF
110	70pF
111	80pF

## D9h TKIII PUD Register (RW)

Bit	D3:D0		
Name	PUD [3:0]		
Default	0000		
Bit	D7	D6	D5:D4
Name	PUDIEN	PUDREN	-
Default	0	00	00

TK3PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance which is caused by a high capacitance key. Connecting a constant current source or resistor can thus maintain touch key detection sensitivity. In general, we will try to maintain the raw count around half of CCNT for the case without key touched.

For DC current, PUD [3:0] enables 8uA/4uA/2uA/1uA current source. For Resistor, PUD [3-0] enables 5K/10K/20K/40K resistor.

### PUDIEN Pull-up/Pull-down DC Current Enable

### PUDREN Pull-up/Pull-down DC Resistor Enable

#### PUD Pull up DC Current

1000	Enable 8uA current source.
0100	Enable 4uA current source.
0010	Enable 2uA current source.
0001	Enable 1uA current source.

#### PUD Pull up Resistor

1000	Enable 5K resistor source.
0100	Enable 10K resistor source.
0010	Enable 20K resistor source.
0001	Enable 40K resistor source.

## DAh System Clock Select Register (RW)

Bit	D7:D4	D3	D2:D0
Name	-	CLKS	OSCD[2:0]
Default	0000	0	000

### CLKS Clock Stretching (For I2C)

0	Disable stretching
1	Enable stretching

### OSCD Oscillator Division

000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The default setting is 1 for 16MHz system clock.

## DBh Spread Spectrum Register (RW)

Bit	D7:D2		
Name	SSR[3:0]	SSA[1:0]	-
Default	0000	11	-

### SS Spread Spectrum Setting

With spread spectrum technique, electromagnetic energy produced over a particular bandwidth is spread in the frequency domain, and that can reduce EMI. Two parameters are listed as follows:

**SSR [3:0]** Defines the spread spectrum sweep rate. If the SSR[3:0] =0, then spread spectrum is disabled.

**SSA [1:0]** Defines how to adjust the spread spectrum frequency bandwidth. The frequency is adjusted by adding SSA [1:0] range to the actual internal OSC control register.

**SSA [1:0]=11** +/- 32

**SSA [1:0]=10** +/- 16

**SSA [1:0]=01** +/- 8

**SSA [1:0]=00** +/- 4

## DCh Auto Sleep Mode Register (RW)

Bit	D3:D0
Name	AST[3:0]-

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Default	1111		
Bit	D7	D6	D5:D4
Name	ASEN	-	BLMA[1:0]
Default	0	0	00

## ASEN Auto-SLEEP Enable

0	Disable
1	Enable

## BLMA Baseline moving average

Hardware baseline can be generated by slow moving average setting.

00	32 average
01	64 average
10	128 average
11	256 average

## AST Auto Sleep Time

0000	0.5s
0001	1s
0010	1.5s
0011	2s
0100	2.5s
0101	3s
0110	3.5s
0111	4s
1000	4.5s
1001	5s
1010	6s
1011	7s
1100	8s
1101	9s
1110	10s

## DDh Sleep Mode Control Register (RW)

Bit	D3:D2		D1:D0	
Name	T2[1:0]		T1[1:0]	
Default	00		00	
Bit	D7	D6	D5	D4
Name	-	PW	-	SC
Default	0	0	0	0

## PW Proximity Wakeup

**Disable: wake up>>scan key once>>go to sleep again**

**Enable: wake up>> generates INT signal (optional) >>go to sleep after Auto Sleep Time is expired if no key is detected.**

0	Disable
1	Enable

## SC Sleep Calibration

0	Disable
1	Enable

## T2 Wake Up Period with Key Disable

**Device will be woken up according to the T2 setting by polling the status of Key.**

00	50ms
01	100ms
10	200ms
11	300ms

## T1 Wake Up Period with Key Enable

**Device will be woken up according to the T1 setting to maintain the baseline to prevent the change of environment from stopping Key waking up device.**

00	2s
01	4s
10	8s
11	16s

## DEh~DFh Wake Up Key Select Register (RW)

Bit	D7:D0
Name	WK[7:0]
Default	0000 0000

Bit	D7:D0
Name	WK[15:8]
Default	0000 0000

## WK Wakeup Key Select Setting

0	Disable
1	Enable

## E0h Wake Up Threshold Register (RW)

Bit	D7:D0
Name	WTH[7:0]
Default	0000 1000

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## Wake up threshold range from 0 to 255

### E1h TKIII Sleep Mode CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

#### CCHG Internal Reference Capacitance Select

000	10pF
001	20pF
010	30pF
011	40pF
100	50pF
101	60pF
110	70pF
111	80pF

### E2h TKIII Sleep Mode PUD Register (RW)

Bit	D3:D0		
Name	PUD[3:0]		
Default	0000		
Bit	D7	D6	D5:D4
Name	PUDIEN	PUDREN	-
Default	0	0	00

TK3 PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance caused by a high capacitance key. Connecting a switching current source or resistor can thus maintain touch key detection sensitivity.

For DC current, PUD[3:0] can enable 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] can enable 5K/10K/20K/40K resistor

#### PUDIEN Pull-up/Pull-down DC Current Enable

#### PUDREN Pull-up/Pull-down DC Resistor Enable

#### PUD Pull up DC Current

1000	Enable 8uA current source.
0100	Enable 4uA current source.
0010	Enable 2uA current source.
0001	Enable 1uA current source.

#### PUD Pull up Resistor

1000	Enable 5K resistor source.
0100	Enable 10K resistor source.
0010	Enable 20K resistor source.
0001	Enable 40K resistor source.

### E3h Sleep Mode Raw Count Register 1 (RO)

Bit	D7:D0
Name	SLRC[15:8]
Default	0000 0000

### E4h Sleep Mode Raw Count Register 2 (RO)

Bit	D7:D0
Name	SLRC[7:0]
Default	0000 0000

**SLRC** Sleep Mode Raw Count  
Read only. Value for reference

### E5h Sleep Mode Baseline Register 1 (RO)

Bit	D7:D0
Name	SLB[15:8]
Default	0000 0000

### E6h Sleep Mode Baseline Register 2 (RO)

Bit	D7:D0
Name	SLB[7:0]
Default	0000 0000

**SLB** Sleep Mode Baseline  
Read only. Value for reference

### E7h Slider1 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

**ACT** Slider is active  
0 Disable slider  
1 Enable slider

**INIP** Initial position

### E8h Slider1 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP
Default	0	0000000

**DIR** Direction of Slide1

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- 0 Rotate to left
- 1 Rotate to right

**ENDP** End position of the slider

## E9h Slider1 Status Register 3 (RW)

Bit	D7	D6:D0
Name	STA	DUR
Default	1	0000000

**STA** Status of Slider1

- 0 Wheel
- 1 Slider

STA is the only bit for write.

**DUR** Duration

The duration between initial position to end position. Every DUR bit increase presents 0.1s.

## EAh Slider2 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

**ACT** Slider2 is active

- 0 Disable slider
- 1 Enable slider

**INIP** Initial position

## EBh Slider2 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP
Default	0	0000000

**DIR** Direction of Slide2

- 0 Rotate to left
- 1 Rotate to right

**ENDP** End position of the slider

## ECh Slider2 Status Register 3 (RO)

Bit	D7	D6:D0
Name	STA	DUR
Default	0	0000000

**STA** Status of Slider2

- 0 Wheel
- 1 Slider

**DUR** Duration

The duration between initial position to end position. Every DUR bit increase presents 0.1s.

## EDh Slider1 Map Register 1 (RW)

Bit	D7:D4	D3:D0
Name	S1K1[3:0]	S1K2[3:0]
Default	1000	1001

## EEh Slider1 Map Register 2 (RW)

Bit	D7:D4	D3:D0
Name	S1K3[3:0]	S1K4[3:0]
Default	1010	1011

## EFh Slider1 Map Register 3 (RW)

Bit	D7:D4	D3:D0
Name	S1K5[3:0]	S1K6[3:0]
Default	1100	1101

**S1Kx** Slider1 Keyx Map table  
Slider1 KEYx is mapped to Touch Key S1Kx[3:0]

## F0h Slider2 Map Register 1 (RW)

Bit	D7:D4	D3:D0
Name	S2K1[3:0]	S2K2[3:0]
Default	0000	0000

## F1h Slider2 Map Register 2 (RW)

Bit	D7:D4	D3:D0
Name	S2K3[3:0]	S2K4[3:0]
Default	0000	0000

## F2h Slider2 Map Register 3 (RW)

Bit	D7:D4	D3:D0
Name	S2K5[3:0]	S2K6[3:0]
Default	0000	0000

**S2Kx** Slider2 Keyx Map table  
Slider2 KEYx is mapped to Touch Key S2Kx[3:0]

## F3h – F8h Slider1 Calibration Register 1 - 6 (RW)

Bit	the the D7:D1
Name	S1CRKx[7:0]
Default	0010 1000

**S1CRKx** These registers are used for slider1 calibration. The slider1 is composed of six touch keys. The range of x is from 1 to 6 which means Key1 to Key6.



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## F9h – FEh Slider2 Calibration Register 1 – 6 (RW)

Bit	D7:D1
Name	S2CRKx [7:0]
Default	0010 1000

S2CRKx These registers are used for slider2 calibration. The slider2 is composed of six touch keys. The range of x is from 1 to 6 which means Key1 to Key6.

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## Page 1 Registers (For Expand Memory)

### 100h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0001 0111

#### CPN Chip Part Number

Chip's part number 17h

### 101h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

#### CV1 Chip Version information 1

### 102h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

#### CV2 Chip Version information 2

CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

### 103h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	010	000	00

#### FV Firmware Version

Default version is 2.0.0

FV1[2:0] Major version

FV2[2:0] Minor version

FV3[1:0] Patch version

### 104h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	SR	RD	-	SP	SS	-
Default	0	0	0	0	0	000

#### SR System Reset

1 System reset

#### RD Reset All Parameters to Manufacturer Default Setting.

1 Reset all user-defined parameters to manufacture the default setting.

#### SP Sleep Mode

1 Sleep mode

#### SS Save User Defined Parameters

1 Save current parameters into flash.

### 105h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)

FLAG=1 Page 1 (Address: 0x100~0x1FF)

### 106h~107h Key Status Register 1 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

#### KSx Key0~Key7 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

### Key Status Register 2 (RO)

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

#### KSx Key8~Key15 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

### 108h Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

#### BM Buzzer Register Write

Buzzer data or stop command

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## 108h Buzzer Register (R)

Bit	D7:D0
Name	BM[7:0]
Default	0000 1010

### BM Buzzer Register Read

It shows the available tone buffer size. IS32SE5117 has 10 built-in note buffers.

## 109h GPIO Value Register 1 (R/W)

Bit	D7:D0
Name	GPV [7:0]
Default	0000 1110

## 10Ah GPIO Value Register 2 (R/W)

Bit	D7:D0
Name	GPV [15:8]
Default	0000 0000

### GPV GPIO Value

Define GPIO values.

- 0 GPIO LOW
- 1 GPIO HIGH

Above GPIO pin HIGH or LOW will be set only when the corresponding bits of the register GPIO Pin Select registers (CFh and D0h) are enabled.

## 10Bh GPIO Enable Register 1 (R/W)

Bit	D7:D0
Name	GPE [7:0]
Default	0111 0000

## 10Ch GPIO Enable Register 2 (R/W)

Bit	D7:D0
Name	GPE [15:8]
Default	0000 0000

### GPE GPIO Enable

- 0 Disable GPIO function
- 1 Enable GPIO function

## 10Dh GPIO Map Register 1 (R/W)

Bit	D7:D4	D3:D0
Name	GM1[3:0]	GM0[3:0]
Default	0000	0000

## 10Eh GPIO Map Register 2 (R/W)

Bit	D7:D4	D3:D0
-----	-------	-------

Name	GM3[3:0]	GM2[3:0]
Default	0000	0000

## 10Fh GPIO Map Register 3 (R/W)

Bit	D7:D4	D3:D0
Name	GM5[3:0]	GM4[3:0]
Default	0001	0010

## 110h GPIO Map Register 4 (R/W)

Bit	D7:D4	D3:D0
Name	GM7[3:0]	GM6[3:0]
Default	0000	0011

## 111h GPIO Map Register 5 (R/W)

Bit	D7:D4	D3:D0
Name	GM9[3:0]	GM8[3:0]
Default	0000	0000

## 112h GPIO Map Register 6 (R/W)

Bit	D7:D4	D3:D0
Name	GM11[3:0]	GM10[3:0]
Default	0000	0000

## 113h GPIO Map Register 7 (R/W)

Bit	D7:D4	D3:D0
Name	GM13[3:0]	GM12[3:0]
Default	0000	0000

## 114h GPIO Map Register 8 (R/W)

Bit	D7:D4	D3:D0
Name	GM15[3:0]	GM14[3:0]
Default	0000	0000

**GMx [3:0]** Map touch key x to which IS32SE5117 pin according to the following table and the value of GMx [3:0].

IS32SE5117 Pin #	GMx [3:0]
P1	0
P2	1
P3	2
P4	3
P9	4
P10	5
P11	6
P12	7
P13	8

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P14	9
P15	10
P16	11
P17	12
P18	13
P19	14
P20	15

## 115h GPIO Toggle Enable Register 1 (R/W)

Bit	D7:D0
Name	TOEN [7:0]
Default	0001 0000

## 116h GPIO Toggle Enable Register 2 (R/W)

Bit	D7:D0
Name	TOEN [15:8]
Default	0000 0000

### TOENx Enable GPIO Toggle Mode

- 0 Disable Touch Key channel to enter GPIO Toggle Mode.
- 1 Enable Touch Key channel to enter GPIO Toggle Mode.

## 117h Key Scan Once Register (RW)

Bit	D7:D2	D1	D0
Name	-	TR	EN
Default	0000	00	00

### TR

- Write 1 Trigger one scan
- Read 1 Busy
- Read 0 Data ready

### EN Enable Key Scan Once

- 0 Continuous scan of all enabled keys
- 1 Scan all enabled keys once

## 118h Table Ready Mark Register (RO)

Bit	D7:D0
Name	MARK[7:0]
Default	0000 0000

### MARK

This register is used by firmware to indicate parameters are correctly programmed.

Ready/Fail status

- 00 ready
- Others not ready

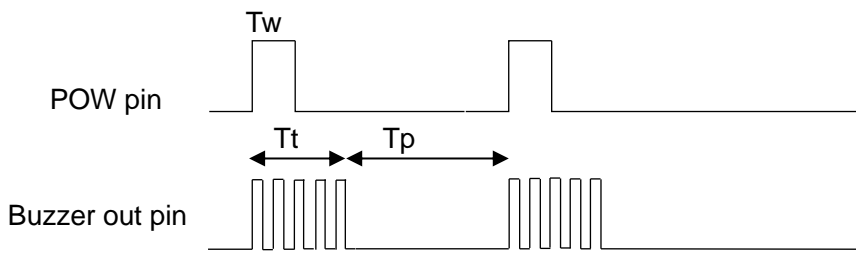
# IS32SE5117

## BUZZER / MELODY APPLICATION

### F0h Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

1st byte	2nd byte	3rd byte	4th byte
Scale ID	Tt	Tw	Tp



**Tt, Tw and Tp range from 0 to 255 @ 4ms step**

A Tone played duration is defined as Tt + Tp.

The support scale is from 3A to 8G#.

Frequencies for equal-tempered scale, A4 = 440 Hz "Middle C" is C4												
	3	freq	divisor	freq error	4	freq	divisor	freq error	5	freq	divisor	freq error
C					3	261.6	1911	0.01%	15	523.3	956	-0.05%
C#					4	277.2	1804	-0.01%	16	554.4	902	-0.01%
D					5	293.7	1703	-0.02%	17	587.3	851	0.04%
D#					6	311.1	1607	0.00%	18	622.3	804	-0.06%
E					7	329.6	1517	-0.01%	19	659.3	758	0.06%
F					8	349.2	1432	-0.02%	20	698.5	716	-0.02%
F#					9	370.0	1351	0.03%	21	740.0	676	-0.05%
G					10	392.0	1276	-0.04%	22	784.0	638	-0.04%
G#					11	415.3	1204	-0.01%	23	830.6	602	-0.01%
A	0	220.0	2273	-0.01%	12	440.0	1136	0.03%	24	880.0	568	0.03%
A#	1	233.1	2145	0.01%	13	466.2	1073	-0.04%	25	932.3	536	0.05%
B	2	246.9	2025	-0.01%	14	493.9	1012	0.04%	26	987.8	506	0.04%

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	6	freq	divisor	freq error	7	freq	divisor	freq error	8	freq	divisor	freq error
C	27	1046.5	478	-0.05%	39	2093.0	239	-0.05%	51	4186.0	119	0.37%
C#	28	1108.7	451	-0.01%	40	2217.5	225	0.21%	52	4434.9	113	-0.23%
D	29	1174.7	426	-0.08%	41	2349.3	213	-0.08%	53	4698.6	106	0.39%
D#	30	1244.5	402	-0.06%	42	2489.0	201	-0.06%	54	4978.0	100	0.44%
E	31	1318.5	379	0.06%	43	2637.0	190	-0.21%	55	5274.0	95	-0.21%
F	32	1396.9	358	-0.02%	44	2793.8	179	-0.02%	56	5587.7	89	0.54%
F#	33	1480.0	338	-0.05%	45	2960.0	169	-0.05%	57	5919.9	84	0.55%
G	34	1568.0	319	-0.04%	46	3136.0	159	0.28%	58	6271.9	80	-0.35%
G#	35	1661.2	301	-0.01%	47	3322.4	150	0.33%	59	6644.9	75	0.33%
A	36	1760.0	284	0.03%	48	3520.0	142	0.03%				
A#	37	1864.7	268	0.05%	49	3729.3	134	0.05%				
B	38	1975.5	253	0.04%	50	3951.1	127	-0.36%				

Scale ID(Sid): 0 is 3A, 1 is 3A#, 2 is 3B ....

## 08h Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

Clear Melody buffer and stop play.

## 08h Buzzer/Melody Register (R)

Bit	D7:D0
Name	BM
Default	0000 1010

**BM Buzzer/Melody Register Read. It shows the available tone buffer size. IS32SE5117 has 10 built-in note buffers.**

I2C command format - Each note is composed of 4-byte data, and the incomplete note will be ignored. The incoming note data will be ignored if the FIFO is full)

0x78, 0xF0, (Sid, Tt, Tw, Tp), (Sid, Tt, Tw, Tp), ....

0x78, 0xF0, 0xFF stop the melody play and clear the FIFO

0x78, 0xF0 Set the register number to 0xF0

0x79 Read FIFO remaining length

Reference schematic and tone waveform are introduced as follows:

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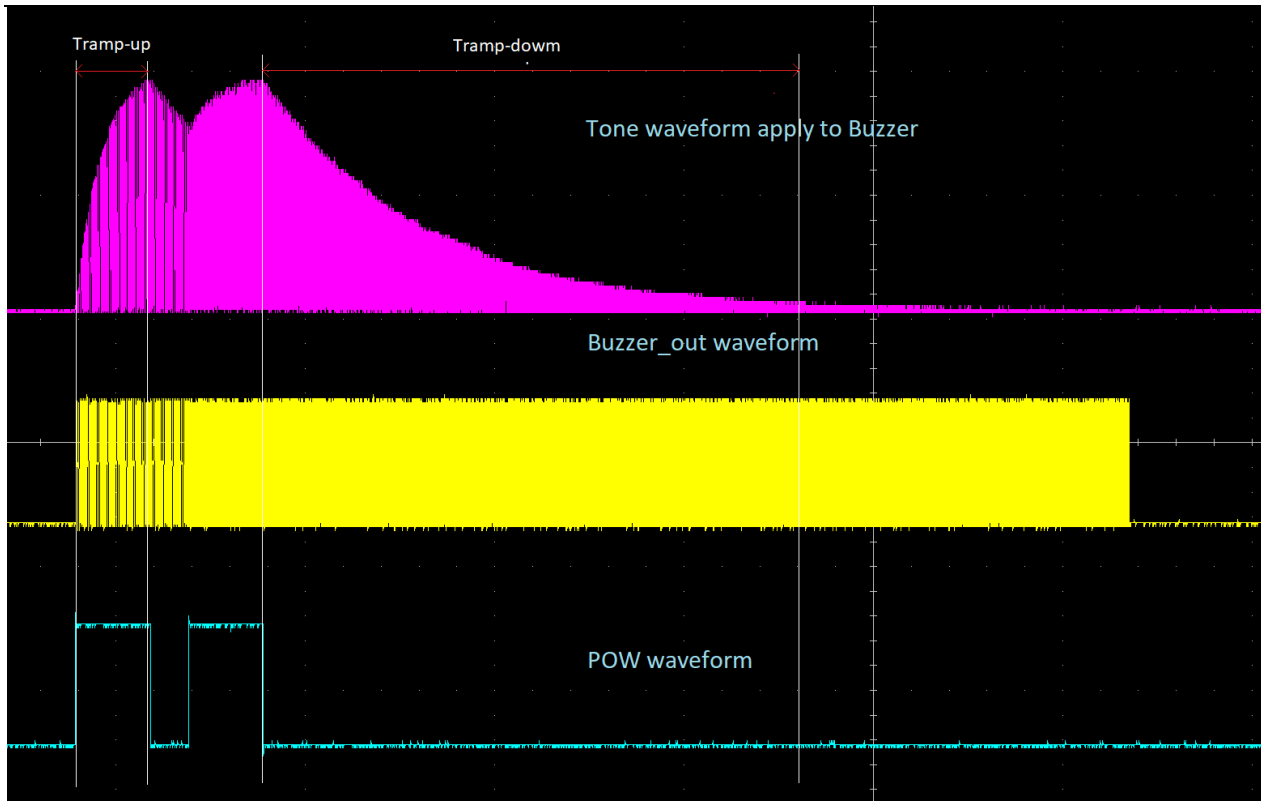


Figure 10: Buzzer/ Melody waveform example

**Note:**

$T_{\text{ramp-up}}$  :  $100R$  as below in figure 11 decides the signal ramp-up rate.

$T_{\text{ramp-down}}$ : The signal ramps down because POW is low and the  $47\mu\text{F}$  capacitor as below in figure 11 decides the ramp-down rate.

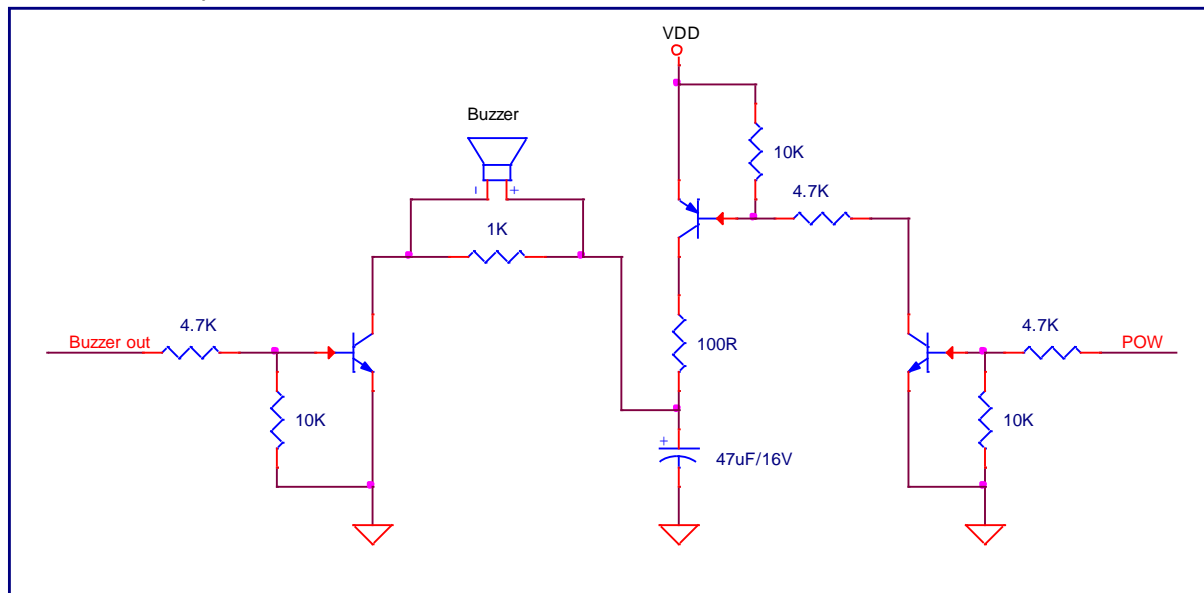


Figure 11: Typical application circuit for Melody

**CBh Buzzer Pin Select Register 1**

Bit	D7:D0
Name	BPS1[7:0]

Default	---- -- 1
---------	-----------

**CCh Buzzer Pin Select Register 2**

Bit	D0
-----	----

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Name	BPS2[7:0]
Default	-----

## BPS1/2 Buzzer output Select 1/2

Enable BPS1[0] will set Pin1 as Buzzer output pin.

BPS1[7:1] & BPS2[7:0] unused register bits.

## CDh Enable Buzzer Power Register 1

Bit	D7:D0
Name	EBP1[7:0]
Default	-----

## CEh Enable Buzzer Power Register 2

Bit	D7:D0
Name	EBP2[7:0]
Default	--- 1 ----

## EBP1/2 Buzzer Power Select 1/2

EBP1[7:0] unused register.

EBP2[4] maps to KEY12, write 1 will enable KEY12 as Buzzer Power. Setting other EBP2 bits doesn't work.



# IS32SE5117

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## TYPICAL APPLICATION INFORMATION

The IS32SE5117 is an ultra-low-power, fully integrated 16-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric material such as glass or plastic.

## SENSITIVITY ADJUSTING

Sensitivity can be adjusted by the external capacitor or internal register.

A higher capacitor value will yield lower detection sensitivity. A lower capacitor value will yield higher detection sensitivity.

## INTERRUPT

Touch key detection event will trigger INTB pin. The INTB pin will be driven low when the selected channel is pressed or released.

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## CLASSIFICATION REFLOW PROFILE

Profile Feature	Pb-Free Assembly
<b>Preheat &amp; Soak</b>	
Temperature min (T <sub>smin</sub> )	150°C
Temperature max (T <sub>smax</sub> )	200°C
Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> )	217°C
Time at liquidous (t <sub>L</sub> )	60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak	8 minutes max.

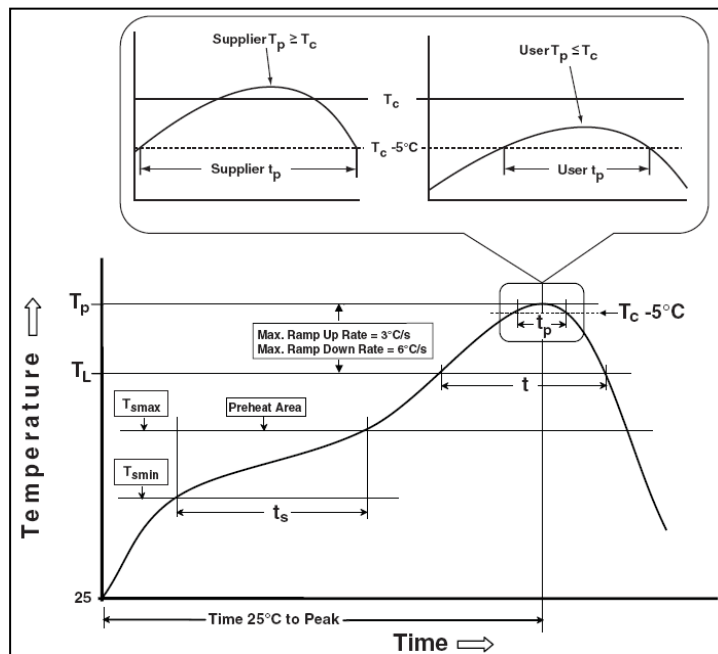
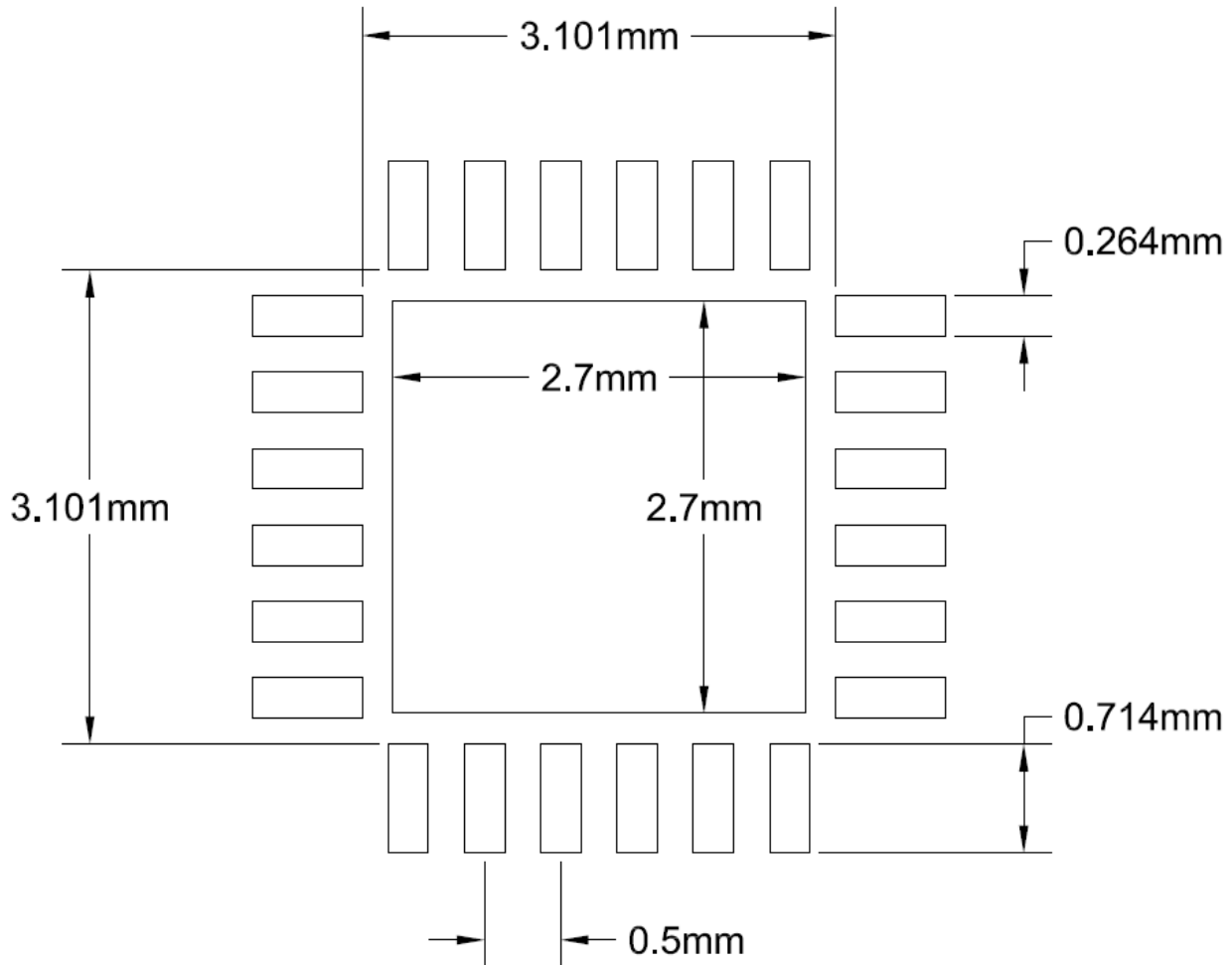


Figure 12: Classification Profile

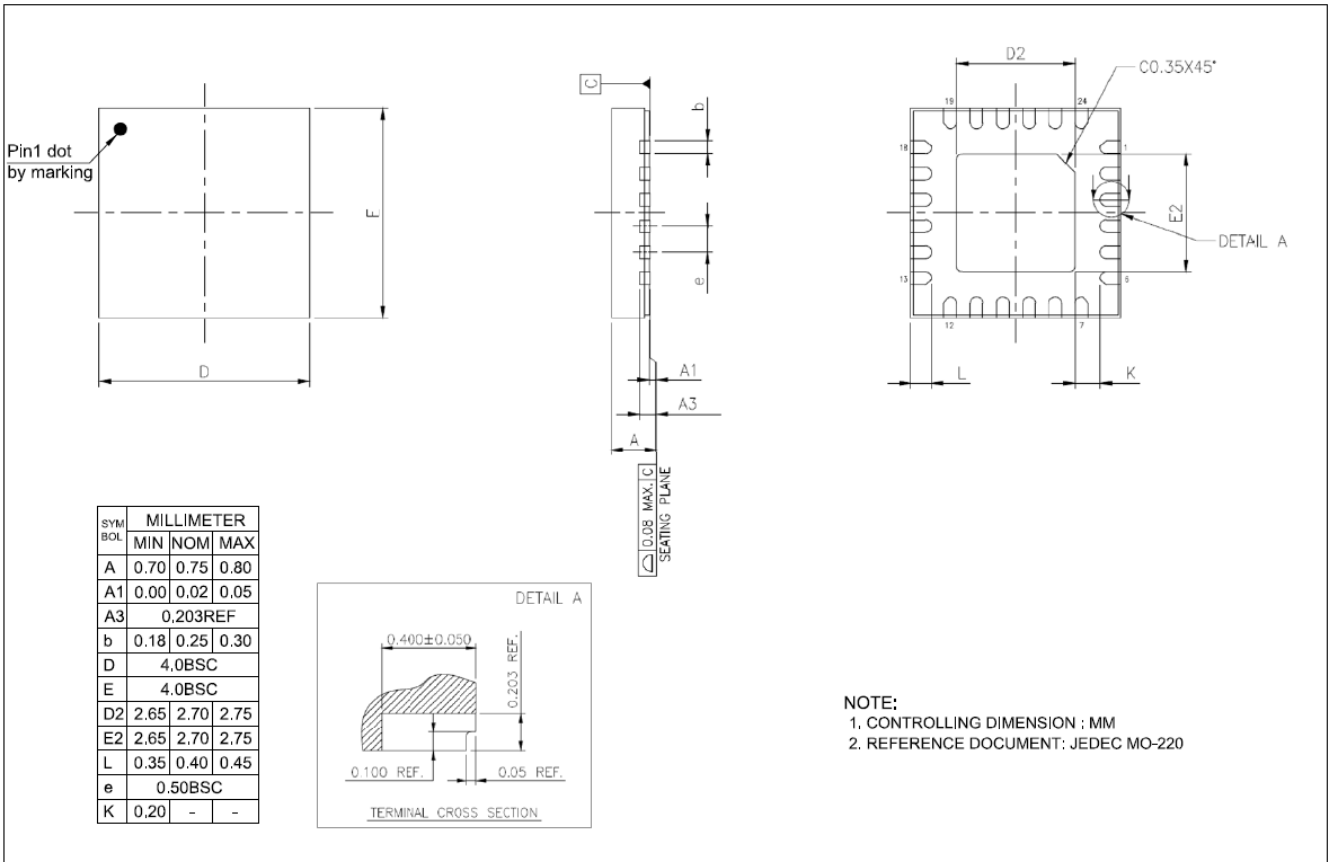
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## PACKAGE INFORMATION WETTABLE FLANK WQFN-24 RECOMMENDED LAND PATTERN



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## POD



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## REVISIONS

Revision	Detailed Information	Date
A	First formal release	2021.06.08
B	<ol style="list-style-type: none"> <li>1. Remove SE5117 GUI 1.0 introduction (Separate SE5117 EvB user manual for GUI)</li> <li>2. Add detailed descriptions for SE5117 functions and registers</li> <li>3. Update T<sub>ja</sub> 29 deg C/W for SE5117</li> <li>4. Update default register values</li> <li>5. Add ROHS compliant</li> </ol>	2022.02.08
C	<ol style="list-style-type: none"> <li>1. Revise VCC to VDD in <a href="#">ABSOLUTE MAXIMUM RATINGS</a> &amp; <a href="#">ELECTRICAL CHARACTERISTICS</a></li> <li>2. Update land pattern and POD information for IS32SE5117 24 WQFN-package</li> </ol>	2022.07.05
D	<ol style="list-style-type: none"> <li>1. Support proximity sensing</li> <li>2. Add “Halogen-Free compliant” claim in product features</li> <li>3. Add GPIO DC Characteristics in Section <a href="#">DC ELECTRICAL CHARACTERISTICS</a></li> <li>4. Add detailed definitions for 010Bh GPIO Enable 1 &amp; 010Ch GPIO Enable 2 in page 1 register list table and clear description for GMx [3:0] for touch key to GPIO function</li> <li>5. Add detailed information for registers CFh ~ D0h <b>GPIO Pin Select</b> and registers 109h <b>GPIO value 1</b> &amp; 10Ah <b>GPIO value 2</b></li> </ol>	2022.12.12
E	<ol style="list-style-type: none"> <li>1. Modify SE5117 I2C speed from 400kHz to 100kHz</li> <li>2. Reword some content for clearer descriptions</li> <li>3. Add “TSCA compliance” support</li> <li>4. Add baseline update description for Figure 4: Baseline Process based on the difference between baseline and raw count in <a href="#">Section Function Block Diagram</a></li> </ol>	2023.07.26