ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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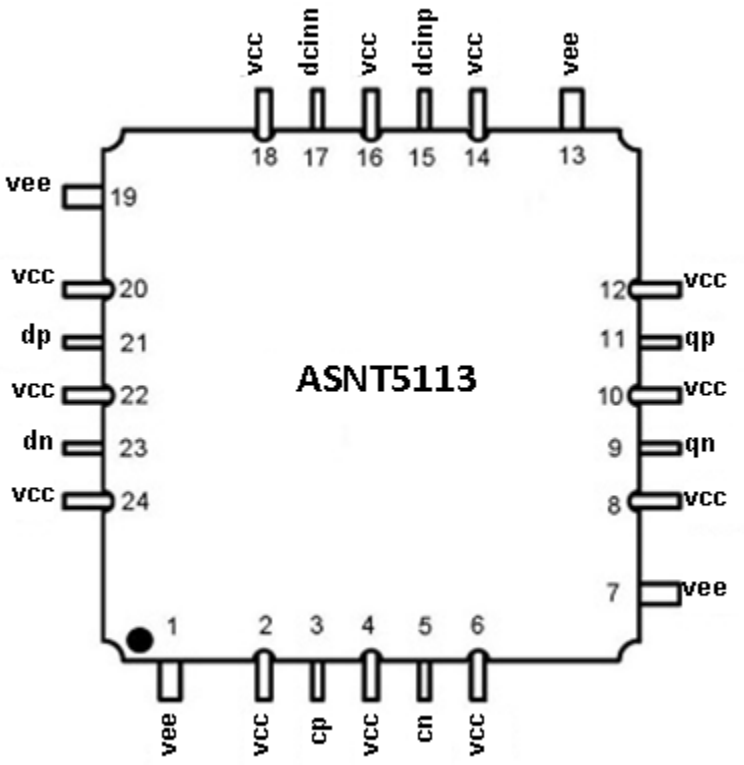
ASNT5113-KMC
DC-32*Gbps* High Sensitivity D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Additional input buffer / level shifter for improved protection
- Sensitive input data buffer with increased CM range that is ideal for sampling applications
- Input data single-ended common mode controls
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 4*ps* set-up/hold time capability
- 88% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 510*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

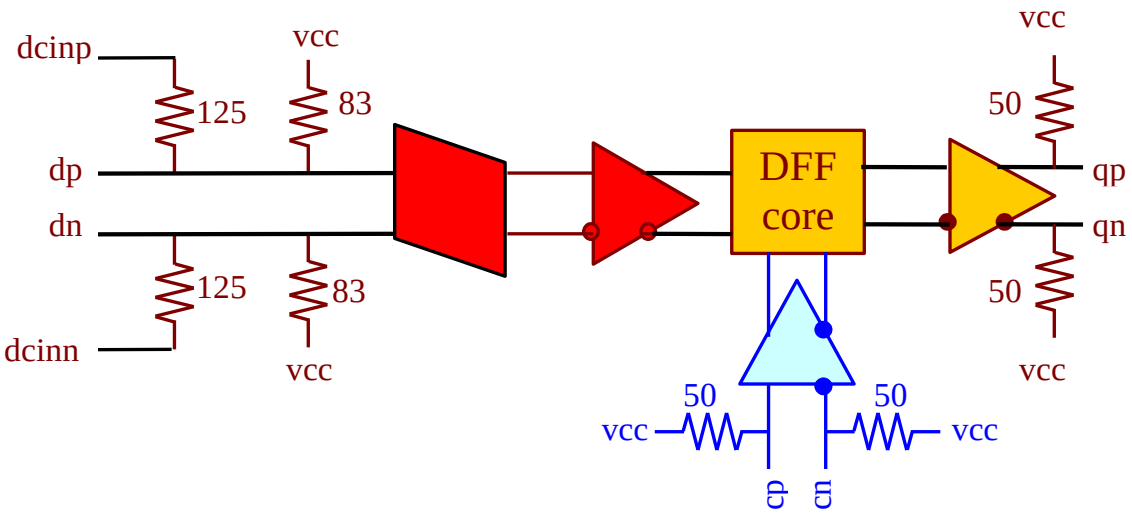

Fig. 1. Functional Block Diagram

The temperature stable ASNT5113-KMC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal dp/dn with a full-rate external clock cp/cn to create a full-rate retimed NRZ data output qp/qn.

The data input buffer is designed to have increased input signal sensitivity, and is able to operate over a wider range of input common mode (CM) voltages. The actual common mode voltage levels at data inputs dp/dn can be adjusted by applying voltages between vee and vcc to the corresponding control inputs dcinp/dcinn. The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

It should be noted that the control inputs dcinp/dcinn should be always connected to voltage sources to ensure correct 50*Ohm* terminations for the data inputs.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.56	*W*
Input Data Voltage Swing (SE)		1.7	*V*
Input Clk Voltage Swing (SE)		1.7	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	21	CML Input	Differential data inputs with internal SE 50*Ohm* termination to vcc
dn	23		
cp	3	CML Input	Differential clock inputs with internal SE 50*Ohm* termination to vcc
cn	5		
qp	11	CML Output	Differential data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
qn	9		
DC Controls			
dcinp	15	Input	Input data DC common mode voltage level controls. **Should be always connected to voltage sources!**
dcinn	17		
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply (+3.3*V* or 0*V*)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)		1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc		0.0		*V*	External ground
vee	-3.1	-3.3	-3.5	*V*	±6%
*I*vcc		155	165	*mA*	
Power consumption		510	545	*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Data rate	DC	32	40	*Gbps*	
Swing	0.01		1.3	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.7+sw/2		vcc+0.6-sw/2	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC	32	40	*GHz*	
Swing	0.05		1.3	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.7+sw/2		vcc+0.6-sw/2	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
Clock Phase Margin	86	88	90	*%*	For reliable data latching at full rate
Setup/Hold Times		2.75/1.0		*ps*	For reliable data latching
HS Output Data (qp/qn)					
Data rate	DC	32	40	*Gbps*	
Logic “1” level	vcc-0.05	vcc-0.03	vcc-0.01	*V*	
Logic “0” level	vcc-0.46	vcc-0.44	vcc-0.42	*V*	With external 50*Ohm* DC termination
Jitter		0.15		*ps*	Peak-to-peak at 32*Gbps*
DC Input Controls (dcinp/dcinn)					
Max level		vcc + 1.0		*V*	
Min level		vcc - 1.0		*V*	

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part’s identification label is ASNT5113-KMC. The first 8 characters of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the underscore represent the package’s manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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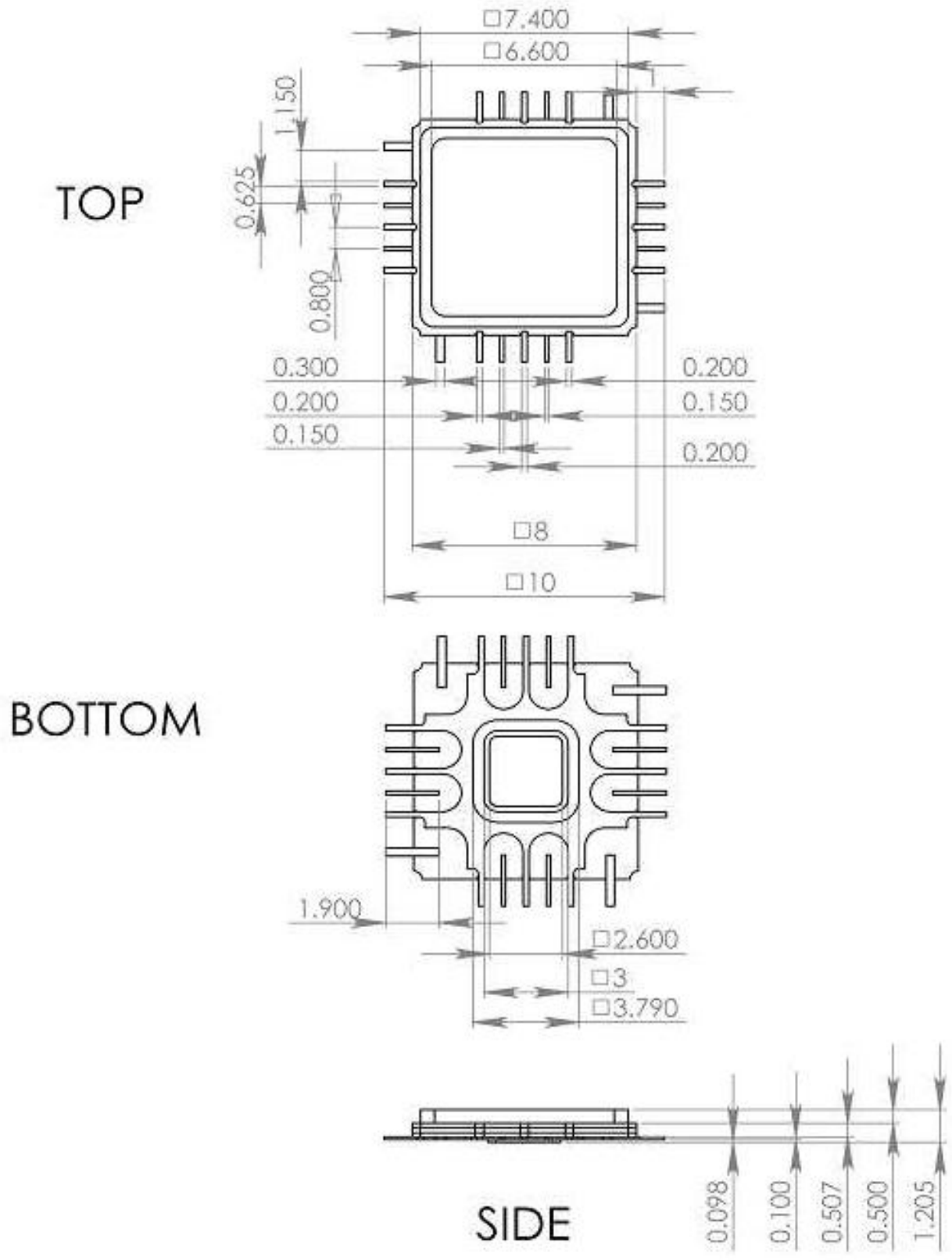

Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.4.2	02-2020	Updated Package Information
1.3.2	07-2019	Updated Letterhead
1.3.1	07-2015	Revised package information section
1.2.1	07-2015	Inserted setup and hold times (identical to clock phase margin)
1.1.1	06-2013	Corrected pin out diagram Removed data duty cycle specification
1.0.1	02-2013	First release