S1D13742

S1D13742 VGA LCD Controller

The S1D13742 is a VGA color LCD graphics controller with an embedded 768 KB display buffer. The S1D13742 supports a 8/16-bit Intel 80 CPU architecture while providing high performance bandwidth into display memory allowing for fast screen updates.

Products requiring a rotated display image can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. Resolutions supported include 800x480 single buffered and 352x416 double buffered.

The S1D13742 uses a double-buffer architecture to prevent any visual tearing during streaming video screen updates. These features combined with the low cost, low power design of the S1D13742, provide an ideal display solution for a wide variety of applications within embedded markets.

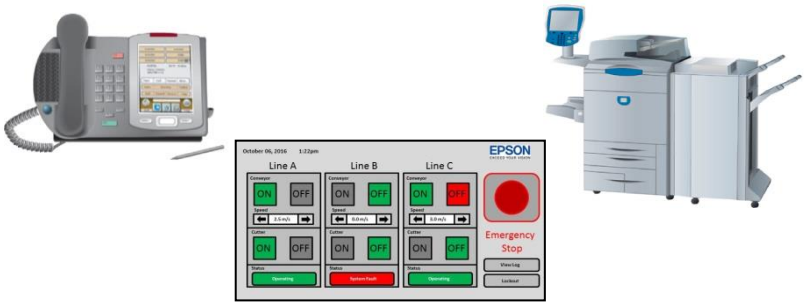
FEATURES

- Embedded 768 KB SRAM display buffer
- Low operating voltage
- 8/16-bit Intel 80 interface (used for display or register data)
- Input data formats:
  - RGB: 8:8:8, 6:6:6, 5:6:5
  - YUV 4:2:2, 4:2:0
- Supports TFT panels
- 18/36-bit RGB interface
- Supports resolutions up to 800x480
- Hardware / software power save mode
- 16/18 bpp color depths
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image
- Double-buffer available to prevent image tearing during streaming input
- Pixel doubling: horizontal and vertical averaging for smooth doubling of a single window
- Pixel halving: no limitation on number of windows
- Internal programmable PLL
- Single MHz clock input: CLKI
- General purpose input/output pins

SYSTEM BLOCK DIAGRAM

S1D13742 Features

- 768 KB SRAM
- Double Buffer support
- Pixel doubling
- Pixel halving
- Swivelview™ Rotation



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DESCRIPTION

Display Buffer

- 768 KB of embedded SRAM

Panel Support

- Supports TFT panels
- 18/36-bit interface
- Supports resolutions up to 800x480

Input Data Formats

- RGB: 8:8:8, 6:6:6, 5:6:5 (8:8:8 will be truncated to 16 or 18 bpp)
- YUV 4:2:2, 4:2:0 (internal YUV to RGB converter stored as 16 or 18 bpp)

Miscellaneous

- Internal programmable PLL
- Single MHz clock input: CLKI
- CLKI available as CLKOUT (separate CLKOUTEN pin associated with output)
- Hardware/software power save mode
- Input pin to enable/disable power save mode
- General purpose input/output pins are available (GPIO[7:0])
- COREVDD 1.5 volts and IOVDD 1.65 ~ 3.6 volts
- QFP20 144-pin package

CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data)
- Chip select used to select device, when inactive,any input data/command is ignored

Display Features

- 16/18 bpp color depths
- All display writes are handled by window apertures/position (for complete or partial display updates). All window coordinates are referenced to top left corner of the displayed image (even in a rotated display, the top-left corner is maintained and no host side translation need take place)
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image. All displayed windows can have independent rotation. No additional programming necessary when enabling these modes.
- Double-buffer available to prevent image tearing during streaming input. Resolutions supported must fit inside 384KB (1/2 of total available display buffer). Typical resolution of 352x416.
- Pixel doubling: horizontal and vertical averaging for smooth doubling of a single window
- Pixel halving: no limitation on number of windows

For more information on the S1D13742 and other Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html

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