LM4869 Boomer® Audio Power Amplifier Series 1.9W Differential Input, BTL Output Stereo Audio Amplifier with Selectable Gain and Shutdown

Check for Samples: LM4869

FEATURES

- **Fully Differential Input and Output**
- **Internal Gain set: 6dB, 10dB, 15.6dB, and 21.6dB**
- **Improved "Click and Pop" Suppression**
- **Thermal Shutdown Protection Circuit**
- **Ultra Low Current Micropower Shutdown Mode**
- **2.0V to 5.5V Operation**
- **Available in Space-Saving Exposed-DAP TSSOP Package**

APPLICATIONS

- **Notebook Computers**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **BTL Output Power**
  - **R_L = 4Ω, V_{DD} = 5.0V, and THD+N = 1%: 1.9W (typ)**
- **BTL Output Power**
  - **R_L = 8Ω, V_{DD} = 5.0V, and THD+N = 1%: 1.2W (typ)**
- **Micropower Shutdown Current: 0.1µA (typ)**
- **PSRR (at 1kHz, V_{DD} = 5V, Figure 1): 62dB (typ)**

DESCRIPTION

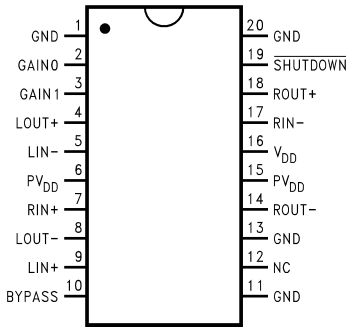
The LM4869 features differential stereo inputs, BTL (bridge-tied load) outputs, and four externally selectable fixed gains. Operating on a single 5V supply, the LM4869 delivers 1.2W and 1.9W (typ) of output power to an 8Ω and 4Ω BTL load (1), respectively, with less than 1% THD+N. The LM4869's gain is selected using two digital inputs. The nominal gain values are 6dB, 10dB, 15.6dB, and 21.6dB.

The LM4869 is designed for notebook and other handheld portable applications. It delivers high quality output power from a surface-mount package and requires few external components.

Other features include an active-low micropower shutdown mode input and thermal shutdown protection.

(1) An LM4869MH that has been properly mounted to a circuit board with a copper heatsink area of at least 2in^2 will deliver 1.9W into 4Ω.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Exposed-DAP TSSOP (Top View)
See Package Number PWP

Typical Application

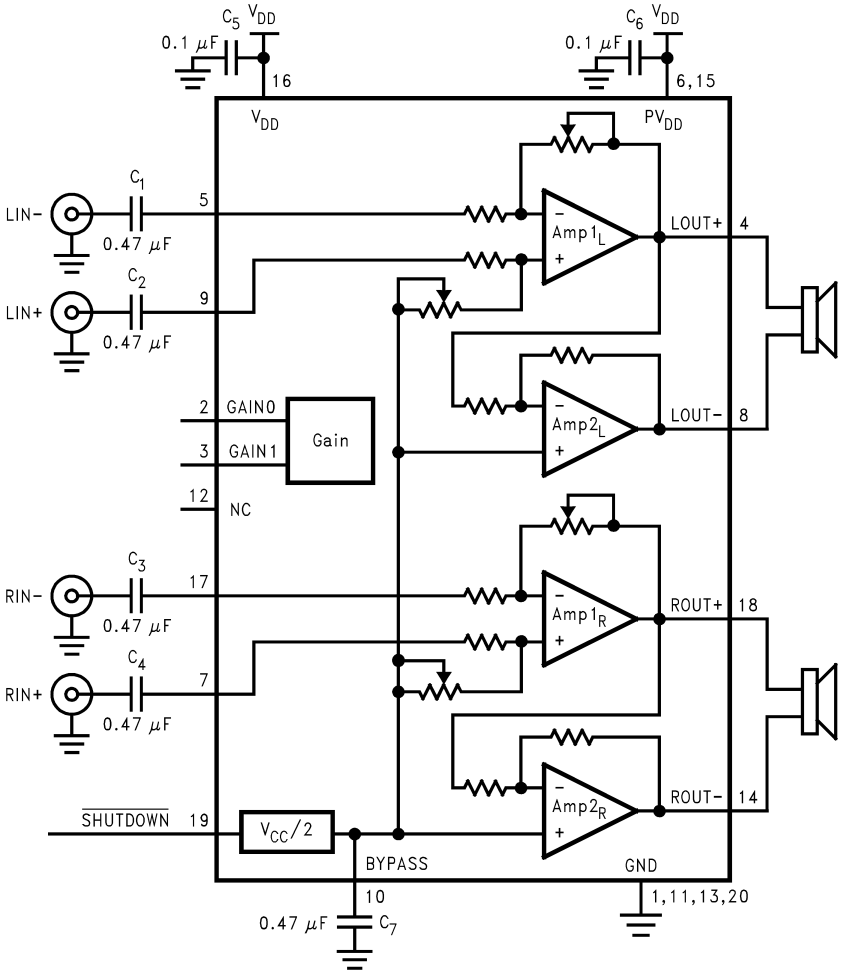


Figure 1. Typical Audio Amplifier Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage		6.0V
Storage Temperature		-65°C to + 150°C
Input Voltage		−0.3V to V_{DD} + 0.3V
Power Dissipation(4)		Internally Limited
ESD Susceptibility(5)		2000V
ESD Susceptibility(6)		200V
Junction Temperature		150°C
Soldering Information Small Outline Package	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JC} (typ) PWP	2°C/W
	θ_{JA} (typ) PWP	47°C/W(7)
	θ_{JA} (typ) PWP	27°C/W(8)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by TJMAX, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4869, see power derating currents for more information.
(5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(6) Machine Model, 220pF-240pF discharged through all pins.
(7) The given θ_{JA} is for an LM4869 packaged in an PWP with the exposed-DAP soldered to an exposed $4in^2$ area of 1oz printed circuit board copper. When driving 4Ω loads from a 5V supply, the LM4869MH must be mounted to the circuit board and its exposed-DAP soldered to an exposed $2in^2$ area of 1oz PCB copper.
(8) The given $\theta_{JA}$is for an LM4869 packaged in an PWP with the exposed DAP soldered to an exposed $8in^2$ area of 1oz printed circuit board (PCB) copper and two $8in^2$ inner layer ground planes in a four-layer PCB.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ TA ≤ 85°C
Supply Voltage		2.0 V ≤ V_{DD} ≤ 5.5V

Electrical Characteristics for LM4869[1][2]

The following specifications applies to the LM4869 when used in the circuit shown in Figure 1 and operating with V_{DD} = 5V and A_V = 6dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4869		Units (Limits)
			Typical[2]	Limit[3][4]	
V_{DD}	Supply Voltage			2 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞	9.0	12.0	mA (max)
I_{SD}	Shutdown Current	$V_{shutdown}$ = GND	0.1	1.0	µA (max)
V_{OS}	Output Offset Voltage		7	50	mV (max)
PSRR	Output Supply Rejection Ratio	V_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P} sinewave, C_{BYPASS} = 0.47µF, R_L = 8Ω	62		dB
P_O	Output Power ([5])	THD+N = 1% (max), f = 1kHz ([6]) R_L = 4Ω R_L = 8Ω	 1.9 1.2	 1.0	 W W (min)
		THD+N = 10% (max), f = 1kHz ([6]) R_L = 4Ω R_L = 8Ω	 2.6 1.5		 W W
THD+N	Total Harmonic Distortion + Noise	20Hz ≤ f ≤ 20kHz R_L = 4Ω, P_O = 2W R_L = 8Ω, P_O = 1W	 0.3 0.3		 % %
S/N	Signal-to-Noise Ratio	f = 1kHz, C_{BYPASS} = 0.47µF, P_O = 1.1W, R_L = 8Ω	97		dB
R_{IN}	Input Resistance	Pins 5, 7, 9, and 17	25	20	kΩ (min)
ΔA_V	Gain Accuracy	R_L = 8Ω			
		Logic Low Applied to Pin 2 Logic Low Applied to Pin 3	6	5.70 6.30	dB (min) dB (max)
		Logic Low Applied to Pin 2 Logic High Applied to Pin 3	10	9.65 10.35	dB (min) dB (max)
		Logic High Applied to Pin 2 Logic Low Applied to Pin 3	15.6	15.25 15.95	dB (min) dB (max)
		Logic High Applied to Pin 2 Logic High Applied to Pin 3	21.6	21.25 21.95	dB (min) dB (max)
$\Delta A_{V\ CH-CH}$	Channel-to-Channel Gain Mismatch	R_L = 8Ω			
		Logic Low Applied to Pin 2 Logic Low Applied to Pin 3	0.12	0.3	dB (max)
		Logic Low Applied to Pin 2 Logic High Applied to Pin 3	0.12	0.3	dB (max)
		Logic High Applied to Pin 2 Logic Low Applied to Pin 3	0.12	0.3	dB (max)
		Logic High Applied to Pin 2 Logic High Applied to Pin 3	0.12	0.3	dB (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Typicals are measured at 25°C and represent the parametric norm.
(3) Limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(4) Datasheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.
(5) Output power is measured at the amplifier's package pins.
(6) When driving 4Ω loads and operating on a 5V supply, the LM4869MH must be mounted to a circuit board that has a minimum of 2.5in^2 of exposed, uninterrupted copper area connected to the LLP package's exposed DAP.

External Components Description

(Refer to Figure 1.)

Components		Functional Description
1.	C_i	The input coupling capacitor blocks DC voltage at the amplifier's inverting input terminals. C_i, along with the LM4869's fixed input resistance R_i (25kΩ, typ), creates a highpass filter with $f_C = 1/(2\pi R_i C_i)$. Both inverting and noninverting inputs require a C_i. Refer to the Application Information section, **Selecting External Components,** for an explanation of determining the value of C_i.
2.	C_S	The supply bypass capacitor. Refer to the **Power Supply Bypassing** section for information about properly placing, and selecting the value of, this capacitor.
3.	C_B	The capacitor, C_B, filters the half-supply voltage present on the BYPASS pin. Refer to the Application Information section, **Selecting External Components,** for information concerning proper placement and selecting C_B's value.

Typical Performance Characteristics
MH Specific Characteristics

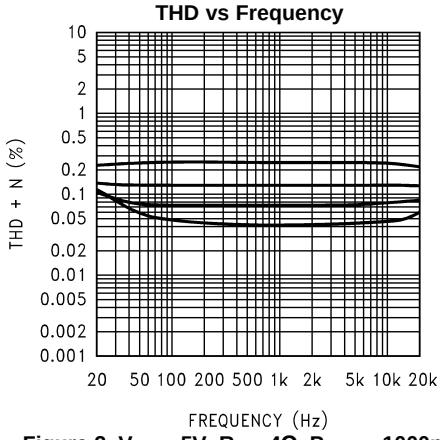


Figure 2. V_{DD} = 5V, R_L = 4Ω, P_{OUT} = 1000mW, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

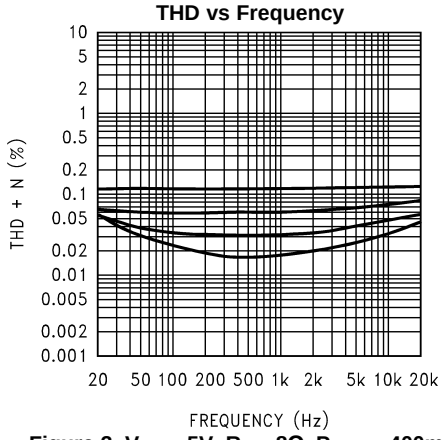


Figure 3. V_{DD} = 5V, R_L = 8Ω, P_{OUT} = 400mW, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

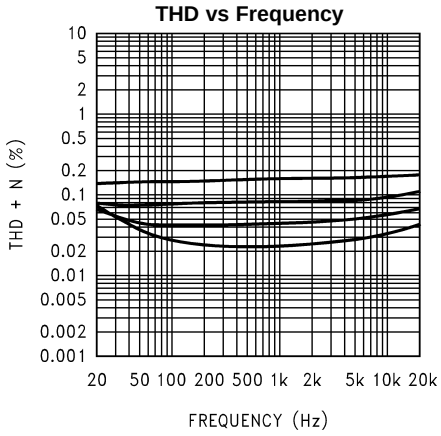


Figure 4. V_{DD} = 5V, R_L = 8Ω, P_{OUT} = 400mW, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

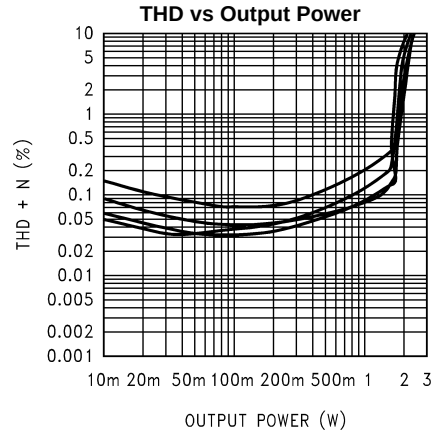


Figure 5. V_{DD} = 5V, R_L = 4Ω, f_{IN} = 20Hz, at (from top to bottom at 100mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 6dB, A_V = 10dB

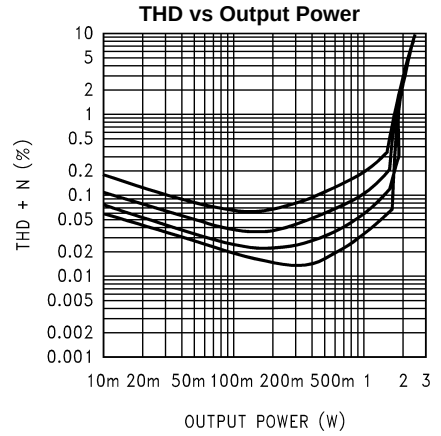


Figure 6. V_{DD} = 5V, R_L = 4Ω, f_{IN} = 1kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

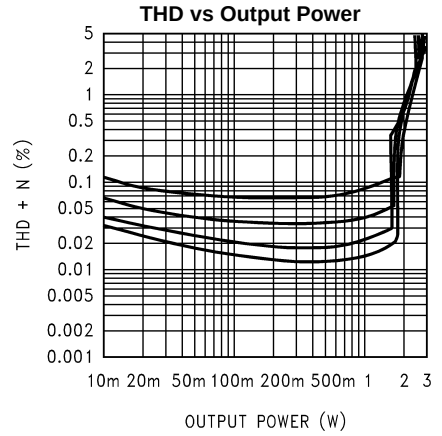


Figure 7. V_{DD} = 5V, R_L = 4Ω, f_{IN} = 20kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

Typical Performance Characteristics
MH Specific Characteristics (continued)

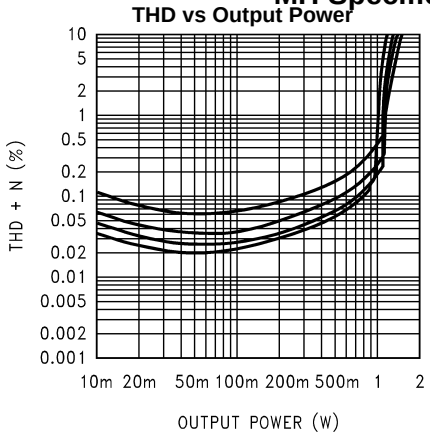


Figure 8. V_{DD} = 5V, R_L = 8Ω, f_{IN} = 20Hz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

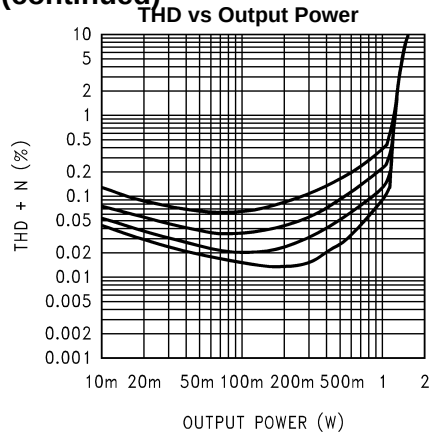


Figure 9. V_{DD} = 5V, R_L = 8Ω, f_{IN} = 1kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

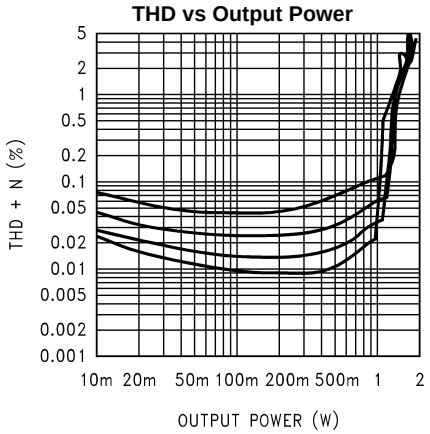


Figure 10. V_{DD} = 5V, R_L = 8Ω, f_{IN} = 20kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

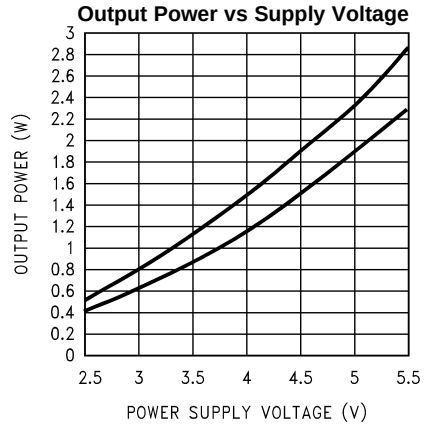


Figure 11. R_L = 4Ω, f_{IN} = 1kHz, at (from top to bottom at 4V): THD+N = 10%, THD+N = 1%

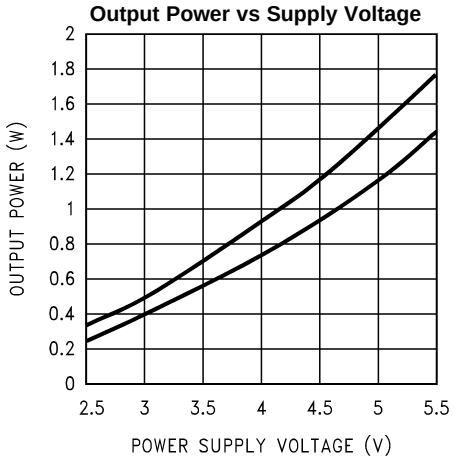


Figure 12. R_L = 8Ω, f_{IN} = 1kHz, at (from top to bottom at 4V): THD+N = 10%, THD+N = 1%

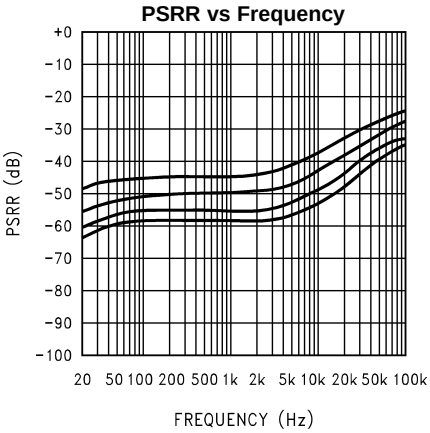


Figure 13. V_{DD} = 5V, R_L = 4Ω, R_{SOURCE} = 10Ω V_{RIPPLE} = 200mV_{P-P}, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

Typical Performance Characteristics
MH Specific Characteristics (continued)

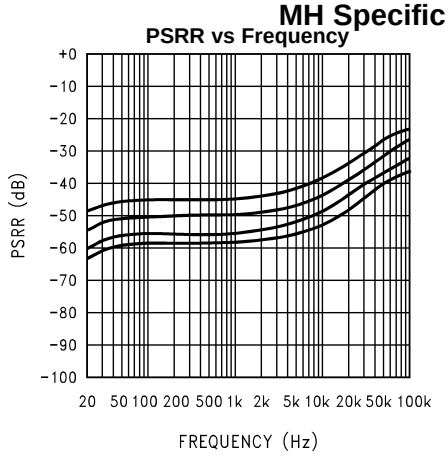


Figure 14. V_{DD} = 5V, R_L = 8Ω, R_{SOURCE} = 10Ω V_{RIPPLE} = 200mV_{P-P}, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

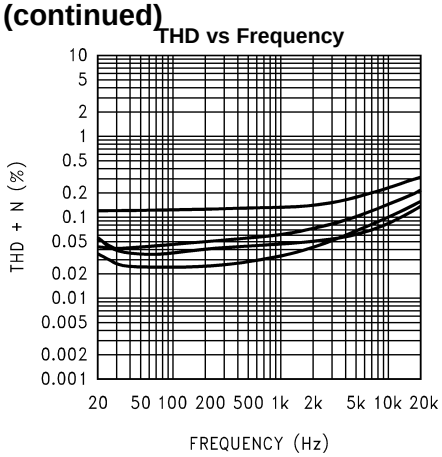


Figure 15. V_{DD} = 3V, R_L = 4Ω, P_{OUT} = 150mW, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

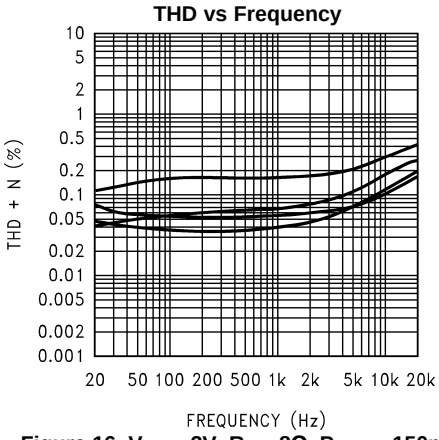


Figure 16. V_{DD} = 3V, R_L = 8Ω, P_{OUT} = 150mW, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

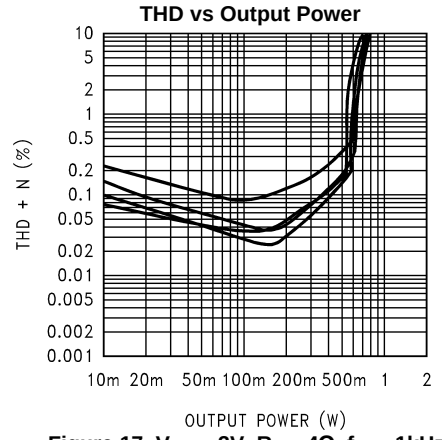


Figure 17. V_{DD} = 3V, R_L = 4Ω, f_{IN} = 1kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 6dB, A_V = 15.6dB, A_V = 10dB

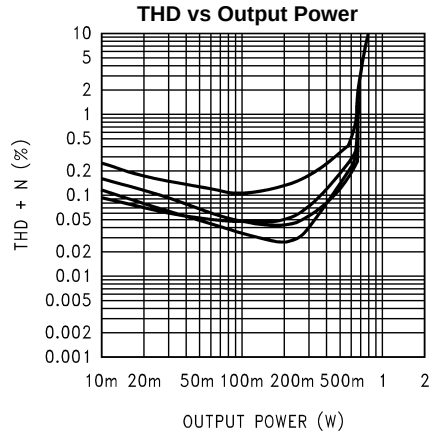


Figure 18. V_{DD} = 3V, R_L = 4Ω, f_{IN} = 20Hz, at (from top to bottom at 100mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 6dB, A_V = 10dB

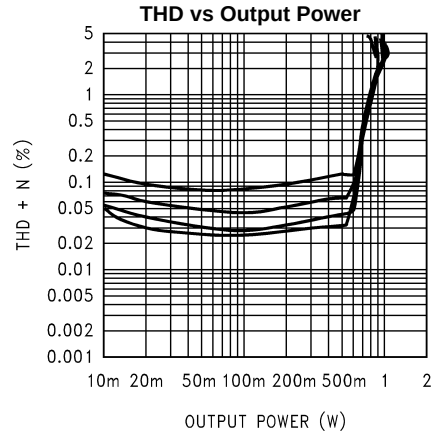


Figure 19. V_{DD} = 3V, R_L = 4Ω, f_{IN} = 20kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

Typical Performance Characteristics
MH Specific Characteristics (continued)

THD vs Output Power

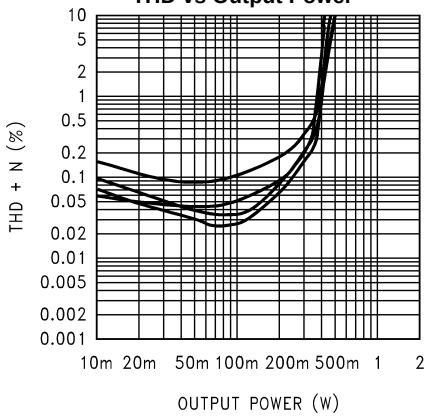


Figure 20. V_{DD} = 3V, R_L = 8Ω, f_{IN} = 20Hz, at (from top to bottom at 100mW): A_V = 21.6dB, A_V = 6dB, A_V = 15.6dB, A_V = 10dB

THD vs Output Power

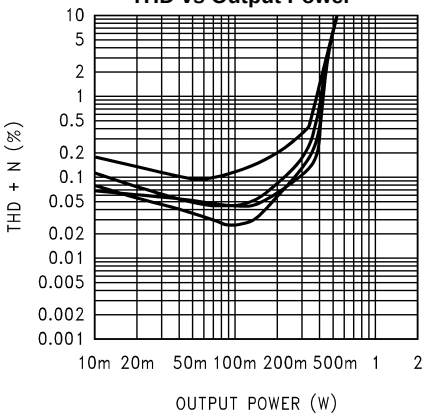


Figure 21. V_{DD} = 3V, R_L = 8Ω, f_{IN} = 1kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 6dB, A_V = 10dB

THD vs Output Power

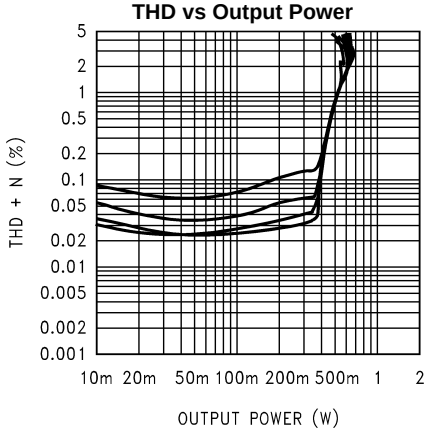


Figure 22. V_{DD} = 3V, R_L = 8Ω, f_{IN} = 20kHz, at (from top to bottom at 200mW): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

PSRR vs Frequency

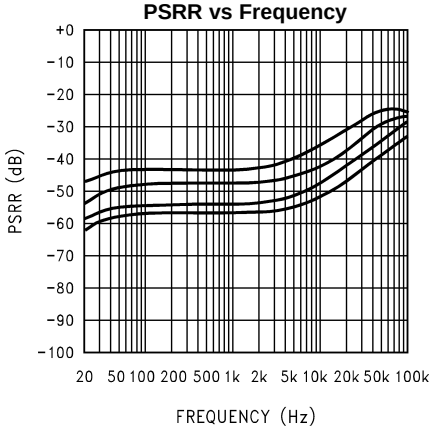


Figure 23. V_{DD} = 3V, R_L = 4Ω, R_{SOURCE} = 10Ω, V_{RIPPLE} = 200mV_{P-P}, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

PSRR vs Frequency

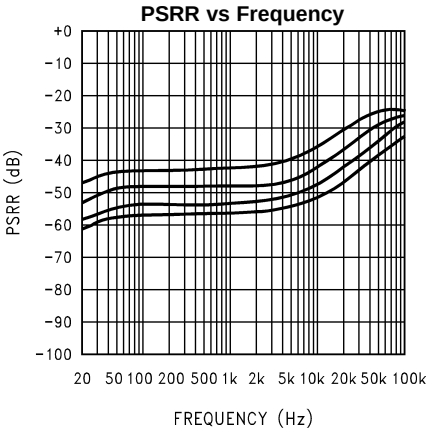


Figure 24. V_{DD} = 3V, R_L = 8Ω, R_{SOURCE} = 10Ω, V_{RIPPLE} = 200mV_{P-P}, at (from top to bottom at 1kHz): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

Output Power vs Load Resistance

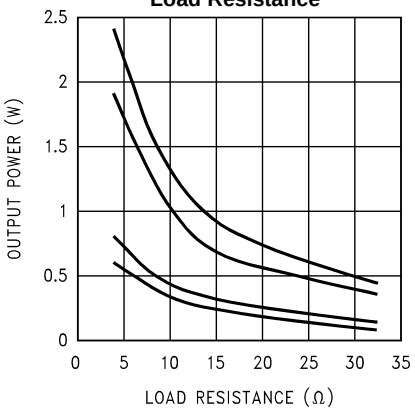


Figure 25. f_{IN} = 1kHz, at (from top to bottom at 20Ω): V_{DD} = 5V, THD = 10%; V_{DD} = 5V, THD = 1%; V_{DD} = 3V, THD = 10%; V_{DD} = 3V, THD = 1%

Typical Performance Characteristics
MH Specific Characteristics (continued)

Channel-to-Channel gain Mismatch vs Power Supply Voltage

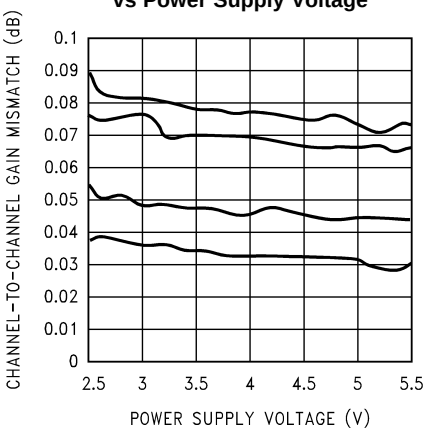


Figure 26. R_L = 4Ω, f_{IN} = 1kHz, at (from top to bottom at 4V): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

Channel-to-Channel gain Mismatch vs Power Supply Voltage

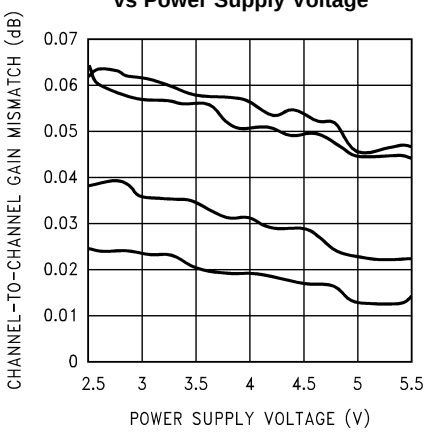


Figure 27. R_L = 8Ω, f_{IN} = 1kHz, at (from top to bottom at 4V): A_V = 21.6dB, A_V = 15.6dB, A_V = 10dB, A_V = 6dB

Dropout Voltage vs Power Supply Voltage

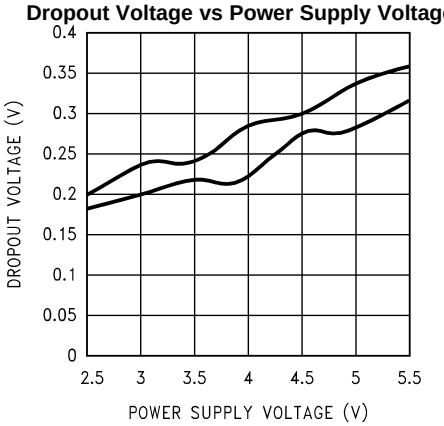


Figure 28. R_L = 8Ω, f_{IN} = 1kHz, both channels driven and loaded at (from top to bottom at 4V): positive signal swing, negative signal swing

Dropout Voltage vs Power Supply Voltage

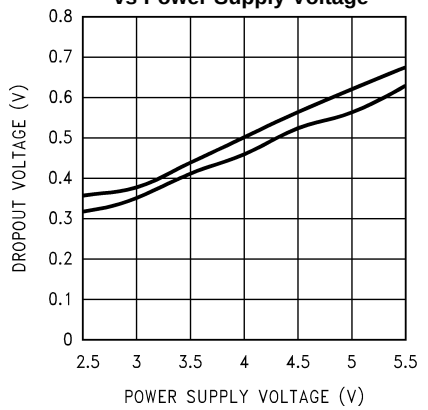


Figure 29. R_L = 4Ω, f_{IN} = 1kHz, both channels driven and loaded at (from top to bottom at 4V): positive signal swing, negative signal swing

Amplifier Power Dissipation vs Amplifier Load Dissipation

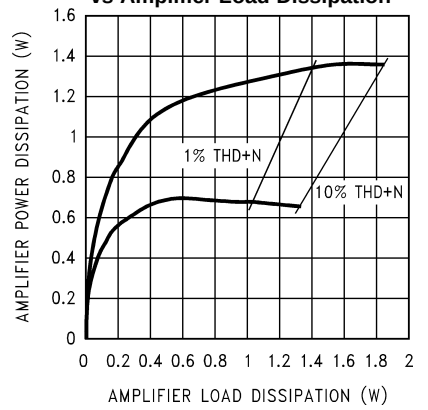


Figure 30. V_{DD} = 5V, f_{IN} = 1kHz, at (from top to bottom at 1W): R_L = 4Ω, R_L = 8Ω, single channel driven and loaded

Amplifier Power Dissipation vs Amplifier Load Dissipation

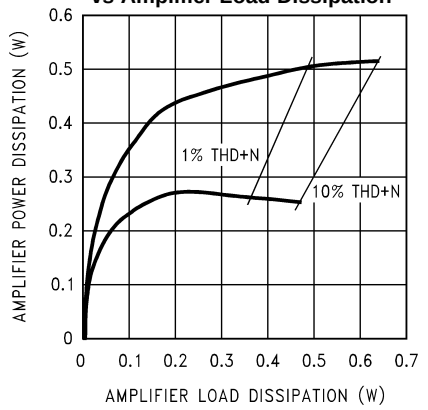


Figure 31. V_{DD} = 3V, f_{IN} = 1kHz, at (from top to bottom at 0.3W): R_L = 4Ω, R_L = 8Ω, single channel driven and loaded

Typical Performance Characteristics
MH Specific Characteristics (continued)

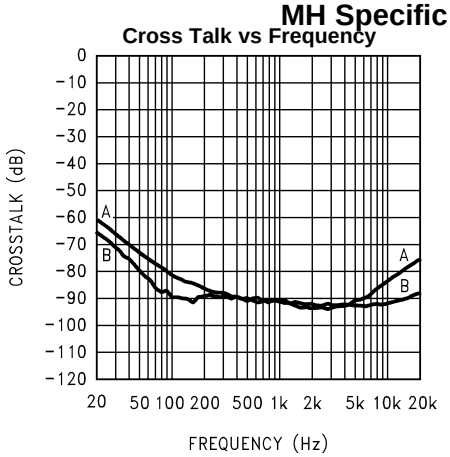


Figure 32. V_{DD} = 5V, R_L = 8Ω, A_V = 6dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

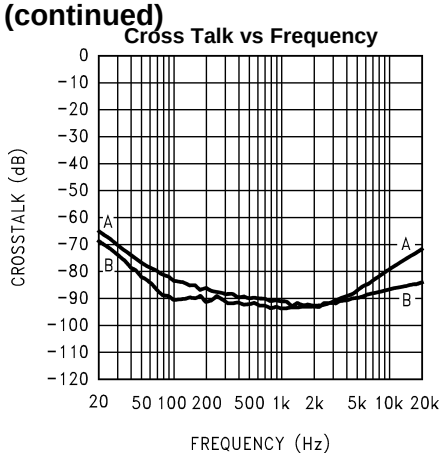


Figure 33. V_{DD} = 5V, R_L = 8Ω, A_V = 10dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

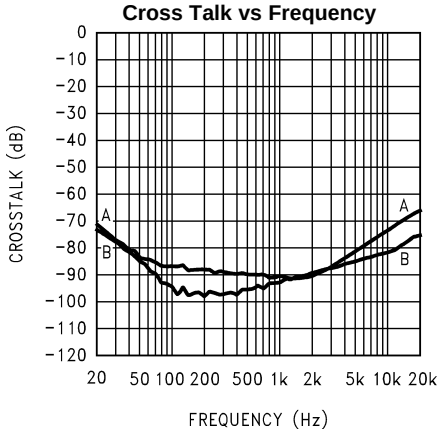


Figure 34. V_{DD} = 5V, R_L = 8Ω, A_V = 15.6dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

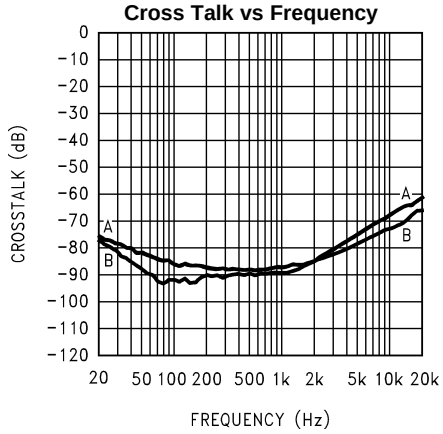


Figure 35. V_{DD} = 5V, R_L = 8Ω, A_V = 21.6dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

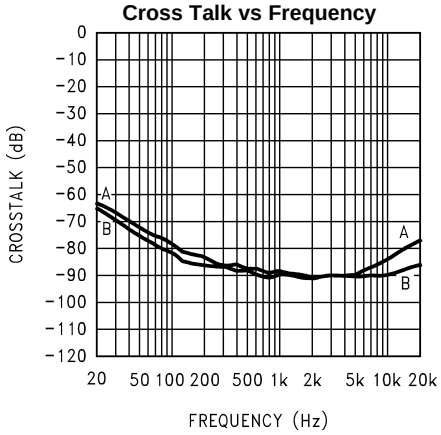


Figure 36. V_{DD} = 3V, R_L = 8Ω, A_V = 6dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

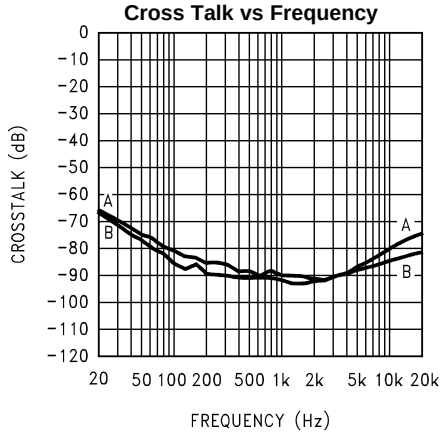


Figure 37. V_{DD} = 3V, R_L = 8Ω, A_V = 10dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

Typical Performance Characteristics
MH Specific Characteristics (continued)

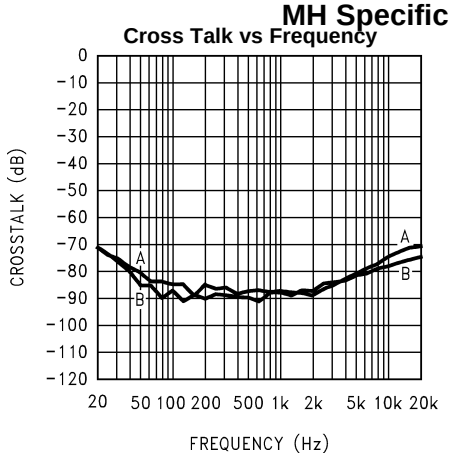


Figure 38. V_{DD} = 3V, R_L = 8Ω, A_V = 15.6dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

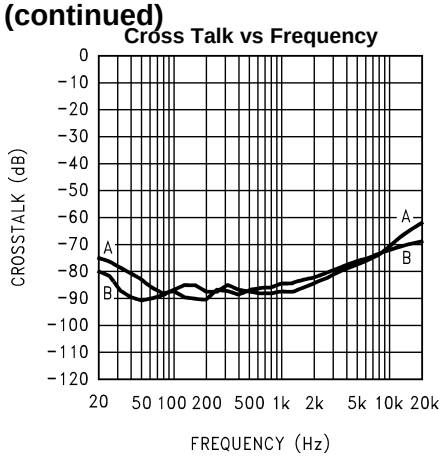


Figure 39. V_{DD} = 3V, R_L = 8Ω, A_V = 21.6dB, A = Left channel driven, right channel measured; B = Right channel driven, left channel measured

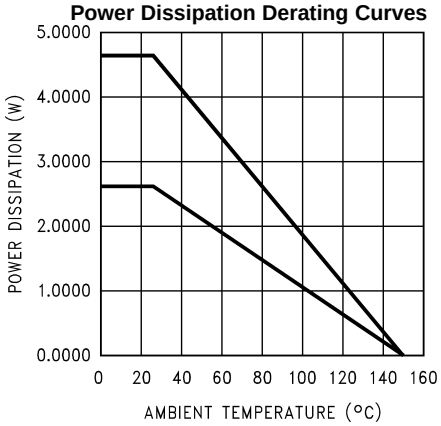


Figure 40. V_{DD} = 5V, R_L = 8Ω, f_{IN} = 1kHz, (from top to bottom at 40°C): 3in x 3in four-layer PCB with bottom and two inner layers connected to the package's DAP, 1.5in x 1.5in two-layer PCB with bottom and top layer planes connected to the package's DAP

APPLICATION INFORMATION

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3W AND 4W LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation also adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, each of the LM4869's stereo channels consists of two operational amplifiers. The LM4869 can be used to drive a speaker connected between the two outputs of each channel's amplifiers.

Figure 1 shows that the output of Amp1 serves as the input to Amp2, which results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between OUT+ and OUT- and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2(R_F/R_I) \quad (1)$$

Bridge mode is different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This results in four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output assumes that the amplifier is not current limited or the output signal is not clipped. To ensure minimum output signal clipping when selecting one of the amplifier's four closed-loop gains, refer to the Audio Power Amplifier Design section.

Another advantage of the differential bridge output is no net DC voltage across the load. This results from biasing OUT+ and OUT- at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single supply amplifier's half-supply bias voltage across the load. The current flow created by the half-supply bias voltage increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful bridged or single-ended amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in the internal power dissipation point for a bridge amplifier operating at the same given conditions.

$$P_{DMAX} = 4 * (V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \quad (3)$$

The LM4869 has four operational amplifiers in one package and the maximum internal power dissipation is four times that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 2W. The maximum power dissipation point obtained from Equation 3 must not exceed the power dissipation predicted by Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

For the exposed DAP TSSOP package, θ_{JA}= 41°C/W. T_{JAMAX} = 150°C for the LM4869. For a given ambient temperature T_A, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation (3) is greater than that of Equation 4, decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that does not violate the maximum junction temperature is approximately 68°C. This further assumes that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power decreases. Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

BTL GAIN SELECTION

The LM4869 features four fixed, internally set, BTL voltage gains: 6dB, 10dB, 15.6dB, and 21.6dB. Select one of the four gains by applying a logic level signal to the GAIN0 (MSB) and GAIN1 (LSB) digital inputs.

The closed-loop gain of the first amplifier is adjustable, having four different gains, whereas two internal 20kΩ resistors set the second amplifier's gain at -1. Table 1. LOGIC LEVEL TRUTH TABLE FOR SHUTDOWN OPERATION section, shows the state of the two logic inputs required to select one of the four gain values.

GAIN 0	GAIN 1	Selected Gain (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitors connected to the bypass and power supply pins should be placed as close to the LM4869 as possible. The capacitor connected between the bypass pin and ground improves the internal bias voltage's stability, producing improved PSRR. The improvements to PSRR increase as the bypass pin capacitor value increases.

Typical applications employ a 5V regulator with 10µF and a 0.1µF filter capacitors that aid in supply stability. Their presence, however, does not eliminate the need for bypassing the LM4869's supply pins. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the Selecting External Components section), system cost, and size constraints.

MICRO-POWER SHUTDOWN

The LM4869 features an active-low micro-power shutdown mode. The voltage applied to the SHUTDOWN pin controls the LM4869's shutdown function. Activate micro-power shutdown by applying 0V to the SHUTDOWN pin. The logic threshold is typically 0.4V for a logic low and 1.5V for a logic high. When active, the LM4869's micro-power shutdown feature turns off the amplifier's bias circuitry, disables the internal $V_{DD}/2$ generator, and forces the amplifier outputs into a high impedance state. The result is greatly reduced power supply current. The low 0.1µA typical shutdown current is achieved by applying a voltage to the SHUTDOWN pin that is as near to GND as possible. A voltage that is greater than GND may increase the shutdown current.

There are a few methods to control the micro-power shutdown. These include using a single-pole, single-throw switch (SPST), a microprocessor, or a microcontroller. When using a switch, connect a 100kΩ pull-down resistor between the SHUTDOWN pin and GND and the SPST switch between the SHUTDOWN pin and V_{DD}. Select normal amplifier operation by closing the switch. Opening the switch applies GND to the SHUTDOWN pin, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the active-state voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-down resistor.

Table 1. LOGIC LEVEL TRUTH TABLE FOR SHUTDOWN OPERATION

SHUTDOWN	OPERATIONAL MODE
High	Full Power, stereo BTL amplifiers
Low	Micro-power Shutdown

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4869's performance requires properly selecting external components. Though the LM4869 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values. The LM4869 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the Audio Power Amplifier Design section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C_I, C_2 and C_3, C_4) in Figure 1. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals with frequencies below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, CI - C4 can also affect on the LM4869's turn-on and turn-off transient ("click and pop") performance. When the supply voltage is first applied, a transient may be created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the transient is proportional to the value of, and more importantly, the mismatch between, the capacitors connected to a given pair of inverting and non-inverting inputs. The better the match, the less the transient magnitude.

Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. This fixed current is supplied through amplifiers input pins. Thus, selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency will reduce turn-on time and help ensure that transients are minimized.

The LM4869's nominal input resistance (R_i) is 25kΩ (20kΩ, minimum) and the input capacitor, C_i, form high pass filter with a -3dB low frequency limit defined by Equation 5.

$$f_{-3dB} = 1/2\pi(25k\Omega)C_i \quad (5)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_I, is 0.047µF. The 0.47µF C_I shown in Figure 1 allows the LM4869 to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides optimizing the input capacitor value, careful consideration should be paid to value of C_B, the capacitor connected between the BYPASS pin and ground. Since C_B determines how fast the LM4869 settles to its quiescent operating state, its value is critical when minimizing turn-on transients. The slower the LM4869's outputs ramp to their quiescent DC voltage (nominally ½ V_{DD}), the smaller the turn-on transient. Choosing C_B equal to 0.47µF along with a small value of C_i (in the range of 0.047µF to 0.47µF), produces a transient-free turn-on and shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize turn-on transients.

OPTIMIZING OUTPUT TRANSIENT REDUCTION (CLICK AND POP PERFORMANCE)

The LM4869 contains circuitry to minimize turn-on and shutdown transients or 'clicks and pop'. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply voltage is ramping to its final value, the LM4869's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the amplifier inputs and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the bypass pin current can not be modified, changing the size of C_B alters the device's turn-on time and the magnitude of output transients. Increasing the value of C_B reduces the magnitude of turn-on transients. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationships between the size of C_B + 2(C_I) and the turn-on time. The table shows some typical turn-on times for various values of C_B:

C_B	Ton	
	C_i = 0.47µF	C_i = 0.33µF
0.01µF	110ms	80ms
0.1µF	120ms	90ms
0.22µF	140ms	100ms
0.47µF	170ms	140ms
1.0µF	240ms	210ms

In order eliminate 'clicks and pops', all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause 'clicks and pops'.

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	1 W_{RMS}
Load Impedance:	8Ω
Input Level:	1 V_{RMS}
Input Impedance:	20 kΩ
Bandwidth:	100 Hz−20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the desired output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation 6, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To ac-count for the amplifier's dropout voltage, two additional volt-ages, based on the Dropout Voltage vs Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation 6. The result is Equation 7.

$$V_{outpeak} = \sqrt{(2R_L P_O)} \quad (6)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (7)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4869 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the Power Dissipation section.

After satisfying the LM4869's power dissipation requirements, the minimum differential gain is found using Equation (8).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (8)$$

Thus, a minimum gain of 2.83 allows the LM4869's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 3. In the example design, the gain will be set to 10dB (A_{VD} = 3.2) by applying a logic low to GAIN 0 and a logic high to GAIN 1.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. This extended bandwith produces a gain variation of -0.17dB at the bandwith's limits, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (9)$$

and an

$$f_H = 20kHz \times 5 = 100kHz \quad (10)$$

As mentioned in the External Components section, the internal input resistor and C_i create a high pass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (11).

$$f_{-3dB} = 1/2\pi(20k\Omega)C_I \quad (11)$$

The result is (using the minimum R_{IN} resistor value to ensure correct magnitude response at 20Hz)

$$1/(2\pi*20k\Omega*20Hz) = 0.398\mu F \quad (12)$$

Use a 0.39µF capacitor, the closest standard value. The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, A_{VD}, determines the upper passband response limit. With A_{VD} = 3.2 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 320kHz. This is less than the LM4869's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

Recommended Printed Circuit Board Layout

Figure 41 through Figure 45 show the recommended four-layer PC board layout that is optimized for the 20-pin PWP-packaged LM4869 and associated external components. This circuit is designed for use with an external 5V supply and 3Ω (or higher) speakers (or load resistors).

This circuit board is easy to use. Apply 5V and ground to the board's V_{DD} and GND terminals, respectively. Connect speakers (or load resistors) between the board's -OUTA and +OUTA and -OUTB and +OUTB pads. Apply balanced differential stereo input signals to the input pins labeled "-INA," "+INA," "-INB," and "+INB."

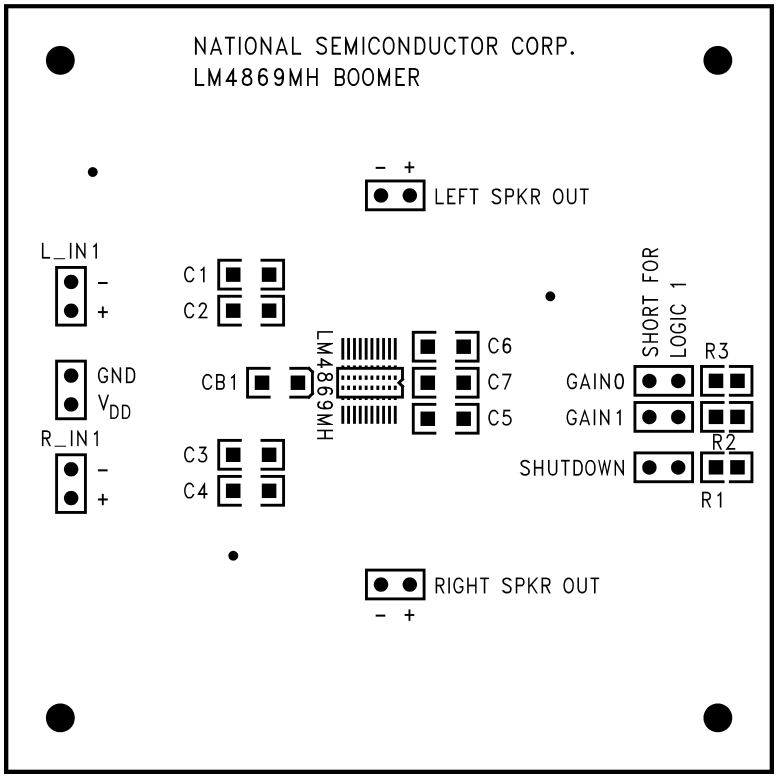


Figure 41. Recommended MH PC Board Layout: Component-Side Silkscreen

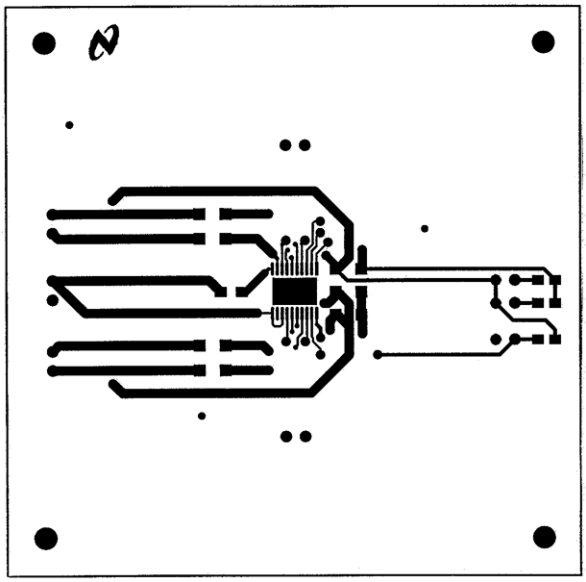


Figure 42. Recommended MH PC Board Layout: Component-Side Layout

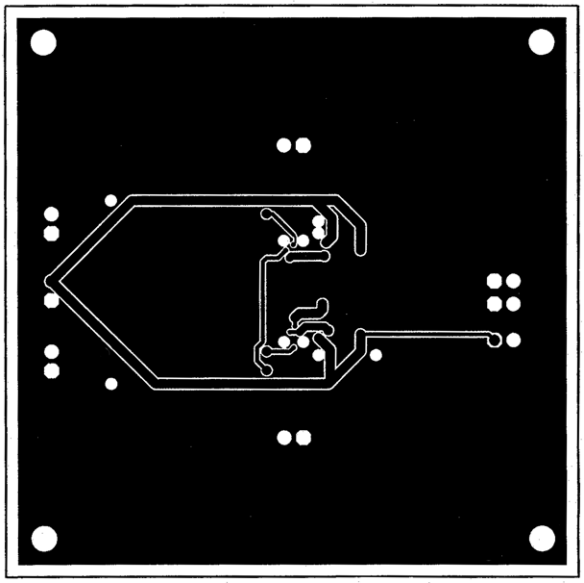


Figure 43. Recommended MH PC Board Layout: Upper Inner-Layer Layout

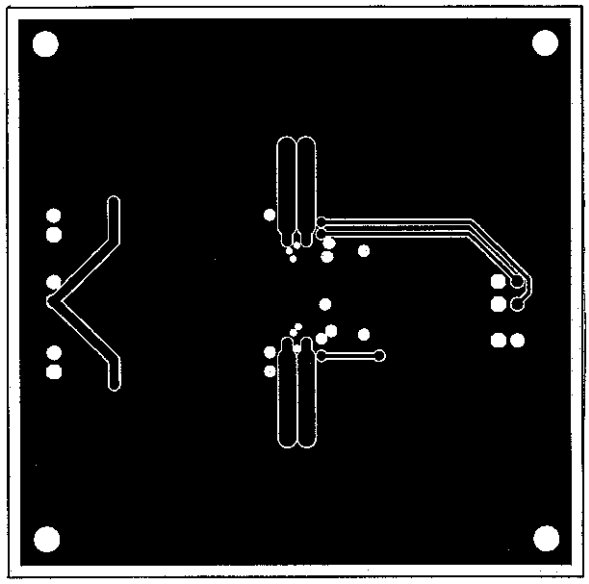


Figure 44. Recommended MH PC Board Layout: Lower Inner-Layer Layout

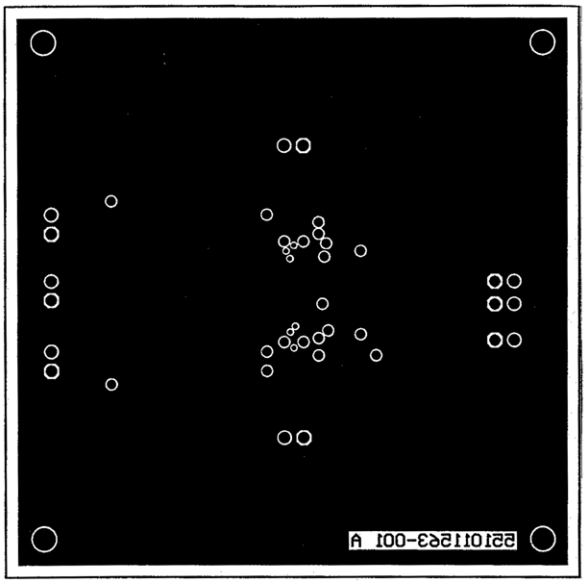


Figure 45. Recommended MH PC Board Layout: Bottom-Side Layout

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	20

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