

THC63LVDM83E

28bits LVTTTL/CMOS to 4ch LVDS Serializer/Transmitter

General Description

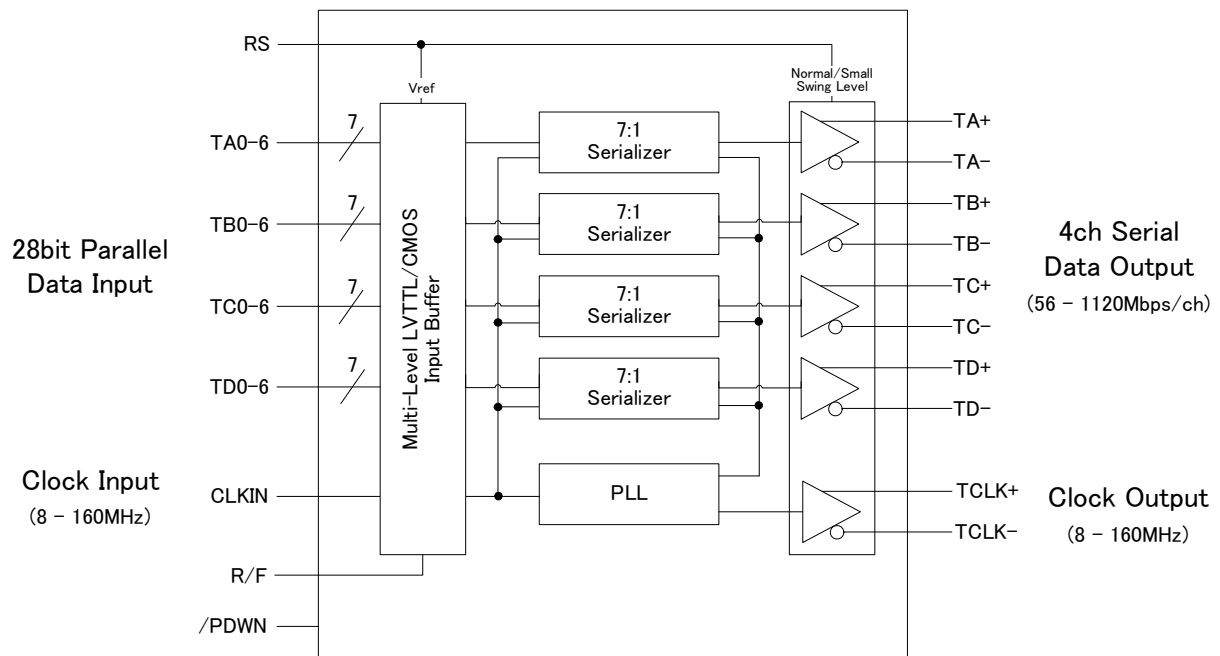
The THC63LVDM83E is a general purpose data serializer based on LVDS technology with no overhead for protocol or encoding.

The THC63LVDM83E converts 28bits of CMOS/TTL data into 4ch LVDS data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin.

Features

- 49pin 0.65mm pitch VFBGA Package
- Wide Input clock range: 8-160MHz
- Maximum total throughput 4.48Gbit/s@160MHz
- 3.3/2.5/1.8/1.2V voltage logic input
- LVDS swing is reducible by RS-pin to reduce EMI and power consumption.
- PLL requires no external components.
- On chip jitter filtering.
- Spread Spectrum Clock input tolerant.
- Power down mode.
- Input clock triggering edge is selectable by R/F-pin.
- Operates from a Single 3.3V Supply and 110mW(typ.) at 75MHz.

Block Diagram



Ball Out

TOP VIEW

	1	2	3	4	5	6	7
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0
B	TB4	TD3	TD2	TD1	TD0	TA-	TA+
C	TB5	TB0	GND	VCC	RS	TB-	TB+
D	TB6	TB1	GND	LVDS VCC	LVDS VCC	TC-	TC+
E	TC0	TB2	GND	PLL VCC	R/F	TCLK-	TCLK+
F	TC1	TB3	TD4	TD5	TD6	TD-	TD+
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PDWN

Pin Description

Pin Name	Pin #	Type	Description																					
TA+, TA-	B7, B6	LVDS Output	4ch Serial Data Output																					
TB+, TB-	C7, C6																							
TC+, TC-	D7, D6																							
TD+, TD-	F7, F6																							
TCLK+, TCLK-	E7, E6																							
TA0 ~ TA6	A7,A6,A5,A4,A3,A2,A1	3.3V LVTTTL 2.5/1.8/1.2V CMOS Digital Input	28bit Parallel Data Input																					
TB0 ~ TB6	C2,D2,E2,F2,B1,C1,D1																							
TC0 ~ TC6	E1,F1,G1,G2,G3,G4,G5																							
TD0 ~ TD6	B5,B4,B3,B2,F3,F4,F5																							
CLKIN	G6																							
/PDWN	G7	3.3V LVTTTL Digital Input	Power Down Control H: Normal operation L: Power Down (All output are Hi-Z.)																					
R/F	E5		Input Clock Triggering Edge Select H: Rising edge L: Falling edge																					
RS	C5	Analog Input	Input/output Level Select and 2.5/1.8/1.2V Logic level Reference Voltage Input																					
			<table border="1"> <thead> <tr> <th>RS-pin Input Voltage Setting</th> <th>Data/Clock Input Voltage</th> <th>Input Buffer Vref</th> <th>LVDS Output VOD</th> </tr> </thead> <tbody> <tr> <td>VCC</td> <td>3.3V</td> <td>VCC/2</td> <td rowspan="3">350mV</td> </tr> <tr> <td>1.25V</td> <td>2.5V</td> <td>1.25V</td> </tr> <tr> <td>0.9V</td> <td>1.8V</td> <td>0.9V</td> </tr> <tr> <td>0.6V</td> <td>1.2V</td> <td>0.6V</td> <td rowspan="2">200mV</td> </tr> <tr> <td>GND</td> <td>3.3V</td> <td>VCC/2</td> </tr> </tbody> </table>	RS-pin Input Voltage Setting	Data/Clock Input Voltage	Input Buffer Vref	LVDS Output VOD	VCC	3.3V	VCC/2	350mV	1.25V	2.5V	1.25V	0.9V	1.8V	0.9V	0.6V	1.2V	0.6V	200mV	GND	3.3V	VCC/2
RS-pin Input Voltage Setting	Data/Clock Input Voltage		Input Buffer Vref	LVDS Output VOD																				
VCC	3.3V		VCC/2	350mV																				
1.25V	2.5V		1.25V																					
0.9V	1.8V	0.9V																						
0.6V	1.2V	0.6V	200mV																					
GND	3.3V	VCC/2																						
VCC	C4	Power	Power Supply Pin for LVTTTL/CMOS input and digital circuit.																					
GND	C3,D3,E3		Ground Pins for Common.																					
LVDS VCC	D4,D5		Power Supply Pins for LVDS Outputs.																					
PLL VCC	E4		Power Supply Pin for PLL circuit.																					

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage	-0.3	+4.0	V
LVTTL/CMOS and Analog Input Voltage	-0.3	VCC + 0.3	V
LVDS Transmitter Output Voltage	-0.3	VCC + 0.3	V
Output Current	-30	30	mA
Junction Temperature	-	+125	°C
Storage Temperature	-55	+125	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	1.2	W

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC	All Supply Voltage	3.0	3.3	3.6	V
Ta	Operating Ambient Temperature	0	25	+70	°C
CLKIN	Clock Frequency	8	-	160	MHz

Power Consumption

VCC = 3.0~3.6V, Ta = 0~+70°C

Symbol	Parameter	Conditions	Typ*	Max	Units
I _{rw}	LVDS Transmitter Operating Current Gray Scale Pattern 16(Fig.1)	RL=100Ω, CL=5pF, f=85MHz RS=VCC, (RS=GND)	42 (34)	-	mA
		RL=100Ω, CL=5pF, f=160MHz RS=VCC, (RS=GND)	58 (50)	-	mA
	LVDS Transmitter Operating Current Worst Case Pattern(Fig.2)	RL=100Ω, CL=5pF, f=85MHz RS=VCC, (RS=GND)	45 (36)	67 (56)	mA
		RL=100Ω, CL=5pF, f=160MHz RS=VCC, (RS=GND)	63 (55)	92 (80)	mA
I _{rw}	LVDS Transmitter Power Down Current		-	10	μA

*Typ values are at VCC=3.3V, Ta = +25°C

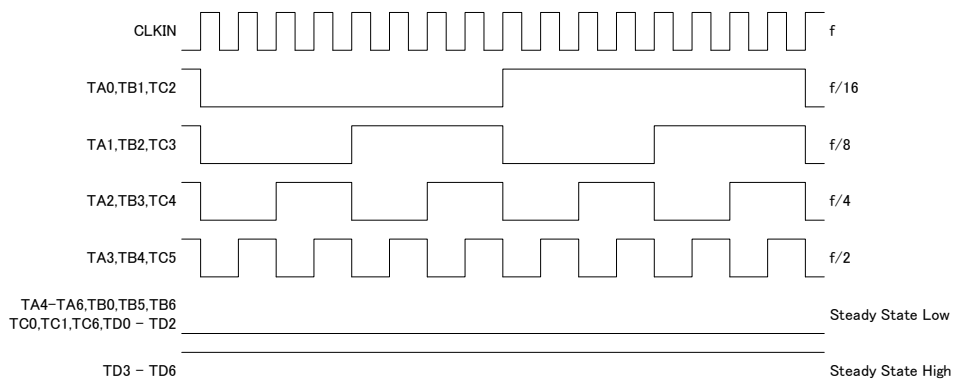


Figure 1. 16 Grayscale Pattern

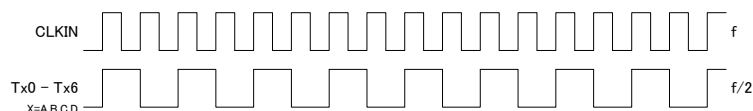


Figure 2. Worst Case Pattern

LVTTL/CMOS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	High Level Input Voltage	3.3V LVTTL V _{ref} = VCC/2	2.0	-	VCC	V
		2.5/1.8/1.2V CMOS V _{ref} = RS Input Voltage	V _{ref} + 0.1	-	VCC	
V _{IL}	Low Level Input Voltage	3.3V LVTTL V _{ref} = VCC/2	GND	-	0.8	V
		2.5/1.8/1.2V CMOS V _{ref} = RS Input Voltage	GND	-	V _{ref} - 0.1	
I _{IN}	Input Current	GND ≤ V _{IN} ≤ VCC	-	-	±10	μA

*Typ values are at VCC=3.3V, Ta = +25°C.

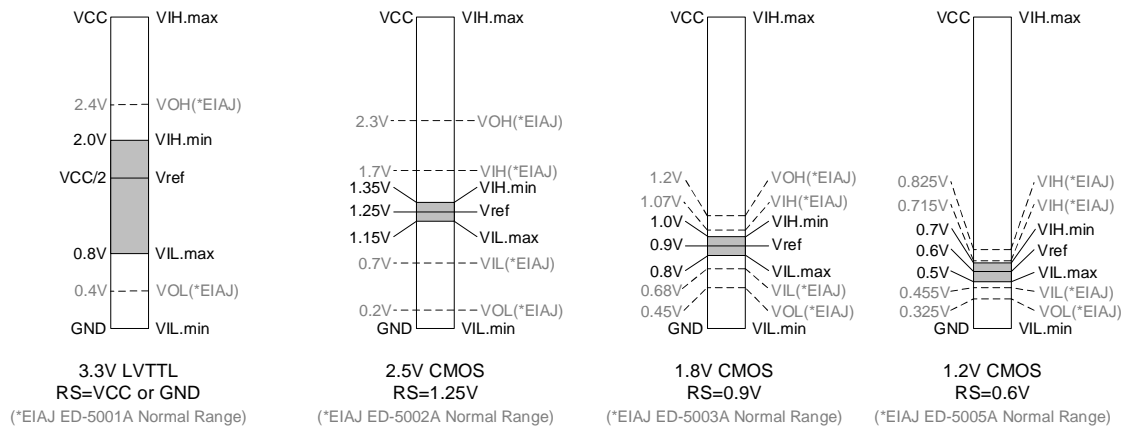


Figure 3. LVTTL/CMOS Digital Input Compatibility

LVDS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOD	Differential Output Voltage	RS=VCC, 0.6 ~ 1.4V RL=100Ω	250	350	450	mV
		RS=GND RL=100Ω	120	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω	-	-	35	mV
VOC	Common Mode Voltage	RL=100Ω	1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states	RL=100Ω	-	-	35	mV
Ios	Output Short Circuit Current	V _{OUT} =GND, RL=100Ω	-	-	-24	mA
Ioz	Output TRI-STATE Current	/PDWN=GND, V _{OUT} =GND to VCC	-	-	±10	μA

*Typ values are at VCC=3.3V, Ta = +25°C.

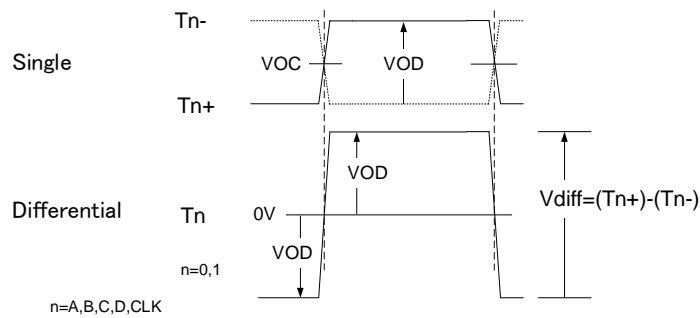


Figure 4. LVDS DC Specifications

LVTTL/CMOS AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLKIN Transition Time	-	-	5.0	ns
t_{TCP}	CLKIN Period	6.25	T	125	ns
t_{TCH}	CLKIN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLKIN Low Time	0.35T	0.5T	0.65T	ns
t_{TCD}	CLKIN to TCLK+/- Delay	-	3T	-	ns
t_{TS}	Tx0-6 Setup time to CLKIN	2.0	-	-	ns
t_{TH}	Tx0-6 Hold time to CLKIN	0.0	-	-	ns

*Typ values are at VCC=3.3V, Ta = +25°C

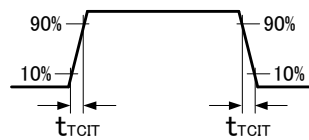


Figure 5. CLKIN Transition Time

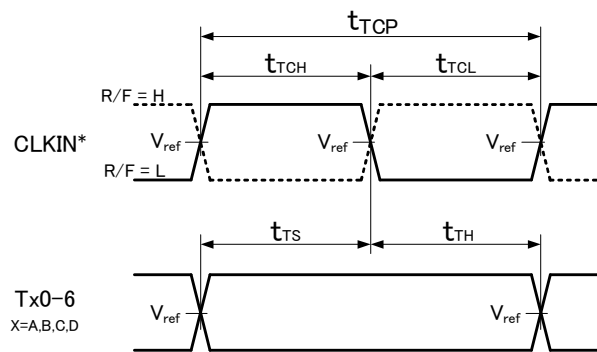


Figure 6. LVTTL/CMOS Input Timings

LVDS AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{LVT}	LVDS Transition Time	-	0.6	1.5	ns
t_{TOP1}	Output Data Position0 (T=6.25ns ~ 20ns)	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (T=6.25ns ~ 20ns)	T/7-0.15	T/7	T/7+0.15	ns
t_{TOP6}	Output Data Position2 (T=6.25ns ~ 20ns)	2T/7-0.15	2T/7	2T/7+0.15	ns
t_{TOP5}	Output Data Position3 (T=6.25ns ~ 20ns)	3T/7-0.15	3T/7	3T/7+0.15	ns
t_{TOP4}	Output Data Position4 (T=6.25ns ~ 20ns)	4T/7-0.15	4T/7	4T/7+0.15	ns
t_{TOP3}	Output Data Position5 (T=6.25ns ~ 20ns)	5T/7-0.15	5T/7	5T/7+0.15	ns
t_{TOP2}	Output Data Position6 (T=6.25ns ~ 20ns)	6T/7-0.15	6T/7	6T/7+0.15	ns

*Typ values are at VCC=3.3V, Ta = +25°C

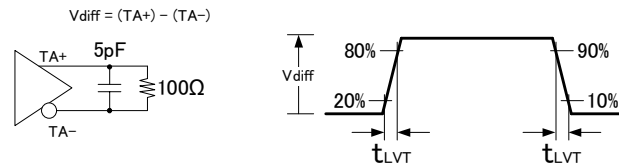


Figure 7. LVDS Output Load and Transition Time

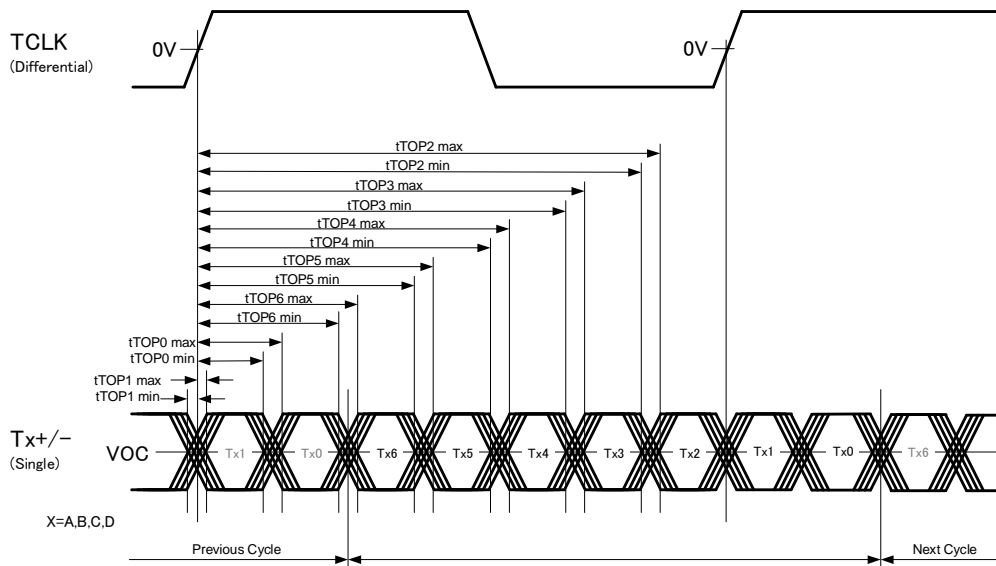


Figure 8. LVDS Output Data Position

Input to Output AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{TCD}	CLKIN to TCLK+/- Delay	-	3T	-	ns
t_{TPLL}	Phase Lock Loop Set	-	-	10.0	ms

*Typ values are at VCC=3.3V, Ta = +25°C

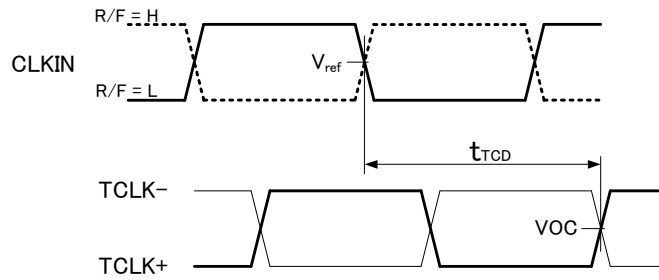


Figure 9. CLKIN to TCLK+/- Delay

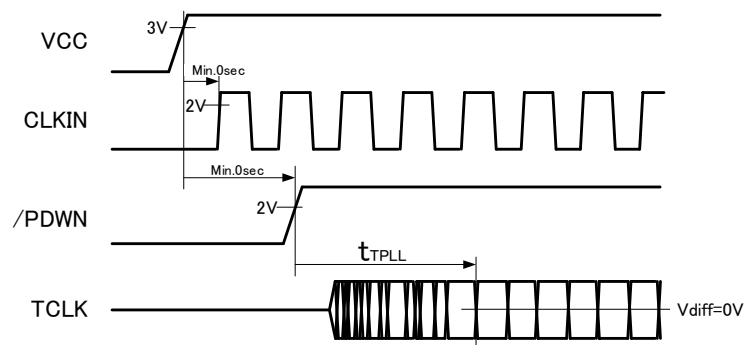
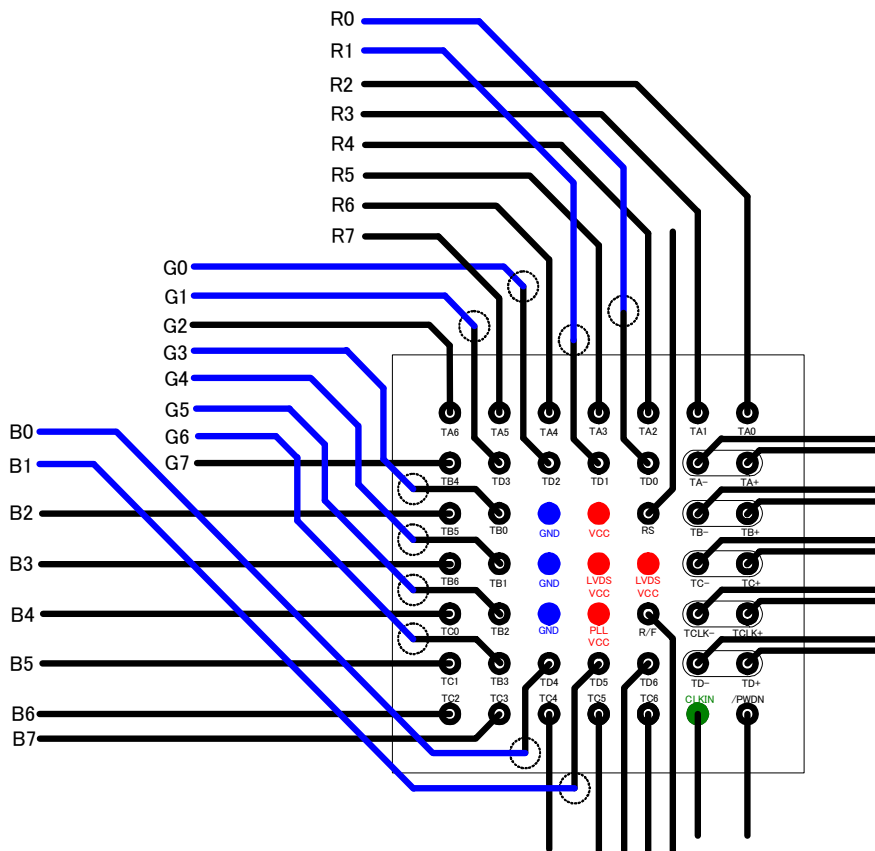


Figure 10. PLL Set Time

Board Layout Example

TOP VIEW

	1	2	3	4	5	6	7	
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0	A
B	TB4	TD3	TD2	TD1	TD0	TA-	TA+	B
C	TB5	TB0	GND	VCC	RS	TB-	TB+	C
D	TB6	TB1	GND	LVDS VCC	LVDS VCC	TC-	TC+	D
E	TC0	TB2	GND	PLL VCC	R/F	TCLK-	TCLK+	E
F	TC1	TB3	TD4	TD5	TD6	TD-	TD+	F
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PDWN	G
	1	2	3	4	5	6	7	



Note

1) Cable Connection and Disconnection

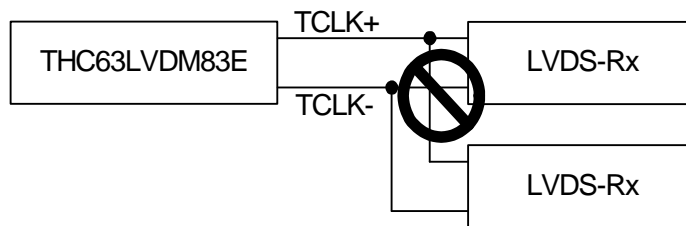
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect the each GND of the PCB which THC63LVDM83E and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

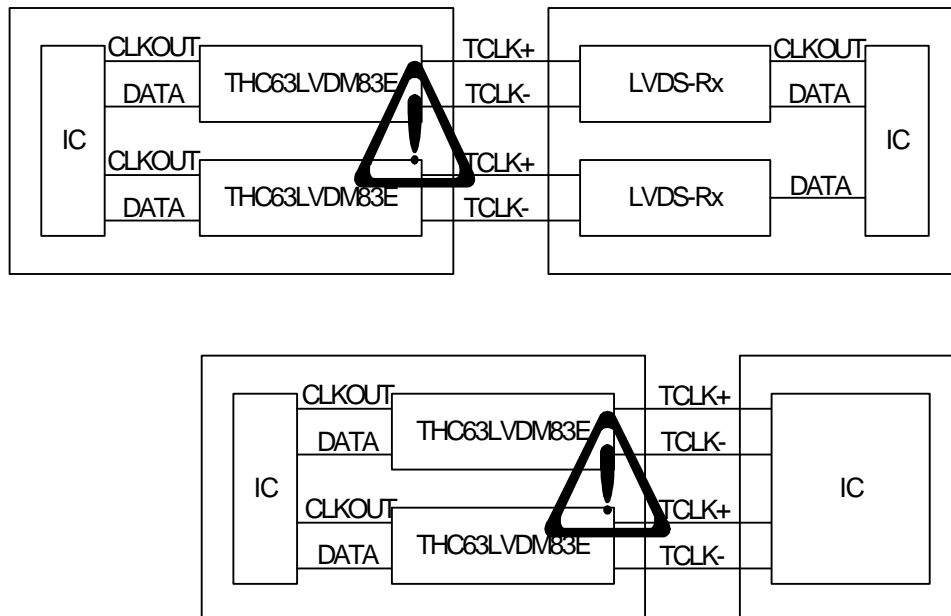
3) Multi Drop Connection

Multi drop connection is not recommended.

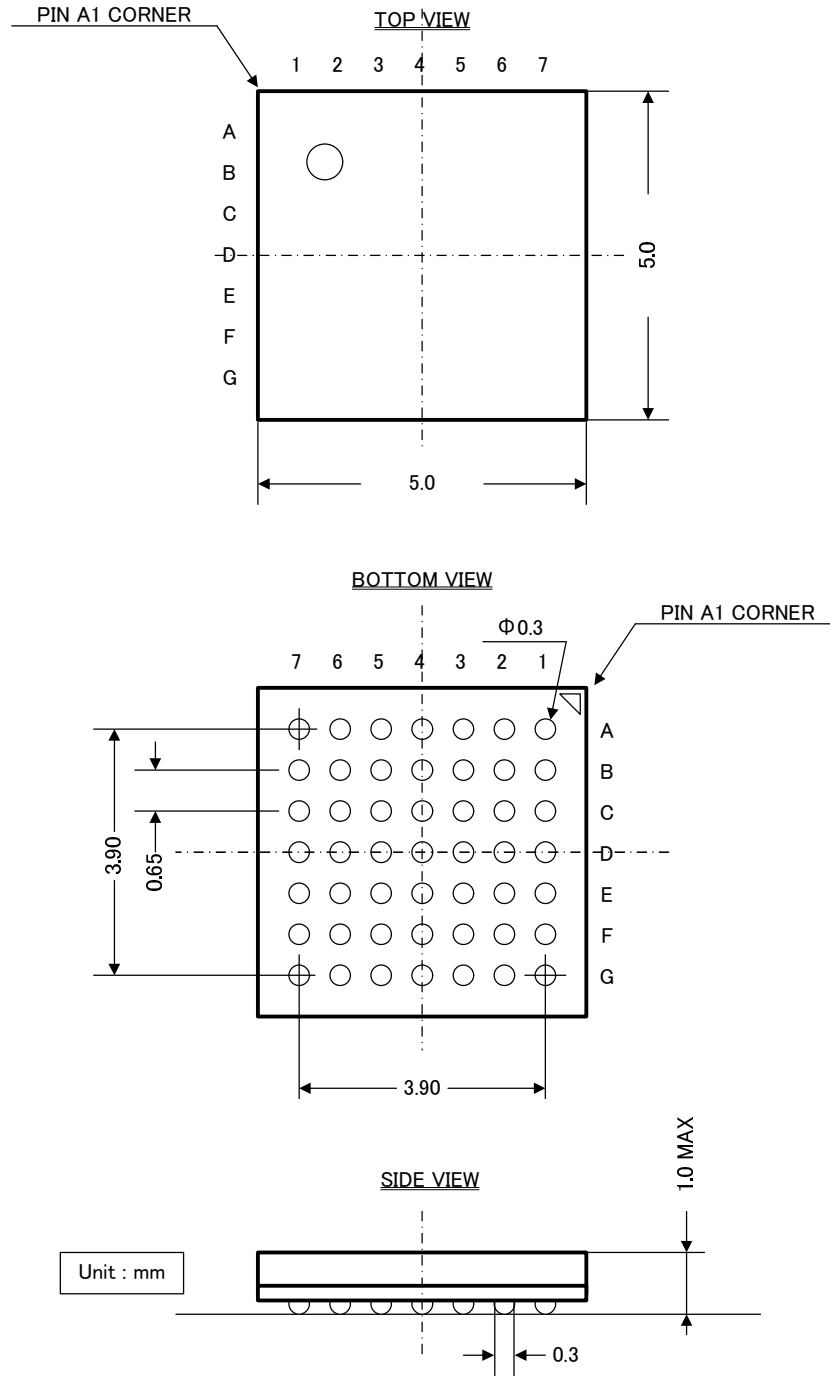


4) Asynchronous use

Asynchronous using such as following systems are not recommended.



Package



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7. Please note that this product is not designed to be radiation-proof.

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 10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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