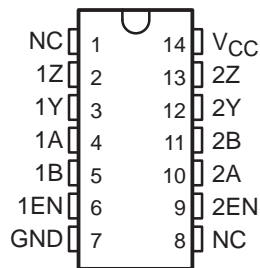


SN75159 DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

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- Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11
- Single 5-V Supply
- Balanced Line Operation
- TTL Compatible
- High-Impedance Output State for Party-Line Applications
- High-Current Active-Pullup Outputs
- Short-Circuit Protection
- Dual Channels
- Clamp Diodes at Inputs

D OR N PACKAGE
(TOP VIEW)



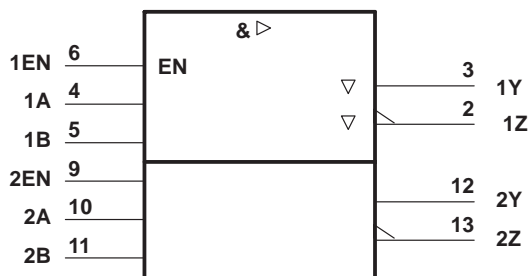
NC—No internal connection

description

The SN75159 dual differential line driver with 3-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

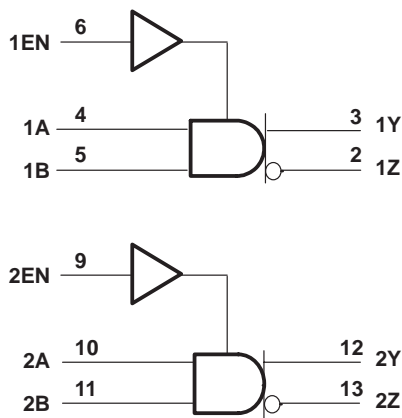
The SN75159 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

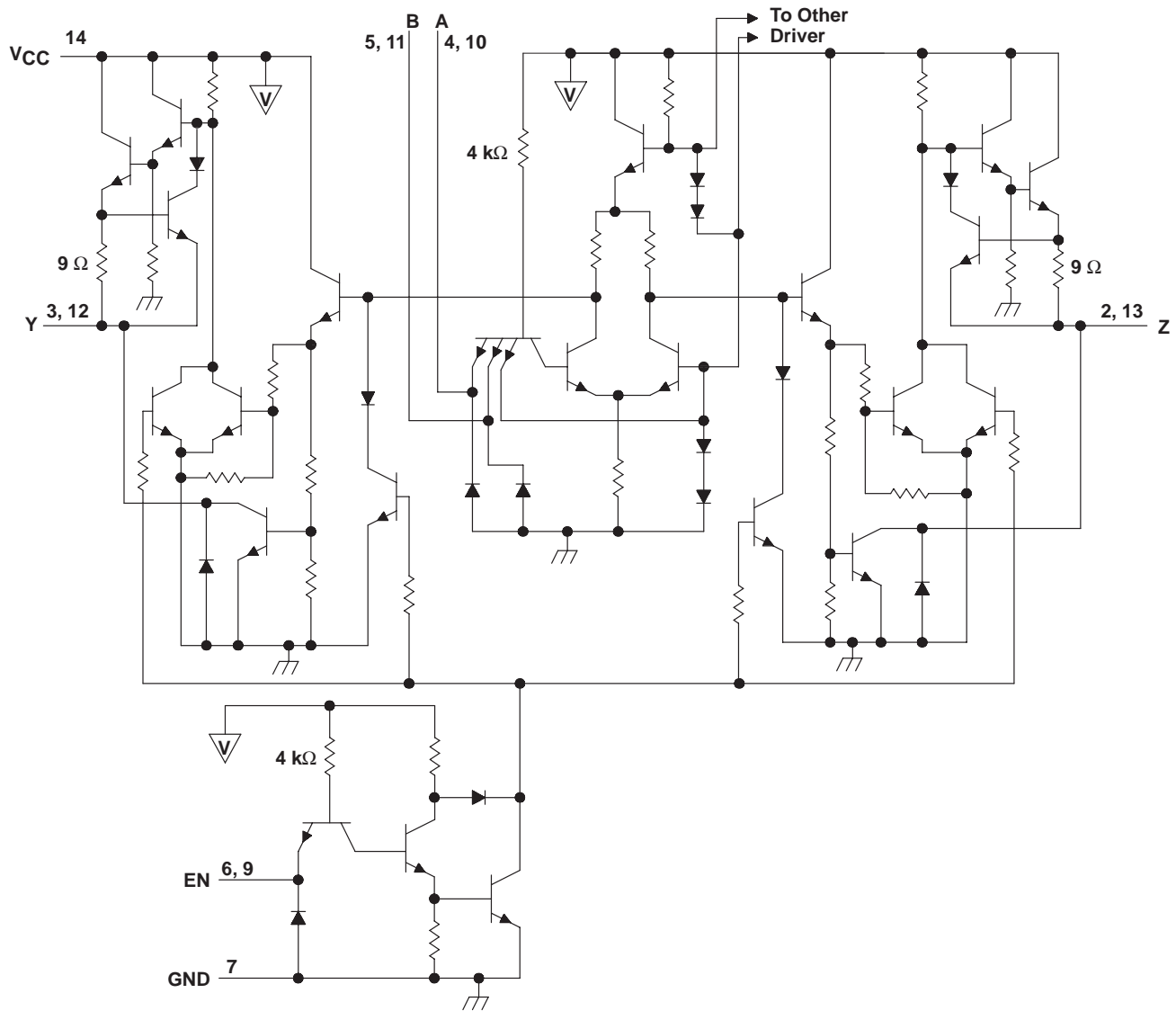
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SN75159 DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

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schematic (each driver)



 ... VCC bus

Resistor values shown are nominal.

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WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|------------------------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I | 5.5 V |
| Off-state voltage applied to open-collector outputs | 12 V |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values except differential output voltage V_{OD} are with respect to the network ground terminal. V_{OD} is at the Y output with respect to the Z output.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|---|--|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---------------------------------------|------|-----|------|------|
| Supply voltage, V_{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V_{IH} | 2 | | | V |
| Low-level input voltage, V_{IL} | | | 0.8 | V |
| High-level output voltage, I_{OH} | | | –40 | mA |
| Low-level output current, I_{OL} | | | 40 | mA |
| Operating free-air temperature, T_A | 0 | | 70 | °C |



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electrical characteristics over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|------------------|---|--|---|-----------------------------|------------|---------------|------|
| V_{IK} | Input clamp voltage | $V_{CC} = 4.75\text{ V}$, | $I_I = -12\text{ mA}$ | -0.9 | -1.5 | | V |
| V_{OH} | High-level output voltage | $V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, | $V_{IL} = 0.8\text{ V}$, $I_{OH} = -40\text{ mA}$ | 2.4 | 3 | | V |
| V_{OL} | Low-level output voltage | $V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, | $V_{IL} = 0.8\text{ V}$, $I_{OL} = 40\text{ mA}$ | | 0.25 | 0.4 | V |
| V_{OK} | Output clamp voltage | $V_{CC} = 5.25\text{ V}$, | $I_O = -40\text{ mA}$ | -1.1 | -1.5 | | V |
| V_O | Output voltage | $V_{CC} = 4.75\text{ V to } 5.25\text{ V}$, | $I_O = 0$ | 0 | | 6 | V |
| $ V_{OD1} $ | Differential output voltage | $V_{CC} = 5.25\text{ V}$, | $I_O = 0$ | | 3.5 | $2V_{OD2}$ | V |
| $ V_{OD2} $ | Differential output voltage | $V_{CC} = 4.75\text{ V}$ | | 2 | 3 | | V |
| $\Delta V_{OD} $ | Change in magnitude of differential output voltage‡ | $V_{CC} = 4.75\text{ V}$ | $R_L = 100\ \Omega$, See Figure 1 | | ± 0.02 | ± 0.4 | V |
| V_{OC} | Common-mode output voltage§ | $V_{CC} = 5.25\text{ V}$ | | 1.8 | 3 | V | |
| | | $V_{CC} = 4.75\text{ V}$ | | 1.5 | 3 | | |
| $\Delta V_{OC} $ | Change in magnitude of common-mode output voltage‡ | $V_{CC} = 4.75\text{ V to } 5.25\text{ V}$ | | | ± 0.01 | ± 0.4 | V |
| I_O | Output current with power off | $V_{CC} = 0$ | $V_O = 6\text{ V}$ | 0.1 | 100 | μA | |
| | | | $V_O = -0.25\text{ V}$ | -0.1 | -100 | | |
| | | | $V_O = -0.25\text{ V to } 6\text{ V}$ | | ± 100 | | |
| I_{OZ} | Off-state (high-impedance state) output current | $V_{CC} = 5.25\text{ V}$, Output controls at 0.8 V | $T_A = 25^\circ\text{C}$ | $V_O = 0\text{ to } V_{CC}$ | ± 10 | μA | |
| | | | $T_A = 70^\circ\text{C}$ | $V_O = 0$ | -20 | | |
| | | | | $V_O = 0.4\text{ V}$ | ± 20 | | |
| | | | | $V_O = 2.4\text{ V}$ | ± 20 | | |
| | | | | $V_O = V_{CC}$ | 20 | | |
| I_I | Input current at maximum input voltage | $V_{CC} = 5.25\text{ V}$, | $V_I = 5.5\text{ V}$ | | 1 | mA | |
| I_{IH} | High-level input current | $V_{CC} = 5.25\text{ V}$, | $V_I = 2.4\text{ V}$ | | 40 | μA | |
| I_{IL} | Low-level input current | $V_{CC} = 5.25\text{ V}$, | $V_I = 0.4\text{ V}$ | -1 | -1.6 | mA | |
| I_{OS} | Short-circuit output current¶ | $V_{CC} = 5.25\text{ V}$ | | -40 | -90 | -150 | mA |
| I_{CC} | Supply current (both drivers) | $V_{CC} = 5.25\text{ V}$, $T_A = 25^\circ\text{C}$, | Inputs grounded, No load | | 47 | 65 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$ except for V_{OC} , for which V_{CC} is as stated under test conditions.

‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

§ In ANSI Standard EIA/TIA-422-B, V_{OC} , which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS} .

¶ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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switching characteristics over operating free-air temperature range, $V_{CC} = 5\text{ V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|--|--|-----|------|-----|------|
| t_{PLH} | Propagation delay time, low-to-high-level output | $C_L = 30\text{ pF}$, $R_L = 100\ \Omega$, See Figure 2, Termination A | | 16 | 25 | ns |
| t_{PHL} | Propagation delay time, high-to-low-level output | | | 11 | 20 | ns |
| t_{PLH} | Propagation delay time, low-to-high-level output | $C_L = 15\text{ pF}$, See Figure 2, Termination B | | 13 | 20 | ns |
| t_{PHL} | Propagation delay time, high-to-low-level output | | | 9 | 15 | ns |
| t_{TLH} | Transition time, low-to-high-level output | $C_L = 30\text{ pF}$, $R_L = 100\ \Omega$, See Figure 2, Termination A | | 4 | 20 | ns |
| t_{THL} | Transition time, high-to-low-level output | | | 4 | 20 | ns |
| t_{PZH} | Output enable time to high level | $C_L = 30\text{ pF}$, $R_L = 180\ \Omega$, See Figure 3 | | 7 | 20 | ns |
| t_{PZL} | Output enable time to low level | $C_L = 30\text{ pF}$, $R_L = 250\ \Omega$, See Figure 4 | | 14 | 40 | ns |
| t_{PHZ} | Output disable time from high level | $C_L = 30\text{ pF}$, $R_L = 180\ \Omega$, See Figure 3 | | 10 | 30 | ns |
| t_{PLZ} | Output disable time from low level | $C_L = 30\text{ pF}$, $R_L = 250\ \Omega$, See Figure 4 | | 17 | 35 | ns |
| Overshoot factor | | $R_L = 100\ \Omega$, See Figure 2, Termination C | | | 10% | |

† All typical values are at $T_A = 25^\circ\text{C}$.

SYMBOL EQUIVALENTS

| DATA-SHEET PARAMETER | EIA/TIA-422-B |
|----------------------|---------------------------|
| V_O | V_{oa}, V_{ob} |
| $ V_{OD1} $ | V_o |
| $ V_{OD2} $ | V_t |
| $\Delta V_{OD} $ | $ V_t - \bar{V}_t $ |
| V_{OC} | $ V_{os} $ |
| $\Delta V_{OC} $ | $ V_{os} - \bar{V}_{os} $ |
| I_{OS} | $ I_{sa} , I_{sb} $ |
| I_O | $ I_{xa} , I_{xb} $ |

PARAMETER MEASUREMENT INFORMATION

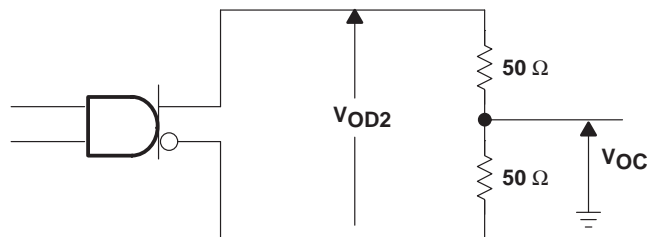
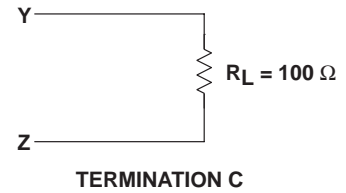
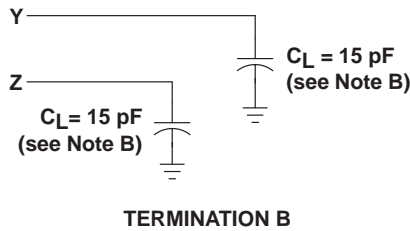
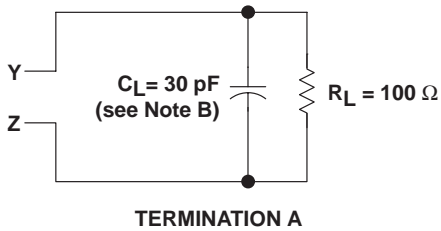
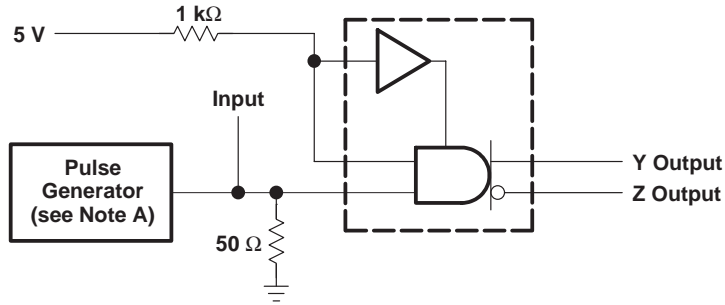


Figure 1. Differential and Common-Mode Output Voltages

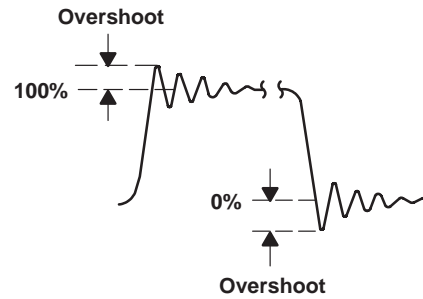
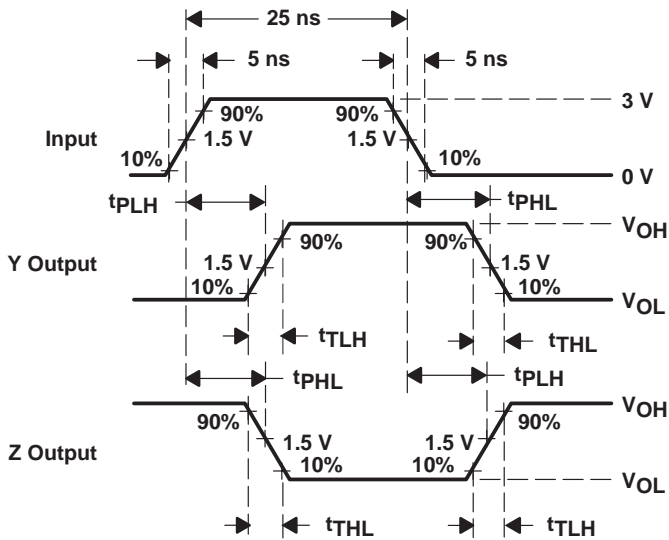
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DUAL DIFFERENTIAL LINE DRIVER
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUITS

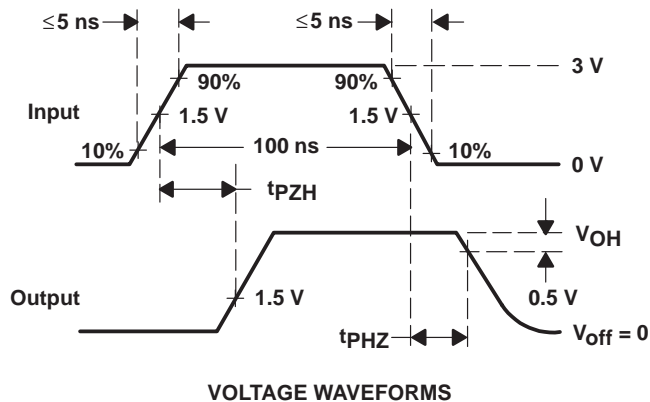
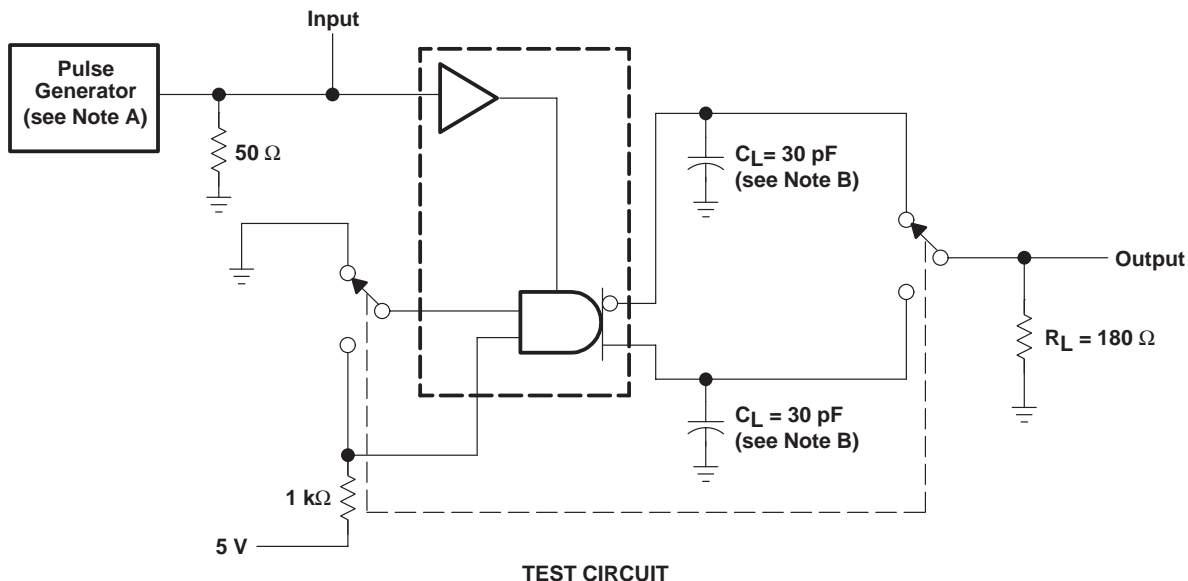


VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, $PRR \leq 10 \text{ MHz}$.
 B. C_L includes probe and jig capacitance.

Figure 2. Test Circuits, Voltage Waveforms, and Overshoot Factor

PARAMETER MEASUREMENT INFORMATION



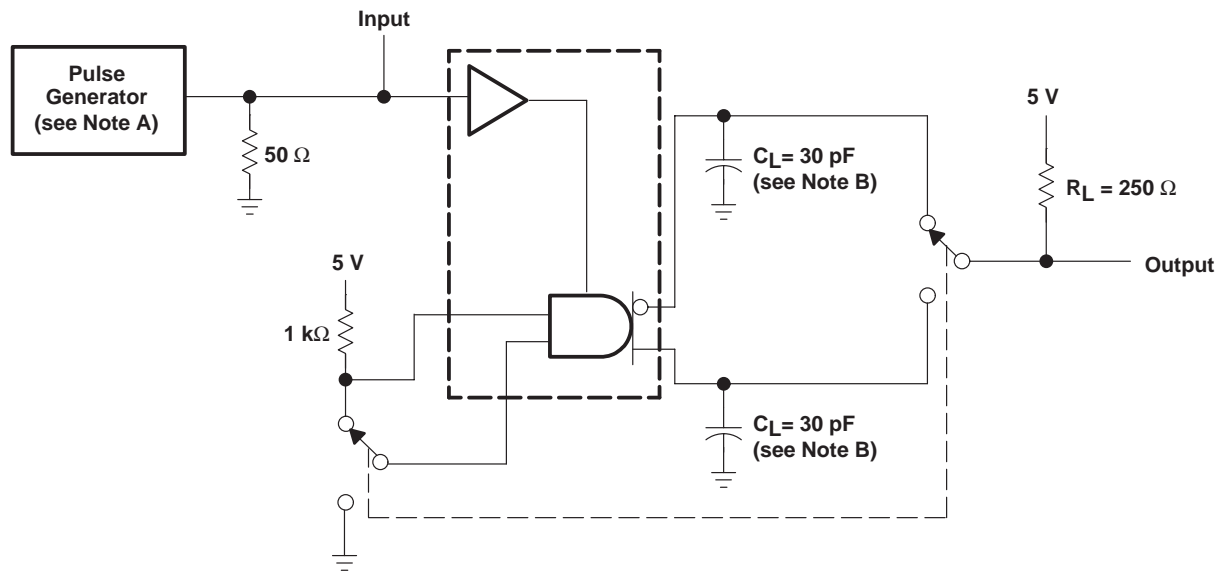
- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, $PRR \leq 500\text{ kHz}$.
 B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms

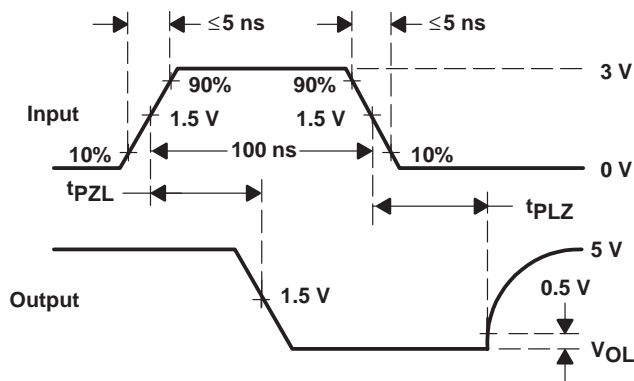
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, $PRR \leq 500 \text{ kHz}$.
 B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

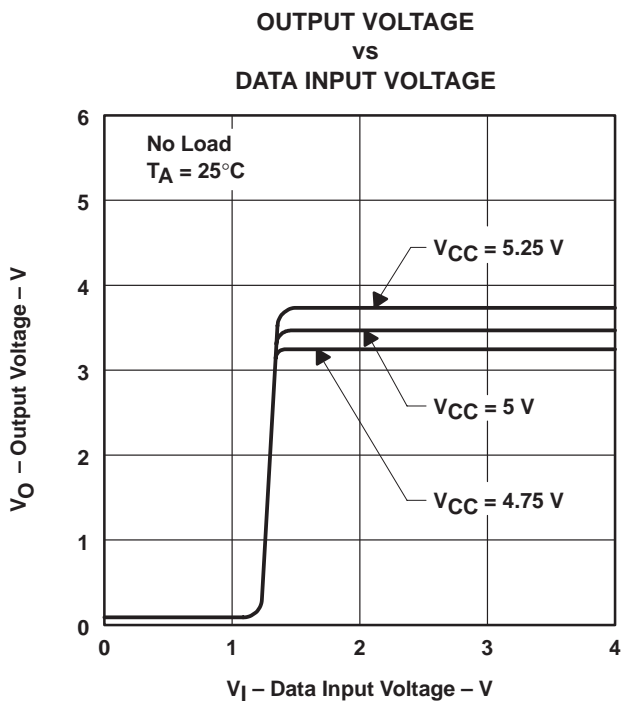


Figure 5

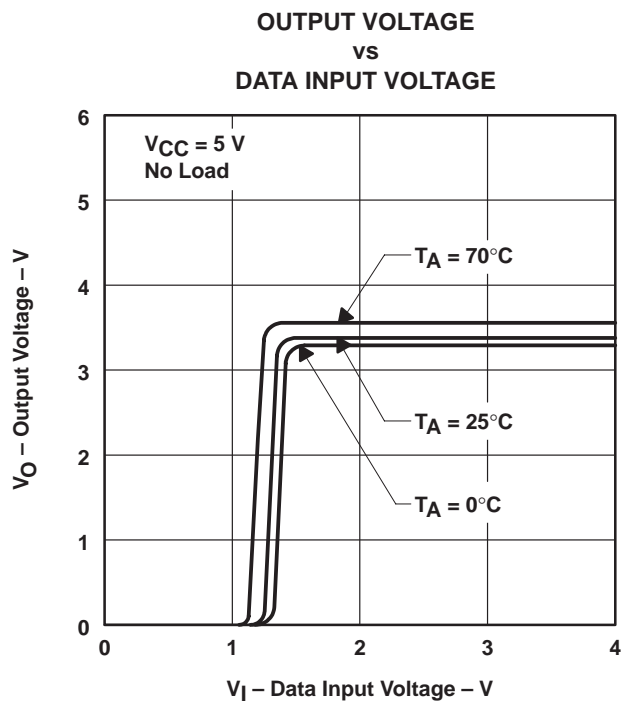


Figure 6

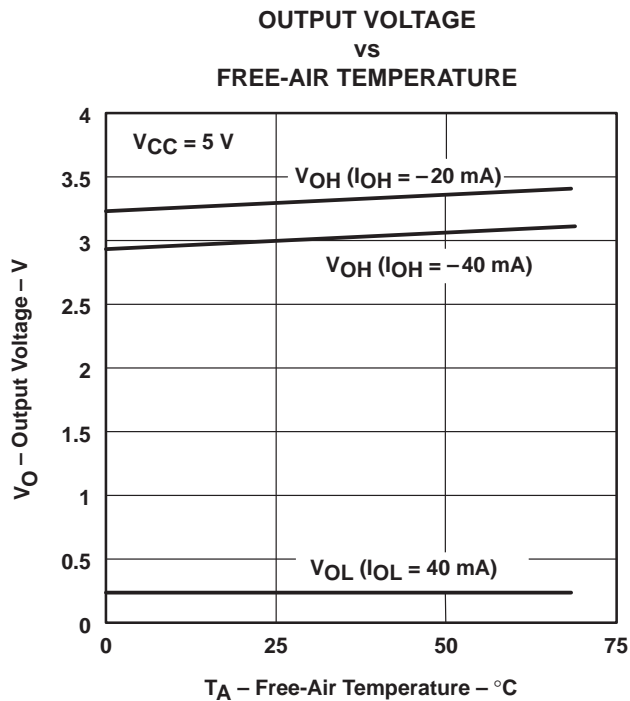


Figure 7

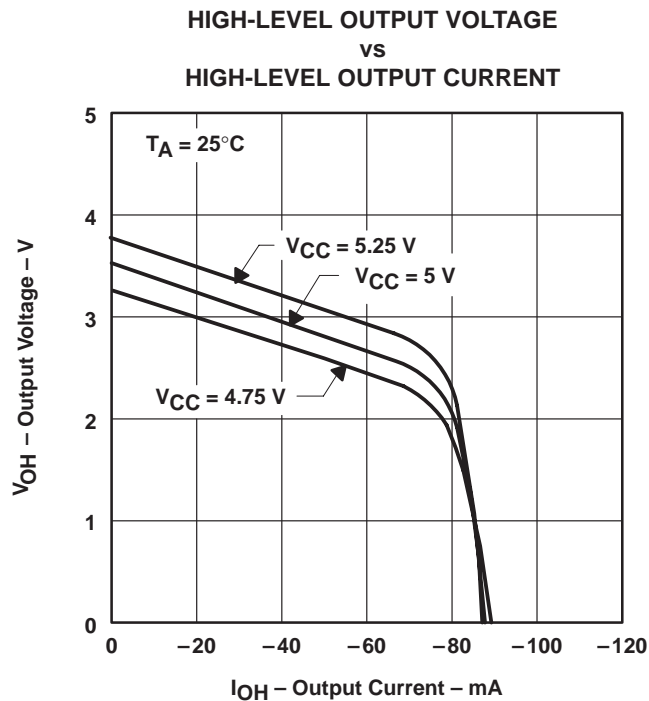
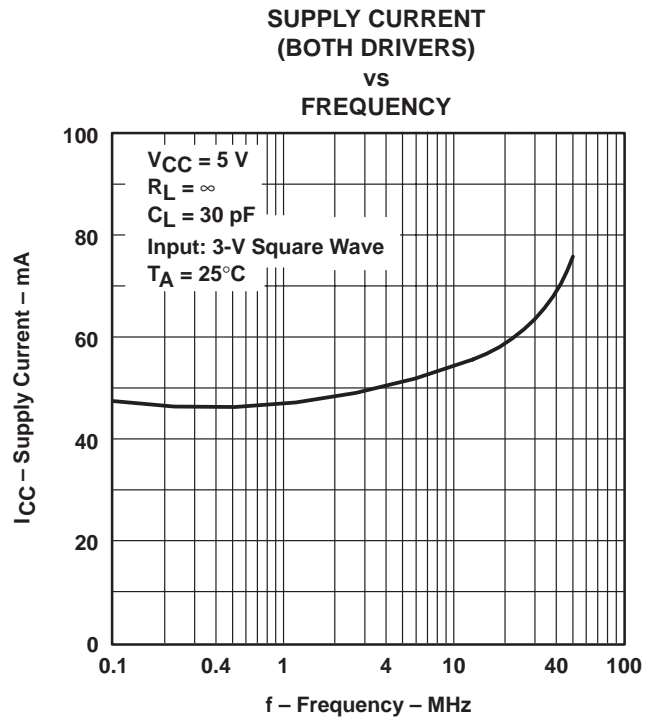
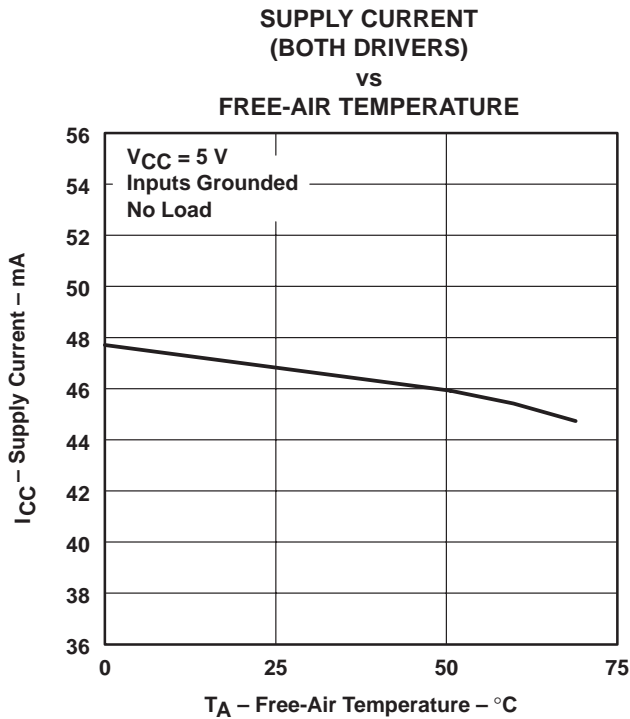
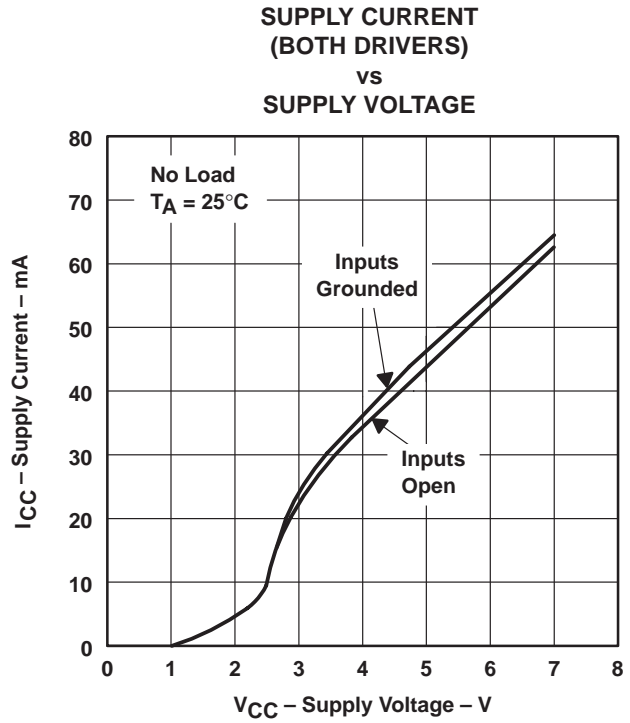
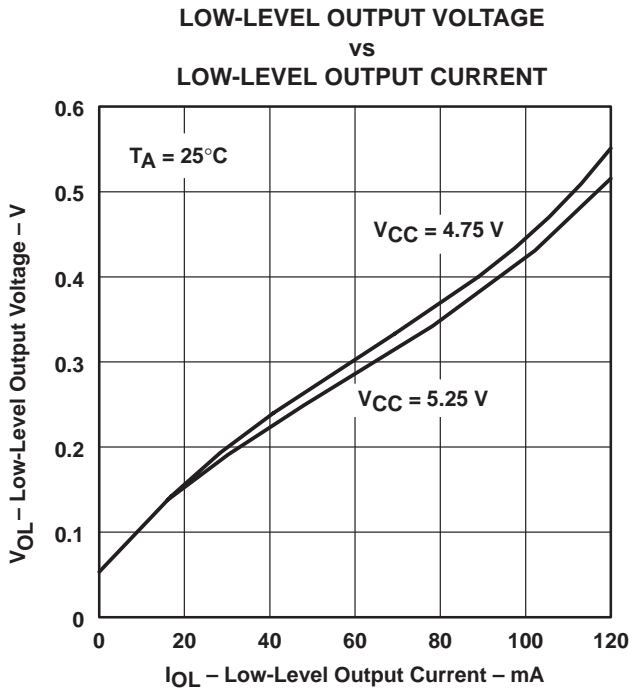


Figure 8

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

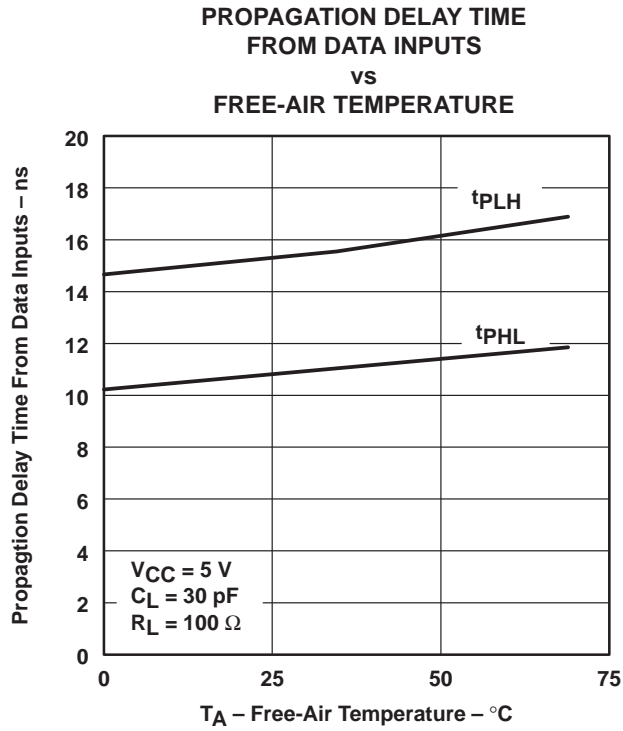


Figure 13

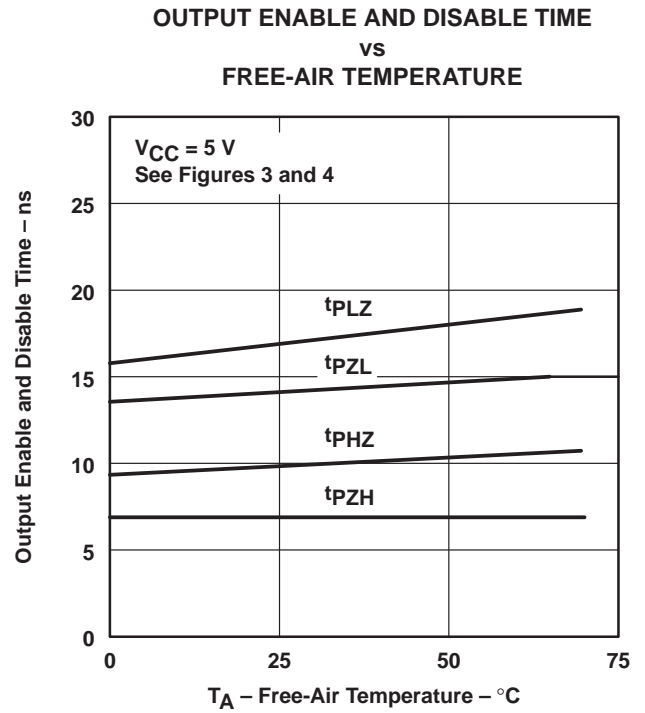


Figure 14

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN75159D | LIFEBUY | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75159 | |
| SN75159N | LIFEBUY | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75159N | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

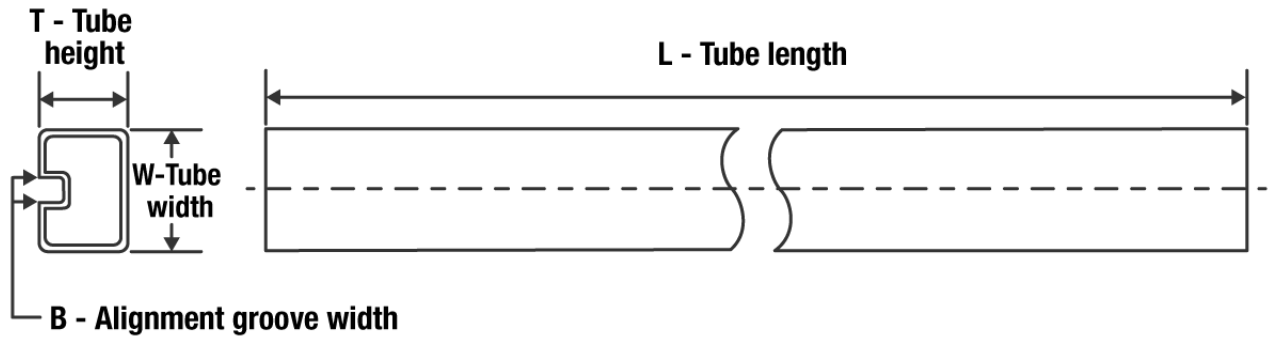
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75159D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN75159N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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