AT28C010

Military Grade 1-Mbit (131,072 x 8) Paged Parallel EEPROM

Features

- Fast Read Access Time: 120 ns
- Automatic Page Write Operation:
  - Internally organized as 131,072 x 8 (1 Mbit)
  - Internal address and data latches for 128 bytes
  - Internal control timer
- Fast Write Cycle Time:
  - Page Write cycle time: 10 ms maximum
  - 1 to 128-byte Page Write operation
- Low-Power Dissipation:
  - 80 mA active current
  - 300 µA CMOS standby current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology:
  - Endurance: 10,000 or 100,000 cycles
  - Data retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC® Approved Byte-Wide Pinout

Packages

- 32-Lead CERDIP, 32-Lead Flatpack, 32-Lead CLCC and 30-Pin PGA

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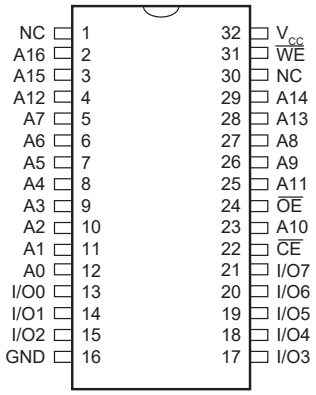
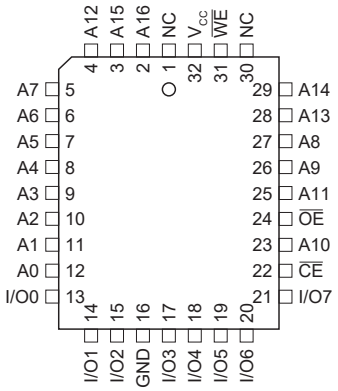
1. Package Types (not to scale)

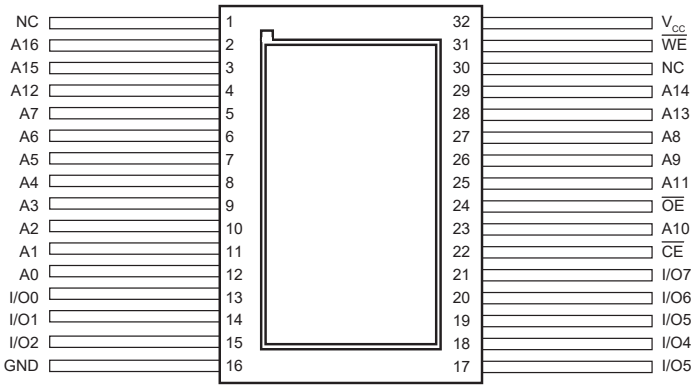
32-Lead CERDIP
Top View



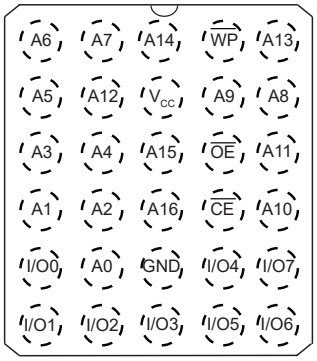
32-Lead CLCC
Top View



32-Lead FLATPACK
Top View



30-Pin PGA
Top View



2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	32-Lead CERDIP	32-Lead CLCC	32-Lead FLATPACK	30-Pin PGA	Function
NC	1	1	1	—	No Connect
A16	2	2	2	30	Address
A15	3	3	3	29	Address
A12	4	4	4	2	Address
A7	5	5	5	3	Address
A6	6	6	6	4	Address
A5	7	7	7	5	Address
A4	8	8	8	6	Address
A3	9	9	9	7	Address
A2	10	10	10	8	Address
A1	11	11	11	9	Address
A0	12	12	12	10	Address
I/O0	13	13	13	11	Data Input/Output
I/O1	14	14	14	12	Data Input/Output
I/O2	15	15	15	13	Data Input/Output
GND	16	16	16	14	Ground
I/O3	17	17	17	15	Data Input/Output
I/O4	18	18	18	16	Data Input/Output
I/O5	19	19	19	17	Data Input/Output
I/O6	20	20	20	18	Data Input/Output
I/O7	21	21	21	19	Data Input/Output
$\overline{CE}$	22	22	22	20	Chip Enable
A10	23	23	23	21	Address
$\overline{OE}$	24	24	24	22	Output Enable
A11	25	25	25	23	Address
A9	26	26	26	24	Address
A8	27	27	27	25	Address
A13	28	28	28	26	Address
A14	29	29	29	1	Address
NC	30	30	30	—	No Connect
$\overline{WE}$	31	31	31	27	Write Enable
V_{CC}	32	32	32	28	Device Power Supply

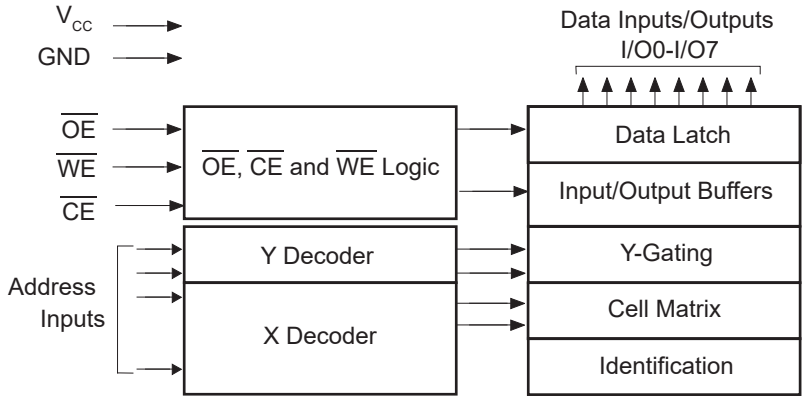
3. Description

The AT28C010 is a high-performance Electrically Erasable and Programmable Read-Only Memory (EEPROM). Its 1-Mb memory is organized as 131,072 words by 8 bits. Manufactured with Microchip's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The AT28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of EEPROM for device identification or tracking.

3.1 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages (including NC pins) with respect to ground	-0.6V to +6.25V
All output voltages with respect to ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with respect to ground	-0.6V to +13.5V

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20	AT28C010-25
Operating Temperature (Case)	Military	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Maximum	Units	Test Conditions
Input Load Current	I_{LI}	—	10	µA	V_{IN} = 0V to V_{CC} + 1V
Output Leakage Current	I_{LO}	—	10	µA	$V_{I/O}$ = 0V to V_{CC}
V_{CC} Standby Current CMOS	I_{SB1}	—	300	µA	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V
V_{CC} Standby Current TTL	I_{SB2}	—	3	mA	$\overline{CE}$ = 2.0V to V_{CC} + 1V
V_{CC} Active Current	I_{CC}	—	80	mA	f = 5 MHz; I_{OUT} = 0 mA
Input Low Voltage	V_{IL}	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	V	
Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH1}	2.4	—	V	I_{OH} = -400 µA
Output High Voltage CMOS	V_{OH2}	4.2	—	V	I_{OH} = -100 µA; V_{CC} = 4.5V

4.4 Pin Capacitance

Table 4-3. Pin Capacitance(1,2)

Symbol	Typical	Maximum	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note:

1. This parameter is characterized but is not 100% tested in production.
2. f = 1 MHz, T_A = 25°C

5. Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write is started, it will automatically time itself to completion. Once a programming operation is initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C010 allows 1 to 128 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 127 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7-A16 inputs. For each $\overline{WE}$ high-to-low transition during the page write operation, A7-A16 must be the same. The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Microchip incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways:

- V_{CC} sense – if V_{CC} is below 3.8V (typical), the write function is inhibited
- V_{CC} power-on delay – once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write
- write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles
- noise filter – pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28C010. When enabled, the software data protection (SDP) will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010 is shipped with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC}, the entire AT28C010 will be protected against inadvertent write operations. It should be noted that, once protected, the host may still perform a byte or page write to the AT28C010. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 128 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH, the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. See Software Chip Erase application note for details.

5.1 Operating Modes

Table 5-1. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(1)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(2)	X	High-Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High-Z

Note:

1. Refer to AC Programming Waveforms.
2. X can be V_{IL} or V_{IH}.

5.2 AC Read Characteristics

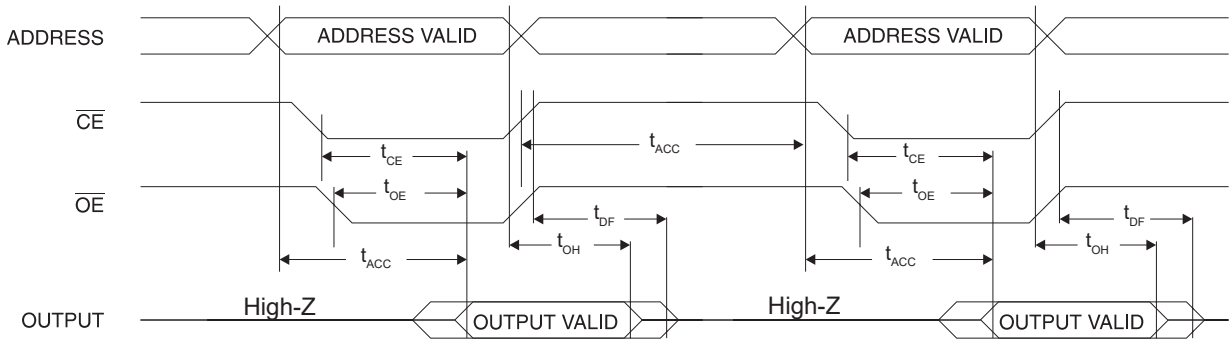
Table 5-2. AC Read Characteristics

Parameter	Symbol	AT28C010-12		AT28C010-15		AT28C010-20		AT28C010-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address to Output Delay	t_{ACC}	—	120	—	150	—	200	—	250	ns
$\overline{CE}$ to Output Delay	t_{CE}(1)	—	120	—	150	—	200	—	250	ns
$\overline{OE}$ to Output Delay	t_{OE}(2)	0	50	0	55	0	55	0	55	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float	t_{DF}(3,4)	0	50	0	55	0	55	0	55	ns
Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	t_{OH}	0		0		0		0		ns
$\overline{CE}$ Pulse High Time	t_{CEPH}(5)	50	—	50	—	50	—	50	—	ns

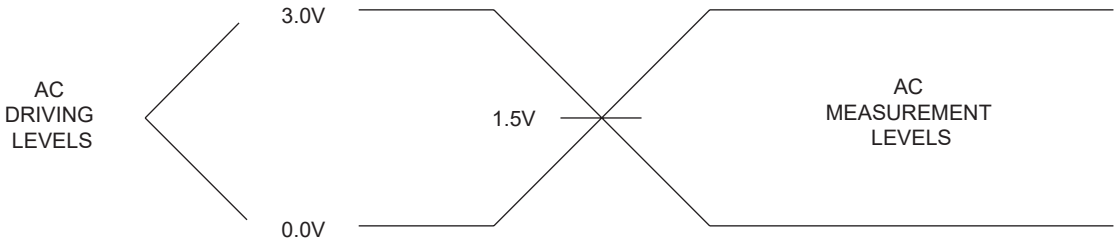
Note:

1. $\overline{CE}$ may be delayed up to t_{ACC}-t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC}-t_{OE} after an address change without impact in t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.
5. If $\overline{CE}$ is de-asserted, it must remain de-asserted for at least 50 ns during read operations, otherwise incorrect data may be read.

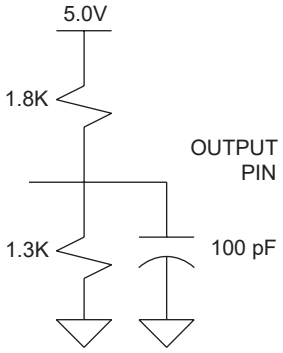
5.3 AC Read Waveforms



5.4 Input Test Waveforms and Measurement Level



5.5 Output Test Load



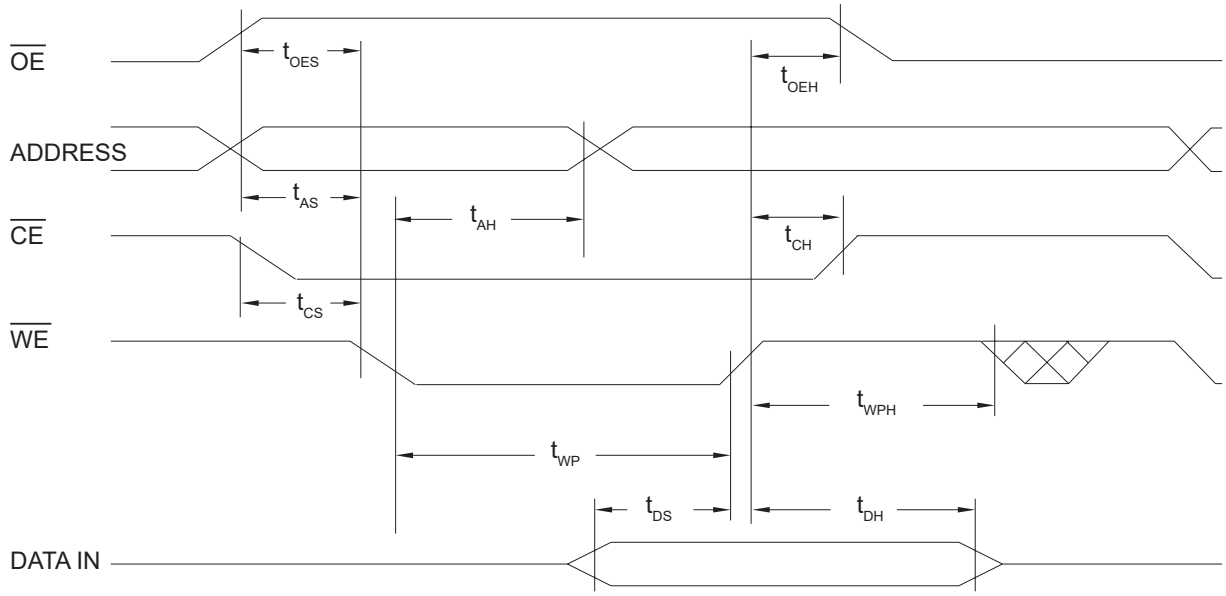
5.6 AC Write Characteristics

Table 5-3. AC Write Characteristics

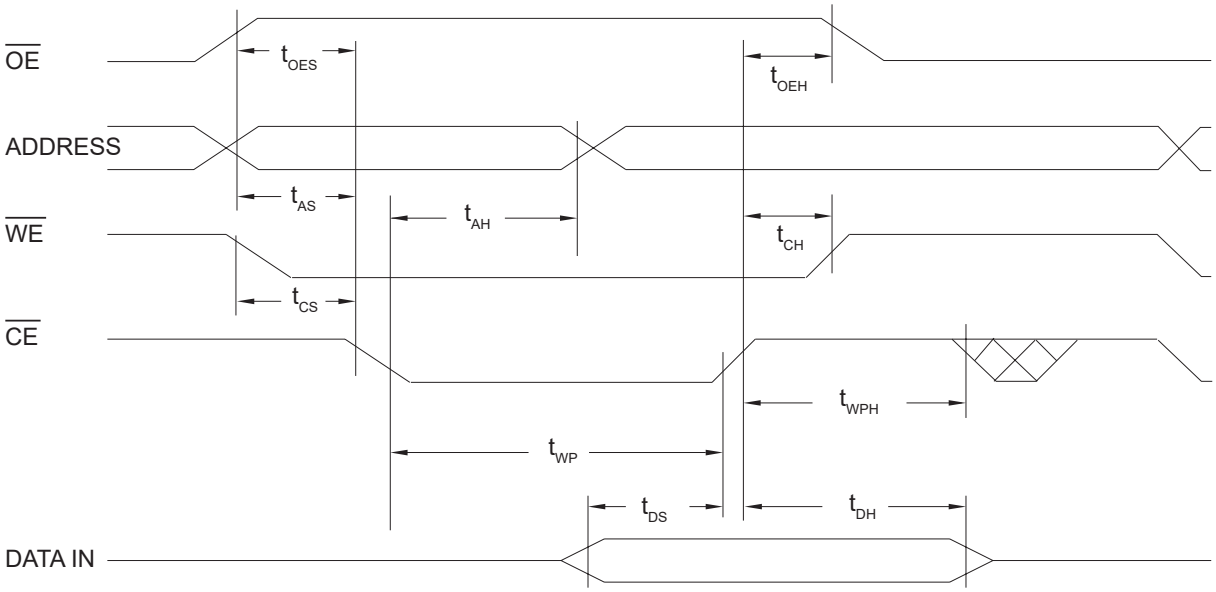
Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t_{WC}	—	10	ms
Address Set-Up Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
Data Set-Up Time	t_{DS}	50	—	ns
Data Hold Time	t_{DH}	0	—	ns
Write Pulse Width	t_{WP}	100	—	ns
Byte Load Cycle Time	t_{BLC}	—	150	µs
Write Pulse Width High	t_{WPH}	50	—	ns

5.7 AC Write Waveforms

5.7.1 $\overline{WE}$ Controlled



5.7.2 $\overline{CE}$ Controlled

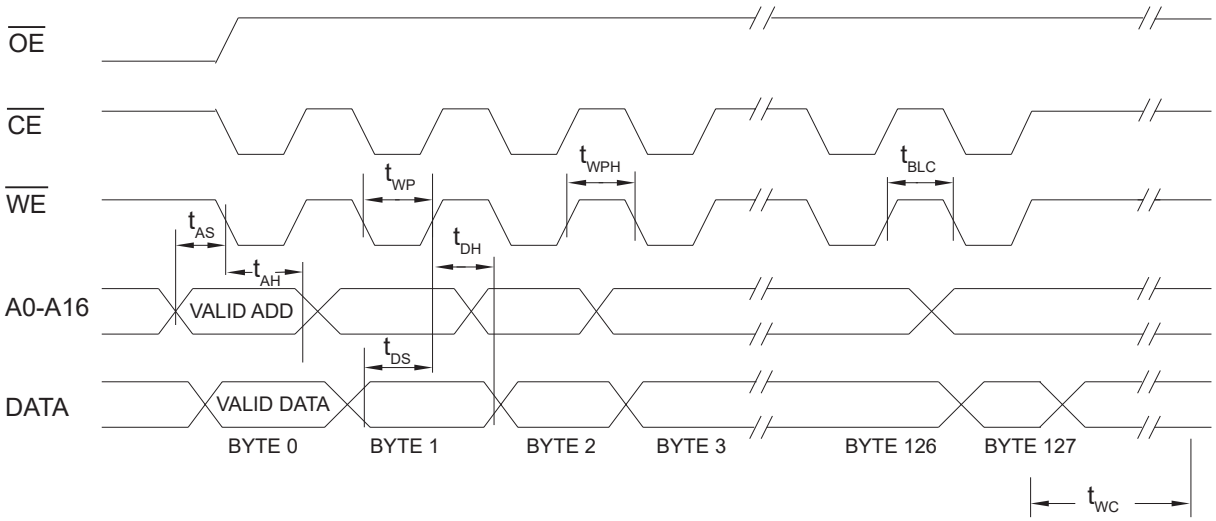


5.8 Page Mode Characteristics

Table 5-4. Page Mode Characteristics

Parameter	Symbol	Minimum	Maximum	Units
Address, $\overline{OE}$ Set-Up Time	t_{AS}, t_{OES}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
Chip Select Set-Up Time	t_{CS}	0	—	ns
Chip Select Hold Time	t_{CH}	0	—	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	t_{WP}	100	—	ns
Data Set-Up Time	t_{DS}	50	—	ns
Data, $\overline{OE}$ Hold Time	t_{DH}, t_{OEH}	0	—	ns

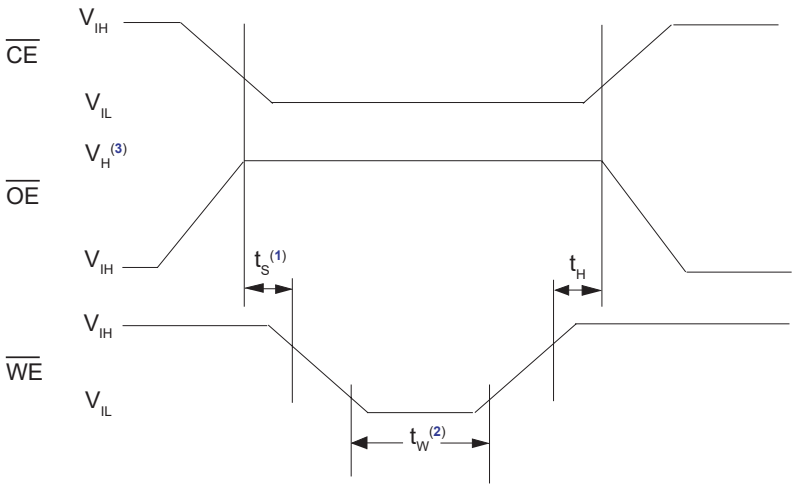
5.9 Page Mode Write Waveforms[1,2]



Note:

1. A7 through A16 must specify the page address during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

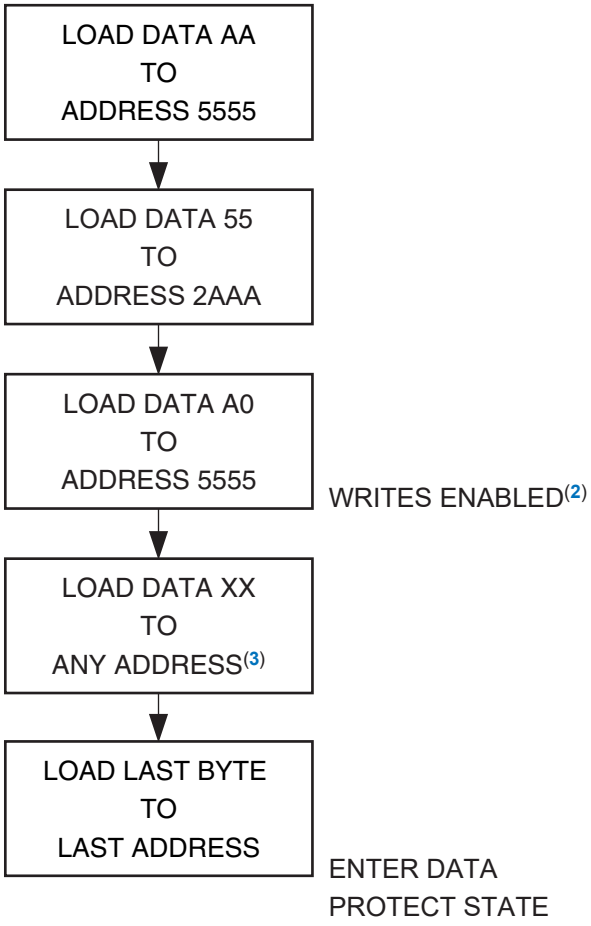
5.10 Chip Erase Waveforms



Note:

1. t_S = 5 msec (minimum)
2. $t_W = t_H$ = 10 msec (minimum)
3. V_H = 12.0V ± 0.5V

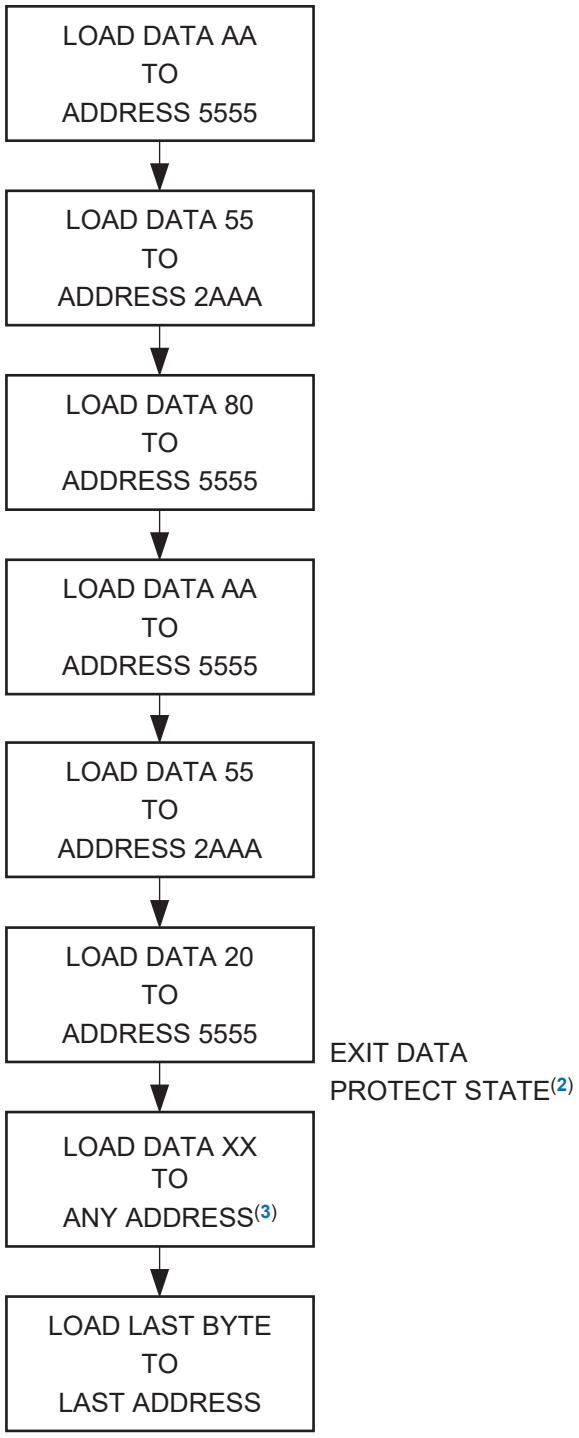
5.11 Software Data Protection Enable Algorithm[1]



Note:

1. Data format: I/O7-I/O0 (Hex); Address format: A16-A0 (Hex).
2. Write-Protect state will be activated at end of write even if no other data is loaded.
3. 1 to 128 bytes of data are loaded.

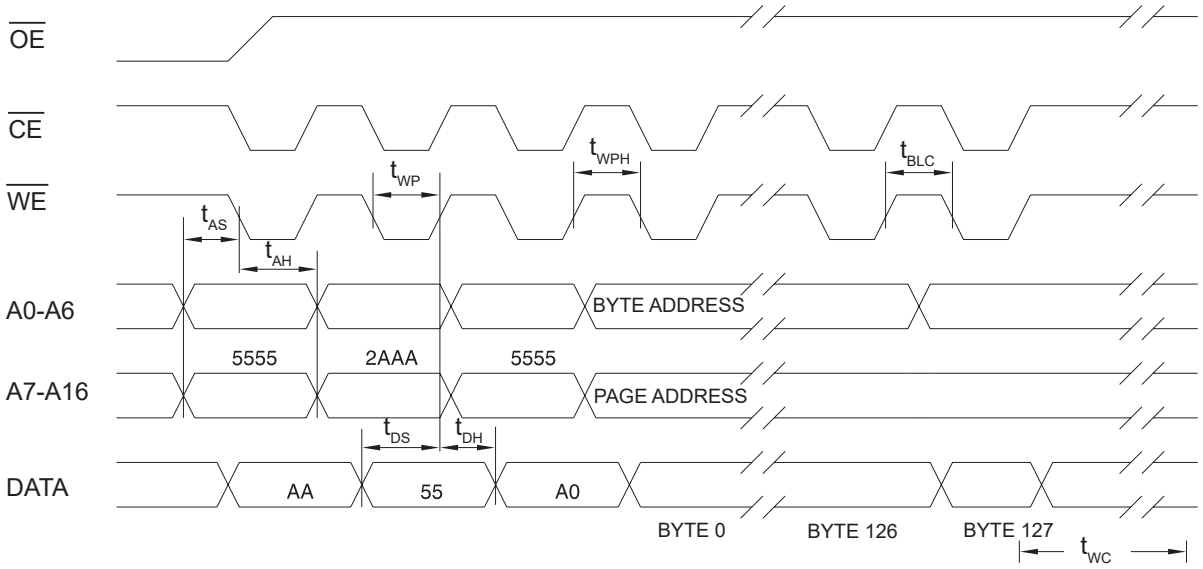
5.12 Software Data Protection Disable Algorithm[1]



Note:

1. Data format: I/O7-I/O0 (Hex); Address format: A16-A0 (Hex).
2. Write-Protect state will be deactivated at end of write period even if no other data is loaded.
3. 1 to 128 bytes of data are loaded.

5.13 Software Protected Program Cycle Waveform[1,2,3]



Note:

1. A0-A16 must conform to the addressing sequence for the first 3 bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A16) must be the same for each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

5.14 $\overline{Data}$ Polling Characteristics[1]

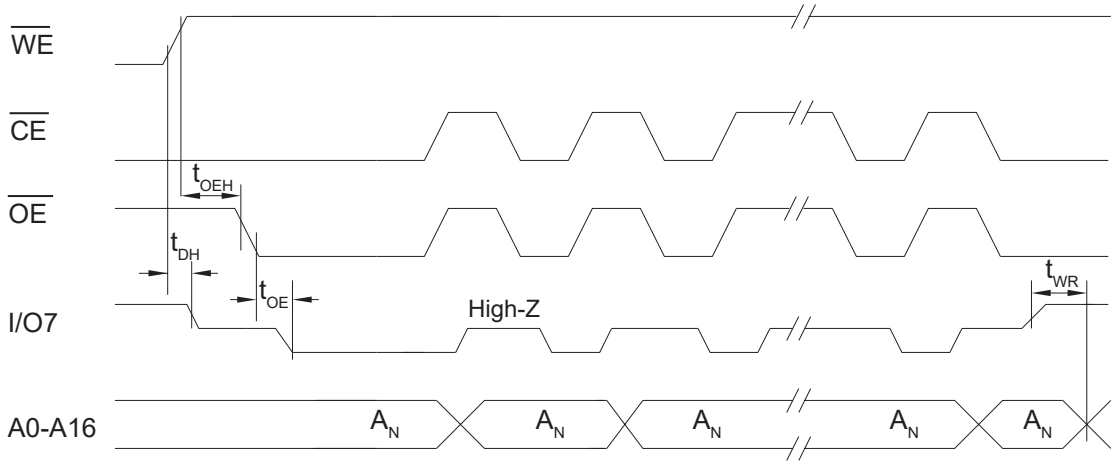
Table 5-5. Data Polling Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	10	—	—	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	—	—	ns
$\overline{OE}$ to Output Delay[2]	t_{OE}	—	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Note:

1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

5.15 $\overline{\text{Data}}$ Polling Waveforms



5.16 Toggle Bit Characteristics[1]

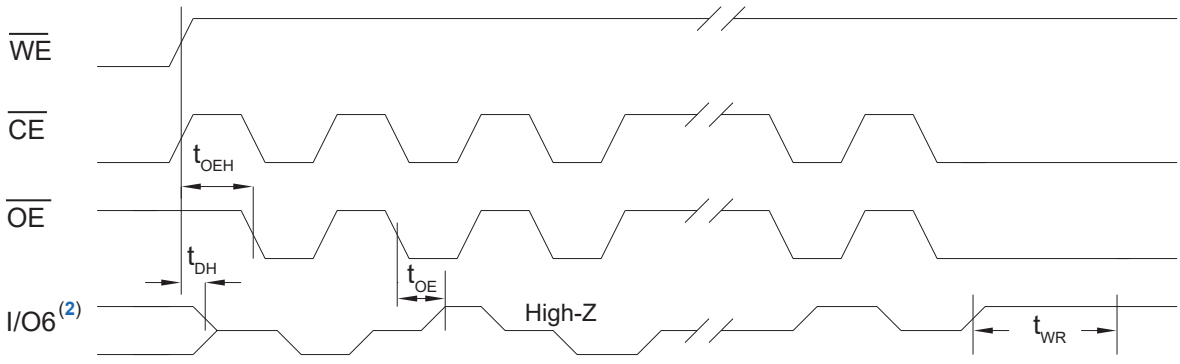
Table 5-6. Toggle Bit Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	10	—	—	ns
$\overline{\text{OE}}$ Hold Time	t_{OEH}	10	—	—	ns
$\overline{\text{OE}}$ to Output Delay[2]	t_{OE}	—	—	—	ns
$\overline{\text{OE}}$ High Pulse[2]	t_{OEHP}	150	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Note:

1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

5.17 Toggle Bit Waveforms



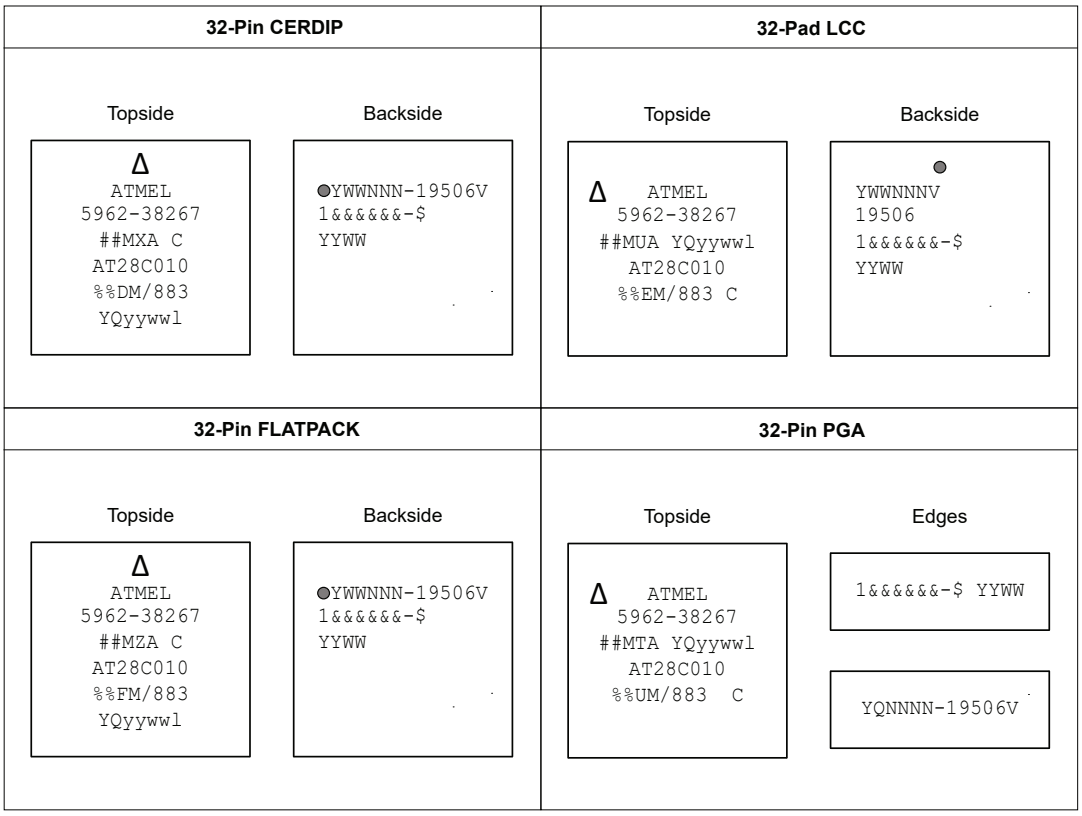
Note:

1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

6. Packaging Information

6.1 Package Marking Information

AT28C010: Package Marking Information (SMD devices)



## = Device Number	%% = Access Time		$ = Assembly Location
01: 250 ns 03: 200 ns 05: 150 ns 07: 120 ns	25: 250 ns 20: 200 ns 15: 150 ns 12: 120 ns		F: Philippines N: Thailand

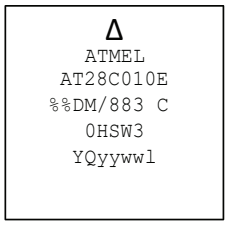
Country of Assembly	**Lot Trace Code**	**Seal Year and Work Week**
&&&&&&: Country of Assembly	YWWNNN: Lot Trace Code	YYWW: Seal Year and Work Week

Year, Quarter, Seal Year, Seal Week and Group D Coverage (Military Date Code)
YQyywwl: Year, Quarter, Seal Year, Seal Week and Group D Coverage (Military Date Code)

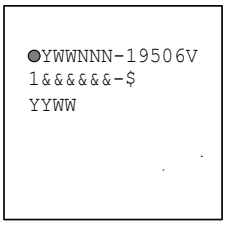
AT28C010E: Package Marking Information (Non-SMD devices)

32-Pin CERDIP

Topside

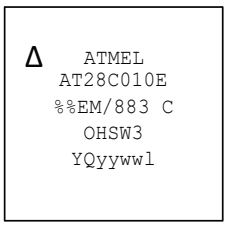


Backside

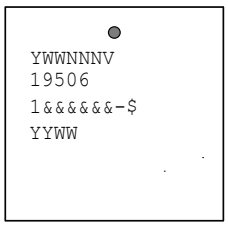


32-Pad LCC

Topside

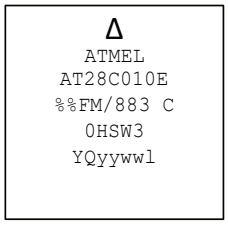


Backside

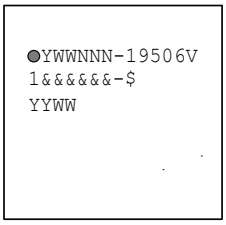


32-Pin FLATPACK

Topside

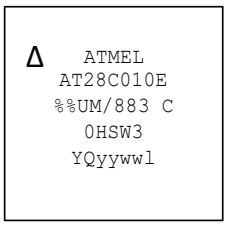


Backside

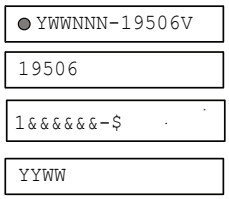


32-Pin PGA

Topside



Edges

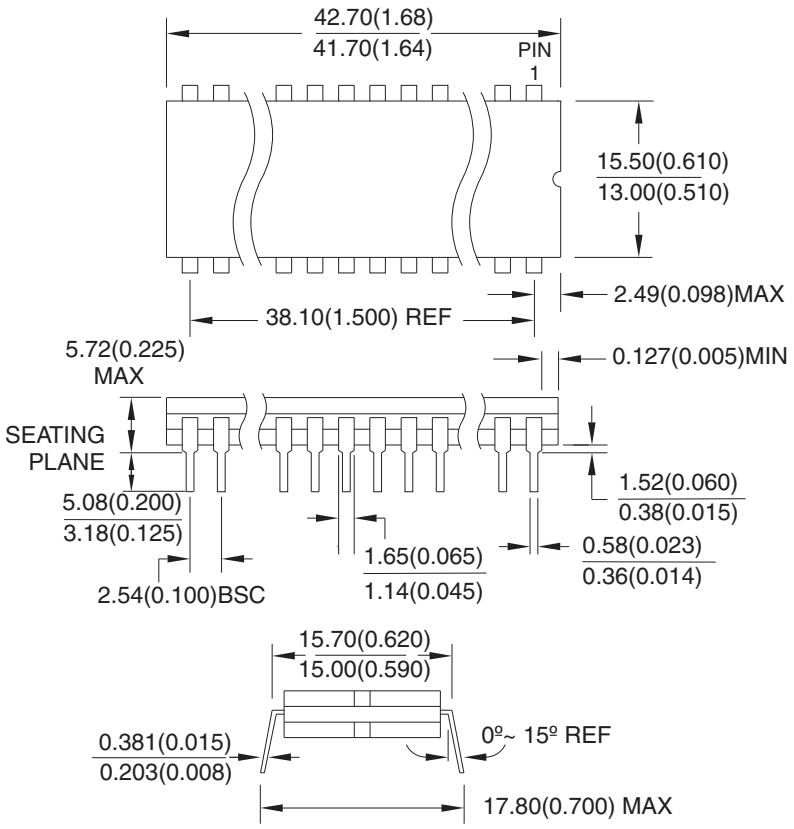


	%% = Access Time	CAGE Code	$ = Assembly Location
	25: 250 ns 20: 200 ns 15: 150 ns 12: 120 ns	0HSW3	F: Philippines N: Thailand

Country of Assembly	**Lot Trace Code**	**Seal Year and Work Week**
&&&&&&: Country of Assembly	YWWNNN: Lot Trace Code	YYWW: Seal Year and Work Week

Year, Quarter, Seal Year, Seal Week and Group D Coverage (Military Date Code)
YQyywwl: Year, Quarter, Seal Year, Seal Week and Group D Coverage (Military Date Code)

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 D-16 Config A

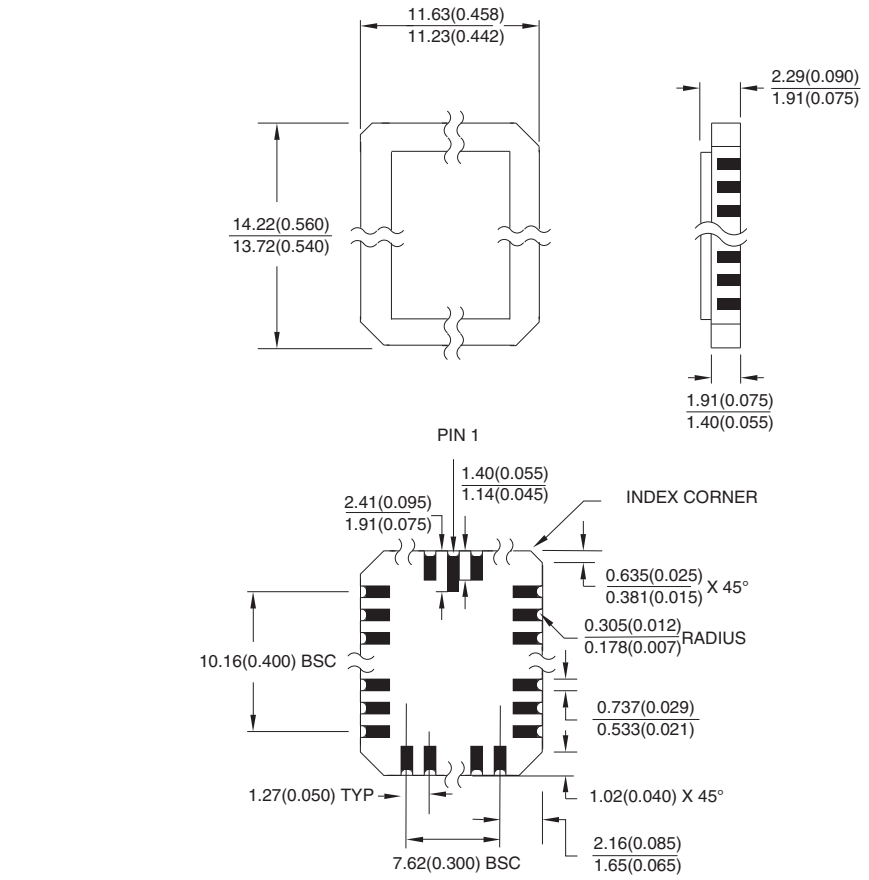


10/23/03

	TITLE	DRAWING NO.	REV.
	32D6, 32-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)	32D6	B

Note:
For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 C-12

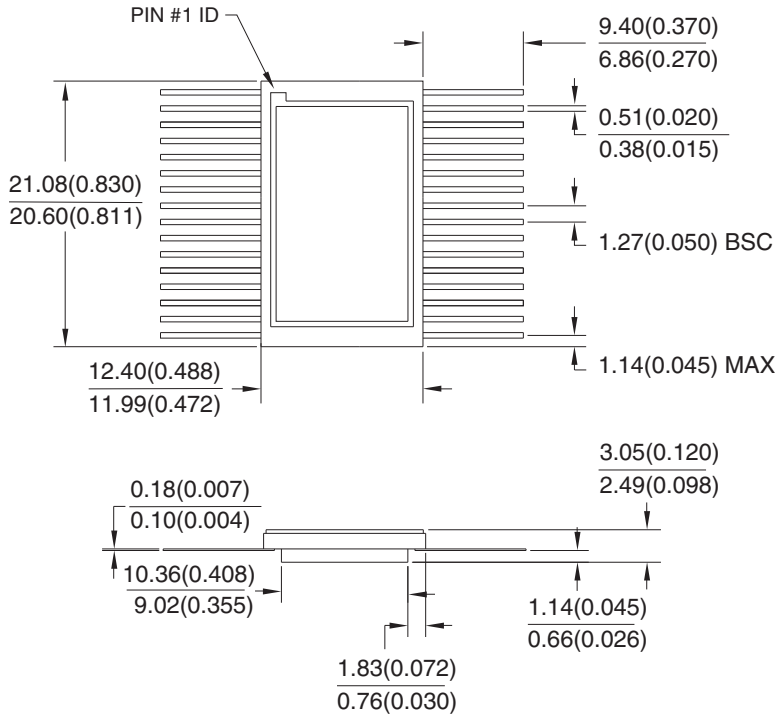


10/21/03

	TITLE	DRAWING NO.	REV.
	32L1, 32-pad, Non-windowed, Combo Lid, Leadless Chip Carrier (LCC)	32L1	B

Note:
For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
JEDEC Outline MO-115 AA

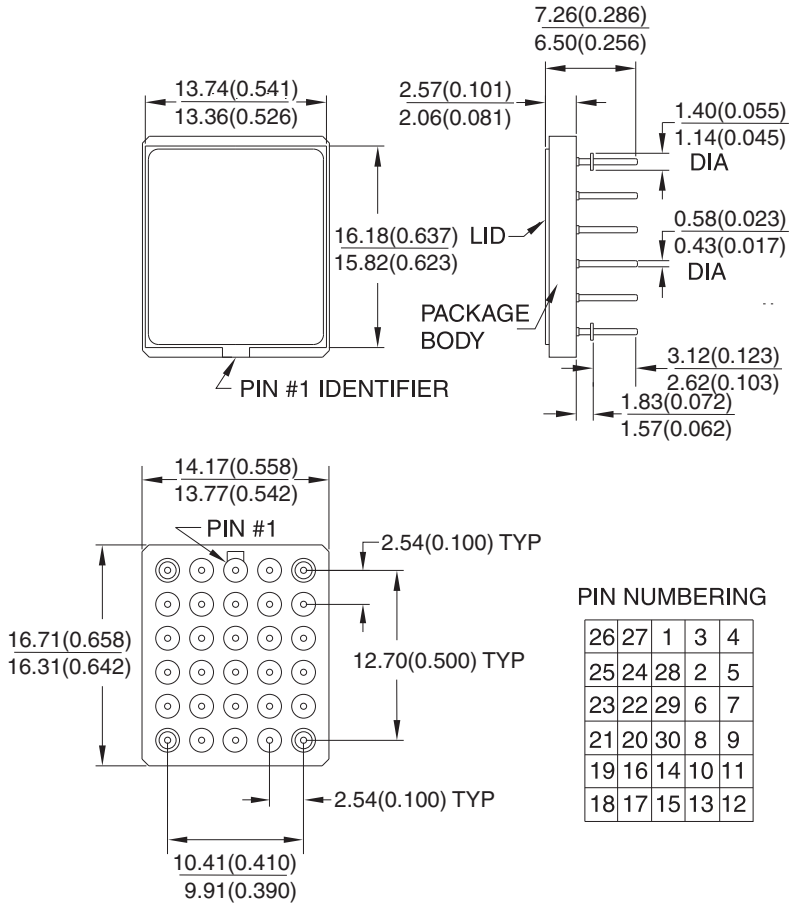


10/21/03

	TITLE	DRAWING NO.	REV.
	32F, 32-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (FlatPack)	32F	B

Note:
For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.



PIN NUMBERING

26	27	1	3	4
25	24	28	2	5
23	22	29	6	7
21	20	30	8	9
19	16	14	10	11
18	17	15	13	12

10/21/03

	TITLE	DRAWING NO.	REV.
	30U, 30-pin, Ceramic Pin Grid Array (PGA)	30U	B

Note:
For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

7. Revision History

Revision A (March 2020)
Updated to the Microchip template. Microchip DS20006311 replaces Atmel document 0010. Added updated Part Markings to include new trace code format.

Atmel Document 0010 Revision I (June 2015)
Added Revision History section. Updated AC Characteristics and ordering information.

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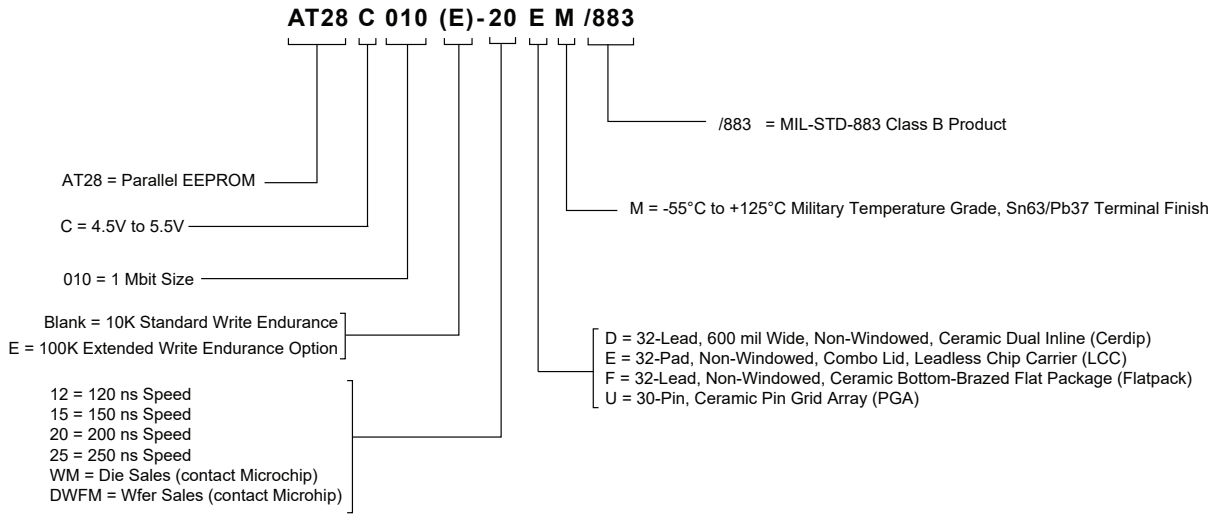

Examples

Table 11-1. AT28C010 Ordering Information

Ordering Code	Standard Military Drawing Number (SMD#)	Package Number	t_{ACC}(ns)	Operating Range
AT28C010-12DM/883	5962-38267 07 MXA	32D6	120	Military/883C Class B, Fully Compliant (-55°C to 125°C)
AT28C010-12EM/883	5962-38267 07 MUA	32L1		
AT28C010-12FM/883	5962-38267 07 MZA	32F		
AT28C010-12UM/883	5962-38267 07 MTA	30U		
AT28C010-15DM/883	5962-38267 05 MXA	32D6	150	
AT28C010-15EM/883	5962-38267 05 MUA	32L1		
AT28C010-15FM/883	5962-38267 05 MZA	32F		
AT28C010-15UM/883	5962-38267 05 MTA	30U		
AT28C010-20DM/883	5962-38267 03 MXA	32D6	200	
AT28C010-20EM/883	5962-38267 03 MUA	32L1		
AT28C010-20FM/883	5962-38267 03 MZA	32F		
AT28C010-20UM/883	5962-38267 03 MTA	30U		
AT28C010-12DM/883	5962-38267 01 MXA	32D6	250	
AT28C010-12FM/883	5962-38267 01 MZA	32F		
AT28C010-WM	None	Die Sales	Note 1	
AT28C010-DWFM	None	Wafer Sales	Note 1	

Note:

1. Contact Microchip Sales for Die and Wafer sales

Table 11-2. AT28C010E Ordering Information

Ordering Code	Standard Military Drawing Number (SMD#)	Package Number	t_{ACC}(ns)	Operating Range
AT28C010E-12DM/883	None	32D6	120	Military/883C Class B, Fully Compliant (-55°C to 125°C)
AT28C010E-12EM/883	None	32L1		
AT28C010E-12FM/883	None	32F		
AT28C010E-12UM/883	None	30U		
AT28C010E-15DM/883	None	32D6	150	

Package Types	
32D6	32-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline (Cerdip)
32F	32-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32L1	32-Pad, Non-Windowed, Combo Lid, Leadless Chip Carrier (LCC)
30U	30-Pin, Ceramic Pin Grid Array (PGA)
WM	Diced Die Military
DWFM	Die in Wafer Form Military
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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