Brief Description

The SAP5S/SAP51 is a next-generation CMOS integrated circuit for AS-Interface networks. This low-level field bus AS-i (Actuator Sensor Interface) was designed for easy, safe, and cost-effective interconnection of sensors, actuators, and switches. It transports both power and data over the same two-wire unshielded cable.

The SAP5S/SAP51 is used as part of a master or slave node and functions as an interface to the physical bus. It provides the power supply, physical data transfer, and communication protocol handling. The SAP5S/SAP51 is fully compliant with the *AS-Interface Complete Specification V3.0*. It is function and pin compatible with the SAP4.1 (AS2702).

The SAP5S/SAP51 can be programmed by the user to operate in Standard Slave Mode, Safety Mode (SAP5S only), or Master Mode. The special AS-i Safety Mode (SAP5S only) assures short response times regarding security-related events.

All configuration data are stored in an internal EEPROM that can be easily programmed by a stationary or handheld programming device.

The SAP5S/SAP51 is optimized for harsh environments by its special burst protection circuitry and excellent electromagnetic compatibility.

Features

- Compliant with the *AS-Interface Complete Specification V3.0*
- Universal application: slaves, masters, repeaters
- Integrated safety code generator (SAP5S only)
- On-chip electronic inductor: 55mA current drive capability
- Two LED outputs to support all *AS-Interface Complete Specification V3.0* status indication modes
- User programmable to operation in Standard Slave Mode, Safety Mode, or Master Mode
- Supports 5.33 and 16 MHz crystals by automatic frequency detection
- Data pre-processing functions
- Clock and communication watchdogs for high system security

Benefits

- Cost savings due to integrated Safety Code Generator (SAP5S only)
- Special burst protection circuitry
- Excellent electromagnetic compatibility

Physical Characteristics

- Operational temperature range: -25 to +85°C
- SOP16 and SOP20 package

Available Support

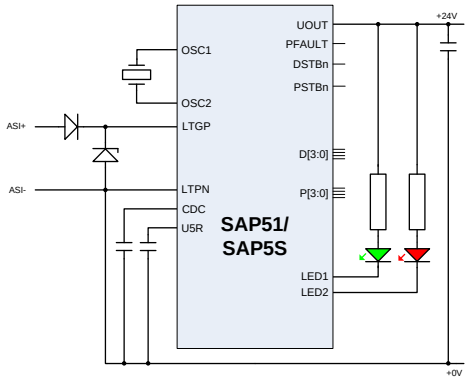
- IDT AS-Interface Programmer Kit USB
- IDT SAP5 Evaluation Board V2.0

Related Products

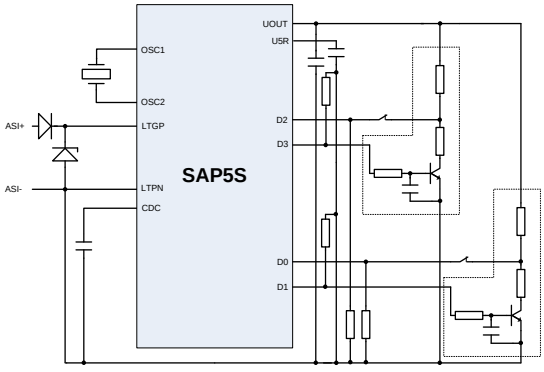
- ASI4U Universal AS-Interface IC

SAP5S/SAP51 Basic Application Circuits

Standard Application



Safety Mode Slave Application



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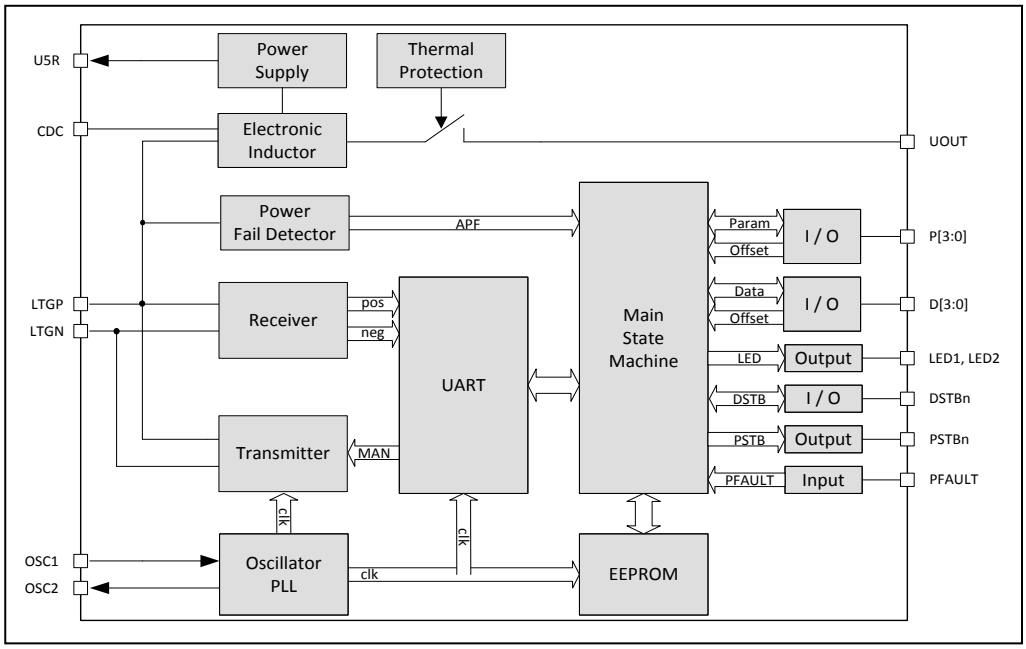
SAP5S/SAP51 Block Diagram



Typical Applications

- AS-i Master Modules
- AS-i Slave Modules
- AS-i Safety Modules (SAP5S only)

Ordering Information

Ordering Code	Operating Temperature	Package Type	RoHS?	Packaging
SAP5SD-A-G1-T SAP51D-A-G1-T	-25°C to +85°C	SOP20 / 300 mil	Yes	Tubes (37 parts/tube)
SAP5SD-A-G1-R SAP51D-A-G1-R	-25°C to +85°C	SOP20 / 300 mil	Yes	Tape and Reel (1000 parts/reel)
SAP5SD-B-G1-T SAP51D-B-G1-T	-25°C to +85°C	SOP16 / 300 mil	Yes	Tubes (46 parts/tube)
SAP5SD-B-G1-R SAP51D-B-G1-R	-25°C to +85°C	SOP16 / 300 mil	Yes	Tape and Reel (1000 parts/reel)

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1 Please Read this First

1.1. Important Notice

Important Safety Notice: This IDT product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support, or life-sustaining equipment, are specifically not recommended without additional mutually agreed upon processing by IDT for such applications.

1.2. Silicon Revision History

Revision	Date	Technical Changes	Affected Page in Datasheet
B	September 2005	First marketed silicon version.	
C	March 2007	Modified I_{IL} – current range for input low level.	Table 5.5 on Page 28
C	March 2007	Modified Delay Mode activation through parameter port P1.	Page 33
C	March 2007	Modified Synchronous Data I/O Mode activation through parameter port P2.	Page 35
C	March 2007	Modified Watchdog activation through parameter port P0.	Page 46
C	March 2007	Improved burst protection filter and improved ESD behavior.	
D	August 2012	UART design corrections for End_Bit transmission error detection. Improved AS-i telegram pause detection.	

2 General Device Specification

Important note: The *absolute maximum ratings* given in section 2.1 are stress ratings only. The SAP5 might not function or be operable above the *recommended operating conditions* given in section 2.2. Stresses exceeding the *absolute maximum ratings* might also damage the device. In addition, extended exposure to stresses above the *recommended operating conditions* might affect device reliability. IDT does not recommend designing to the specifications given under “Absolute Maximum Ratings.”

Important note: The *operating conditions* given in section 2.2 set the conditions over which IDT specifies device operation. These are the conditions that the application circuit should provide to the device for it to function as intended. Unless otherwise noted, the limits for parameters that appear in the *operating conditions* section are used as test conditions.

2.1. Absolute Maximum Ratings (Non-operating)

Table 2.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage reference	V_{LTGN}	0	0	V
Voltage difference [1] between LTGP and LTGN pins (V_{LTGP} - V_{LTGN})	$V_{LTGP-LTGN}$	0	40	V
Pulse voltage [2, 3] between LTGP and LTGN (V_{LTGP} - V_{LTGN})	$V_{LTGP-LTGN\_P}$	0	50	V
Voltage at the CDC, D0, D1, D2, D3, P0, P1, P2, P3, DSTBn, PSTBn, LED1, LED2, PFAULT, and UOUT pins	$V_{inputs1}$	-0.3	V_{UOUT}+ 0.3	V
Voltage at the OSC1, OSC2, U5R pins	$V_{inputs2}$	-0.3	7	V
Input current into any pin except supply pins [4]	I_{in}	-50	50	mA
Humidity – non-condensing [5]	H			
Electrostatic discharge [6] – Human Body Model (HBM2)	V_{HBM}	1500		V
Electrostatic discharge [7] – Equipment Discharge Model (EDM)	V_{EDM}	200		V
Storage temperature	T_{STG}	-55	125	°C
Soldering temperature Sn/Pb [8]	T_{lead}		240	°C
Soldering temperature 100%Sn [8]	T_{lead}		260	°C
Thermal resistance of SOP 16 package [9]	R_{thj-16}	80	100	K/W
Thermal resistance of SOP 20 package [9]	R_{thj-20}	75	95	K/W

1) Reverse polarity protection must be performed externally.

2) $V_{LTGP-LTGN}$ and $V_{LTGP-LTGN\_P}$ must not be violated.

3) Pulse with ≤ 50µs, repetition rate ≤ 0.5 Hz.

4) Latch-up resistance, reference pin is 0V.

5) Level 4 according to JEDEC-020D is guaranteed.

6) HBM: C = 100pF charged to VHBM2 with resistor R = 1.5kΩ in series, valid for all pins except LTGP-LTGN.

7) EDM: C = 200pF charged to VEDM with no resistor in series, valid for LTGP-LTGN only.

8) Soldering must comply with the JEDEC-J-STD-020D standard.

9) Single layer board, P_{tot} = 0.5W; air velocity = 0m/s ⇒ max. value; air velocity = 2.5m/s ⇒ min. value.

2.2. Operating Conditions

Table 2.2 Operating Conditions

Parameter	Symbol	Conditions	Min	Max.	Unit
Negative supply voltage	V_{LTGN}		0	0	V
DC voltage at LTGP pin [1), 2)]	V_{LTGP}	Relative to V_{LTGN}	16	34	V
Operating current	I_{LTGP}	V_{LTGP} = 30V f_c = 16.000MHz No load at any pin; transmitter is turned off; digital state machine is in idle state.		6	mA
Max. output sink current at pins D[3:0], DSTBn	I_{CL1}			10	mA
Max. output sink current at pins P[3:0], PSTBn	I_{CL2}			10	mA
Ambient operating temperature range	T_{amb}		-25	85	°C

1) Below $V_{LTGPmin}$ the power supply block might not be able to provide the specified output currents at UOUT and U5R.

2) Outside of these limits, the send current shape and send current amplitude cannot be guaranteed.

Table 2.3 Crystal Frequency

Parameter	Symbol	Conditions	Nominal	Unit
Crystal frequency [1)]	f_c		5.333 or 16.000	MHz

1) The SAP5 automatically detects whether the crystal frequency is 5.333MHz or 16.000MHz and controls the internal clock circuit accordingly.

2.3. EMC Behavior

The SAP51/SAP5S fulfills the requirements defined in *AS-Interface Complete Specification V3.0* and related test requirements for AS-Interface slave ICs. In addition to the *AS-Interface Complete Specification* and in combination with a reference component circuit, the SAP51/SAP5S achieves a communication failure rate less than 10% of the allowed failure rate according to the "Fast Transient" test method specified in the related AS-Interface association test procedures. The behavior specified above is correct by design and is proven during SAP51/SAP5S characterization.

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2.4. Quality Standards

The quality of the SAP51/SAP5S will be ensured according to the IDT quality standards. IDT is a qualified supplier according to ISO/TS 16949:2002 and ISO 14001:1996.

The following IDT reference documents apply for the development process (available on request; see section 9):

- *Management Regulation: 0410 Product Development Procedure*
- *Process Specification: IDT C7D 0.6µm Technology*

Functional device parameters are valid for the device operating conditions specified in section 2.2. Production device tests are performed within the recommended ranges of V_{LTGP} - V_{LTGN}, T_{amb} = +25°C (+85°C and -25°C on sample basis only) unless otherwise stated.

2.5. Failure Rate

Symbol	Parameter	Max.	Unit
AQL	Acceptance Quality Level	0.1	%
F55	Failure Rate at 55°C	18	FIT
F70	Failure Rate at 70°C	60	FIT
F85	Failure Rate at 85°C	150	FIT
F125	Failure Rate at 125°C	1400	FIT

2.6. Humidity Class

Level 3 humidity tolerance according to JEDEC-020D is guaranteed.

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3 Basic Functional Description

Note: Unless otherwise noted, the product name SAP5 refers to both the SAP51 and the SAP5S.

The SAP5 is a low-level field bus IC designed for AS-i (Actuator Sensor Interface), which provides a secure interconnection for sensors, actuators, and switches via a two-wire unshielded cable.

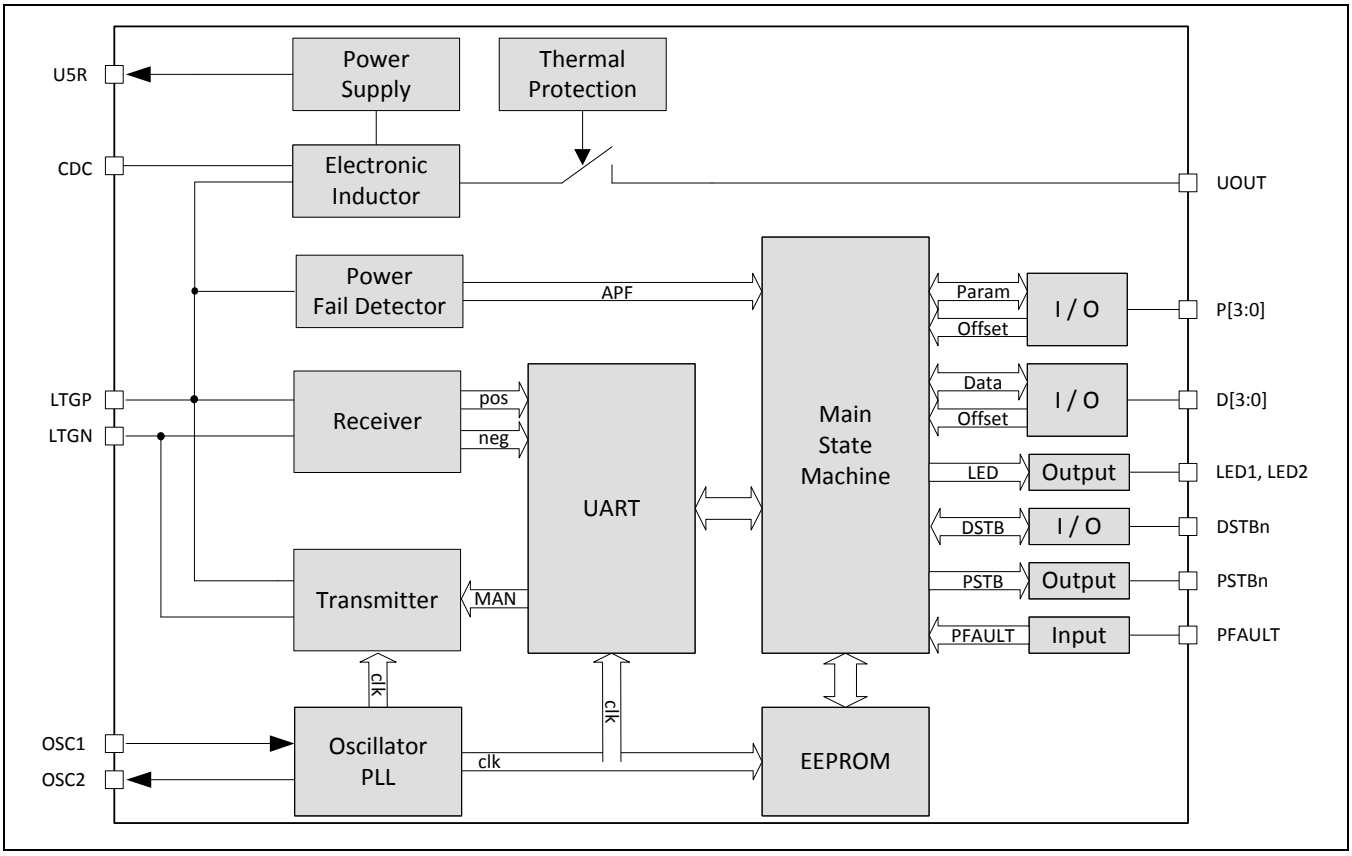
The SAP5 is used as part of a master or slave node and functions as an interface to the physical bus. It provides the power supply, physical data transfer, and communication protocol handling. The SAP5 can be programmed by the user to operate in Standard Slave Mode, Safety Mode (SAP5S only), or Master Mode. The special AS-i Safety Mode (SAP5S only) assures short response times regarding security-related events.

Configuration data are stored in a programmable internal EEPROM.

The SAP5 is optimized for harsh environments by its special burst protection circuitry and excellent electro-magnetic compatibility.

3.1. Functional Block Diagram

Figure 3.1 Functional Block Diagram



Following device functions are handled by the different blocks of the SAP5:

RECEIVER

The RECEIVE block converts the analog telegram waveform from the AS-i bus to a digital pulse-coded signal that can be processed further by a digital UART circuit.

The RECEIVE block is directly connected to the AS-i line pins LTGP and LTGN. It converts the differential AS-i telegram to a single-ended signal and removes the DC offset by high-pass filtering. To adapt quickly to changing signal amplitudes in telegrams from different network users, the amplitude of the first telegram pulse is measured by a 3-bit flash ADC and the threshold of a positive and a negative comparator is set accordingly to about 50% of the measured level. The comparators generate the *p_pulse* and *n_pulse* signals.

TRANSMITTER

The transmit block transforms a digital response signal to a correctly shaped send current signal, which is applied to the AS-i bus. Due to the inductive network behavior of the network, the changing send current induces voltage pulses on the network line that overlay the DC operating voltage. The voltage pulses must have $\sin^2$-wave shapes; therefore the send current shape must follow the integral of the $\sin^2$-wave function.

UART / MAIN STATE MACHINE / EEPROM

EEPROM write access and other I/O operations of the Main State Machine are supported in Slave Mode only (see the description of the general SAP5 operational modes below). In Master Mode, the SAP5 is basically equivalent to a physical layer transceiver.

If Slave Mode is activated, the UART demodulates the received telegrams, verifies telegram syntax and timing, and controls a register interface to the Main State Machine. After reception of a correct telegram, the UART generates appropriate Receive Strobe signals, which tell the Main State Machine to start further processing. The Main State Machine decodes the telegram information and starts respective I/O processes or EEPROM access. A second register interface is used to send data back to the UART for construction of a telegram response. The UART modulates the response data into a Manchester-II-coded bit stream that is used to control the TRANSMITTER unit.

ELECTRONIC INDUCTOR

The electronic inductor is basically a gyrator circuit. It provides an inductive behavior between the SAP5 pins LTGP and UOUT while the inductance is controlled by the capacitor on the CDC pin. The inductor decouples the power regulator of the SAP5 as well as the external load circuit from the AS-i bus and hence prevents crosstalk or switching noise from disturbing the telegram communication on the bus.

The *AS-Interface Complete Specification* describes the input impedance behavior of a slave module via an equivalent circuit that consists of R, L, and C in parallel. For example, a slave module in Extended Address Mode must have R > 13.5kΩ, L > 13.5mH, and C < 50pF. The electronic inductor of the SAP5 delivers values that are well within the required ranges for output currents up to 55mA (V_{LTGP}>24V). More detailed parameters can be found in section 5.1.

The electronic inductor requires an external capacitor of 10µF at the UOUT pin for stability.

POWER SUPPLY

The power supply block consists of a band-gap referenced 5V-regulator as well as other reverence voltage and bias current generators for internal use. The 5V regulator requires an external capacitor at pin U5R of at least 100nF for stability. It can source up to 4mA for external use, however the power dissipation and the resulting device heating become a major concern if too much current is drawn from the regulator. See section 5.1.

OSCILLATOR / PLL	The oscillator supports direct connection of 5.333MHz or 16.000MHz crystals with a dedicated load capacity of 12pF and parasitic pin capacities of up to 8pF. The SAP5 automatically detects the oscillation frequency of the connected crystal and controls the internal clock generator circuit accordingly. After power-on reset, the SAP5 is set to 16.000MHz operation by default. After about 200µs, it will either switch to 5.333MHz operation or remain in the 16.000 MHz mode. The frequency detection is active until the first AS-i telegram has been successfully received in order to ensure the SAP5 has found the correct clock frequency setting. The detection result is locked thereafter to increase resistance against burst or other interferences. The oscillator unit also contains a Clock Watchdog circuit that can generate an unconditioned SAP5 reset if there has been no clock oscillation for more than approximately 20µs. This is to prevent unpredicted SAP5 behavior if the clock signal is lost.
THERMAL PROTECTION	The SAP5 is self-protected against thermal overload. If the silicon die temperature rises above approximately 140°C for more than 2 seconds, the SAP5 detects thermal overheating, switches off the electronic inductor, performs an SAP5 reset, and sets all analog blocks to power-down mode. The 5V regulator is also turned off in this state; however, there will still remain a voltage of approximately 3 to 3.5 V available at U5R that is derived from the internal start circuitry. If the over-temperature condition is no longer present, the SAP5 resumes operation and performs an initialization.
POWER FAIL DETECTOR	The POWER FAIL DETECTOR observes the voltage at the AS-i line. It signals at the PSTBn/APF pin when the voltage drops below approximately 22.5V. This is active in Master Mode only.
INPUT STAGE	All digital inputs, except the oscillator pins, have high voltage capabilities and pull-up features. For more details see sections 5.3, 5.7, 5.8 and 7.1.
OUTPUT STAGE	All digital output stages, except the oscillator pins, have high voltage capabilities and are implemented as NMOS open-drain buffers. Each pin can sink up to 10mA of current. See section 5.4.

3.2. General Operational Modes

The SAP5 provides two operational modes: Slave Mode and Master/Repeater Mode. The operational mode that becomes active is defined by programming the flag *Master_Mode* in the Firmware Area of the EEPROM (also see Table 4.2). The EEPROM is read out at every initialization of the SAP5. Online mode switching is not provided. The configurations in Table 3.1 apply:

Table 3.1 Assignment of Operational Modes

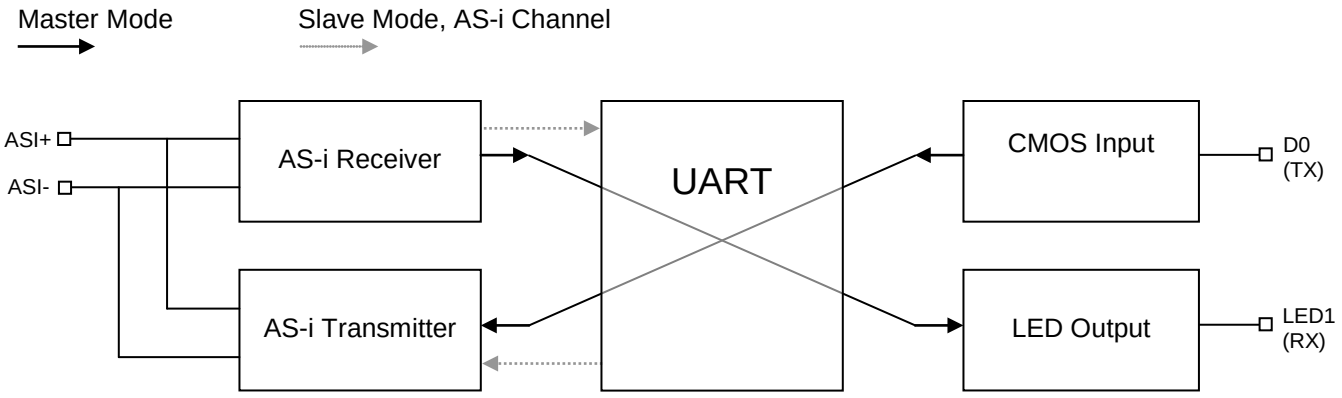
Selected Operational Mode	Master Mode Flag
Slave Mode	0
Master/Repeater Mode	1

In Slave Mode, the SAP5 operates as a fully featured AS-i slave IC according to *AS-Interface Complete Specification v3.0*.

In Master/Repeater Mode, the SAP5 acts as physical layer transceiver. It translates a digital output signal from the external master control logic (e.g., programmable logic controller (PLC), microprocessor, etc.) to a correctly shaped, analog AS-i pulse sequence and vice versa. Every AS-i telegram received is checked for consistency with the AS-i communication protocol specifications and if no errors were found, an appropriate Receive Strobe signal is generated.

Figure 3.2 shows the different data path configurations.

Figure 3.2 Data Path in Master and Repeater Modes



More detailed signal descriptions can be found in sections 5.19 and 5.14.

3.2.1. Slave Mode

The Slave Mode is the most complex operational mode of the SAP5. The SAP5 supports not only all mandatory AS-i slave functions but also a variety of additional features that facilitate the design of AS-i slave modules.

3.2.2. AS-i Communication Channel

The AS-i channel is directly connected to the AS-i bus via the pins LTGP and LTGN. A receiver and a transmitter unit are connected in parallel to the pins, which allows fully bi-directional communication through LTGP and LTGN.

3.2.3. Parameter Port Pins

In the 20-pin package, the SAP5 features a 4-bit wide parameter port (P0, P1, P2, and P3 pins) and a related parameter strobe signal pin PSTBn. *AS-Interface Complete Specification V3.0* newly defines a bidirectional mode for parameter data. The SAP5 supports this feature, which can be activated by special EEPROM setting (*IO_Code*, see section 5.9).

There is a defined phase relation between a parameter output event, the parameter input sampling, and the activation of the PSTBn signal. Therefore it can be used to trigger external logic or a microcontroller to process the received parameter data or to provide new input data for the AS-i slave response.

See section 5.7 for further details.

3.2.4. Data Port Pins

The SAP5 provides a 4-bit wide data port. The outputs work independently from each other allowing a maximum of 4 output devices to be connected to the SAP5. The directions of the Data Port pins are set through the *IO_Code*, see section 5.9.

The data port is accompanied by the data strobe signal DSTBn. There is a defined phase relation between a data output event, the input data sampling and the activation of the DSTBn signal. Thus, it can be used to trigger external logic or a microcontroller to process the received data or to provide new input data for the AS-i slave response. See section 5.8 for further details.

3.2.5. Data Input Inversion

By default, the logic signal (HIGH/LOW) that is present at the data input pins during the input sampling phase is transferred without modification to the send register, which is interfaced by the UART. Thus, the signal becomes directly part of the slave response.

Some applications work with inverted logic levels. To avoid additional external inverters, the input signal can be inverted by the SAP5 before transferring it to the send register. The inversion of the input signals can be done jointly for all data input pins. See section 5.8.

3.2.6. Data Input Filtering

To prevent input signal bouncing from being transferred to the AS-i master, the data input signals can be digitally filtered. Activation of the filter is done jointly either by EEPROM configuration or by the logic state of parameter port pin P2. For more detailed information, refer to section 5.8.

3.2.7. Synchronous Data I/O Mode

AS-Interface Complete Specification V3.0 newly defines a synchronous data I/O feature, which allows a number of slaves in the network to switch their outputs at the same time and to have their inputs sampled simultaneously. This feature is especially useful if more than 4-bit wide data is to be provided synchronously to an application.

The synchronization point is defined as the data exchange event of the slave with the lowest address in the network. This definition relies on the cyclical slave polling with increasing slave addresses per cycle, which is one of the basic communication principles of AS-i. The SAP5 always monitors the data communication and detects the change from a higher to a lower slave address. If such a change has been recognized, the SAP5 assumes that the slave with the lower address has the lowest address in the network.

There are some special procedures that become active during the start of synchronous I/O mode operation and if more than three consecutive telegrams have been sent to the same slave address. This is described in more detail in section 5.8.3.

3.2.8. 4 Input / 4 Output Processing in Extended Address Mode

A new feature of *AS-Interface Complete Specification V3.0* is additional support of 4-bit wide output data in Extended Address Mode. Until *AS-Interface Complete Specification V2.11,* it was only possible to send three data output bits from the master to the slave in Extended Address Mode because telegram bit I3 was used to select between the A or B slave type for extended slave addressing (up to 62 slaves per network). In normal address mode, bit I3 carries output data for pin D3.

The new definition introduces a multiplexed data transfer so that all 4-bits of the data output port can be used again. A first AS-i cycle transfers the data for a 2-bit output nibble only, and then the second AS-i cycle transfers the data for the complementary 2-bit nibble. Nibble selection is done by the remaining third bit. To ensure continuous alternation of information bit I2 and thus continued data transfer of both nibbles, a special watchdog has been implemented that observes the state of the I2 bit. The watchdog can be activated or deactivated by EEPROM setting. It provides a watchdog filter time of about 327ms.

The multiplexed transfer increases the refresh time per output by a factor of two; however, some applications can tolerate this increase and gain the advantage of less external circuitry and better slave address efficiency. The sampling cycle of the data inputs remains unchanged since the meaning of bit I3 has not been changed in the slave response with the definition of the Extended Address Mode.

More detailed information is given in section 5.8.4.

3.2.9. AS-i Safety Mode

Using the SAP5 Safety Mode makes it easy to implement a safety-related AS-i slave according to the AS-i Safety at Work concept. Slaves complying with the control category 4 according to EN 954 –1 can be implemented even with a minimum of external circuitry.

In Safety Mode, the response of the SAP5 on a *Data_Exchange* master call (*DEXG*) is different. Instead of responding with the regular input data provided at the data ports, a 4-bit data word from a specific 8∗4 bit code table is transmitted to the master. Cycling the code table is used to transmit another data word with each *DEXG* master call. The data transmission is supervised by a safety monitor.

In Safety Mode, the use of the enhanced data input features described in sections 3.2.5 to 3.2.8 are disabled. In this case, the Safety Mode related inputs act as 3-level inputs. See section 5.18 for further details.

3.2.10. Enhanced LED Status Indication

The SAP5 supports status indication by two LED outputs. More detailed information on the signaling scheme can be found in section 5.11.

3.2.11. Communication Monitor/Watchdog

Data and parameter communication is continuously observed by a communication monitor. If neither *Data_Exchange* nor *Write_Parameter* calls have been addressed to and received by the SAP5 within a time frame of approximately 41ms, the No Data/Parameter Exchange status is detected and signaled at LED1.

If the respective flags are set in the EEPROM, the communication monitor can also act as a communication watchdog that initiates a complete SAP5 reset after the expiration of the watchdog timer. The watchdog mode can also be activated and deactivated by a signal at parameter port pin P0. For additional detailed information, see section 5.17.

3.2.12. Write Protection of ID_Code_Extension_1

As defined in *AS-Interface Complete Specification V3.0* the SAP5 also supports write protection for *ID_Code_Extension_1*. The feature allows the activation of new manufacturer-protected slave profiles and is enabled by EEPROM setting. It is described in more detail in section 5.20.

3.2.13. Summary of Master Calls

Table 3.2 and Table 3.3 on the following pages show the complete set of master calls that are decoded by the SAP5 in Slave Mode. The master calls in Table 3.3 are intended for programming the SAP5 by the slave manufacturer only. They become deactivated as soon as the *Lock_EE_PRG* and *Safety_Program_Mode_Disable* flags are set in the Firmware Area of the EEPROM.

The following abbreviations are used in Table 3.2 and Table 3.3 column headings:

- ST: Start bit
- CB: Control bit
- PB: Parity Bit
- EB: End Bit

Important note regarding full compliance with the *AS-Interface Complete Specification*: In order to achieve full compliance with the *AS-Interface Complete Specification*, the *Lock_EE_PRG* flag must be set by the manufacturer of AS-i slave modules during the final manufacturing and configuration process and before an AS-i slave device is delivered to field application users.

Table 3.2 SAP5 Master Calls and Related Slave Responses

Note: In Extended Address Mode, the "Select Bit" defines whether the A-Slave or B-Slave is being addressed. Depending on the type of master call, the I3 bit carries the select bit information (Sel) or the inverted select bit information ($\overline{Sel}$) in Extended Address Mode. The Extended Address Mode cannot be activated if the EEPROM flag *Lock_EE_PRG* is at the logic LOW level. Refer to section 4.3 for programming the *Lock_EE_PRG* flag.

		Master Request														Slave Response						
Instruction	**Name**	**ST**	**CB**	**A4**	**A3**	**A2**	**A1**	**A0**	**I4**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**	**SB**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**
Data_Exchange	**DEXG**	0	0	A4	A3	A2	A1	A0	0	D3 $\overline{Sel}$	D2	D1	D0	PB	1	0	D3	D2	D1	D0	PB	1
Write_Parameter	**WPAR**	0	0	A4	A3	A2	A1	A0	1	P3 $\overline{Sel}$	P2	P1	P0	PB	1	0	P3	P2	P1	P0	PB	1
Address_Assignment	**ADRA**	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	PB	1	0	0	1	1	0	0	1
Write_Extended_ID-Code_1	**WID1**	0	1	0	0	0	0	0	0	ID3	ID2	ID1	ID0	PB	1	0	0	0	0	0	0	1
Delete_Address	**DELA**	0	1	A4	A3	A2	A1	A0	0	0 Sel	0	0	0	PB	1	0	0	0	0	0	0	1
Reset_Slave	**RES**	0	1	A4	A3	A2	A1	A0	1	1 $\overline{Sel}$	1	0	0	PB	1	0	0	1	1	0	0	1
Read_I/O-Configuration	**RDIO**	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	0	PB	1	0	IO3	IO2	IO1	IO0	PB	1
Read_ID-Code	**RDID**	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read_Extended_ID-Code_1	**RID1**	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	0	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read_Extended_ID-Code_2	**RID2**	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read_Status	**RDST**	0	1	A4	A3	A2	A1	A0	1	1 $\overline{Sel}$	1	1	0	PB	1	0	S3	S2	S1	S0	PB	1
Broadcast (Reset)	**BR01**	0	1	1	1	1	1	1	1	0	1	0	1	1	1	— no slave response —						

Table 3.3 SAP5 Additional Master Calls for Slave Configuration

		Master Request													Slave Response						
Instruction	**Name**	**ST**	**CB**	**A4**	**A3**	**A2**	**A1**	**A0**	**I4**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**	**SB**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**
Set_ID-Code	**(RDIO)**	0	1	A4	A3	A2	A1	A0	1	1	0	0	0	PB	1	0	0	1	1	0	0	1
Set_IO_Config	**(RDID)**	0	1	A4	A3	A2	A1	A0	1	1	0	0	1	PB	1	0	0	1	1	0	0	1
Set_Extended_ID-Code_2	**(RID1)**	0	1	A4	A3	A2	A1	A0	1	1	0	1	0	PB	1	0	0	1	1	0	0	1
Set_Control_Code	**(RID2)**	0	1	A4	A3	A2	A1	A0	1	1	0	1	1	PB	1	0	0	1	1	0	0	1
Set_Control_Code_2	**(RES)**	0	1	A4	A3	A2	A1	A0	1	0	1	0	0	PB	1	0	0	1	1	0	0	1
Enter_Safety_Program_ Mode	**PRGM**	0	1	0	0	0	0	0	1	1	1	0	1	1	1	— no slave response —						

4 EEPROM

4.1. Overview

The SAP5 features an on-chip EEPROM with typical write and read times according to Table 4.1.

Table 4.1 EEPROM Read and Write Times

Parameter	Symbol	Min	Max	Unit
Initialization read out time [1)]	t_{read_init}		50.0	µs
Write time after *ADRA* master request [2)]	t_{wrt_adra1}		38.0	ms
Write time after *ADRA* master request [3)]	t_{wrt_adra2}		12.5	ms
Write time after *WID1* master request (user access) [2)]	t_{wrt_wid1u}		38.0	ms
Write time after *WID1* master request (manufacturer access) [3)]	t_{wrt_wid1m}		25.0	ms
Single cell write time [4)]	t_{wrt_prgm}		12.5	ms

1) Time includes read out of the configuration block. If running in Safety Mode, the User/Firmware Area and the Safety Area will be read out in parallel.
2) The *Lock_EE_PRG* flag is set.
3) The *Lock_EE_PRG* flag is not yet set.
4) Applies to the programming of data in both Firmware Area and Safety Area.

For security reasons, the memory area is structured in three independent data blocks and a single configuration block containing the *Security_Flag*. The data blocks are named User Area, Firmware Area, and Safety Area, which are defined in Table 4.2 and Table 4.4.

The Firmware Area contains all manufacturing-related configuration data; e.g., selection of optional features, ID codes, etc. It can be protected against undesired data modification by setting the *Lock_EE_PRG* flag to ‘1’.

The User Area contains only such data that is relevant for changes at the final application (i.e., field installation of slave module). Because the environment where modifications of the user data might become necessary can sometimes be harsh and unpredictable, additional security has been added to the programming of the User Area, ensuring a write access cannot result in an undetected corruption of EEPROM data.

The Safety Area contains the cryptographic code table for the Safety Mode.

The EEPROM cells in the User Area, Firmware Area, and Safety Area have a word width of 6 bits. The sixth bit is not shown in Table 4.2 and Table 4.4. The sixth bit of each cell represents the odd parity of the respective data word, providing an additional data security mechanism. The programming of the parity bit is performed automatically during the EEPROM write process and cannot be influenced by the user. Each EEPROM read process – particularly during initialization of the SAP5 – involves an evaluation of the parity bits. If an incorrect parity bit is found in the User Area, the entire User Area data is treated as corrupted. The SAP5 returns to Slave Address “0” and the *ID_Code* as well as the *IO_Code* are set to F_{HEX}. If a false parity bit has been found in one or more cells of the Firmware Area or the Safety Area, the status register bit S1 will be set (= ‘1’), signaling the same state as if the input PFAULT had been set (see section 5.16).

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4.2. User Area Programming

User Area data can be written by an *ADRA* or *WID1* master request (see Table 3.2). Any such write access is accompanied by two write steps to the *Security_Flag*, one before and one after the actual modification of user data.

1. The following procedure is executed when writing to the User Area of the EEPROM:
2. The *Security_Flag* is programmed to '1'.
3. The content of the *Security_Flag* is read back, verifying it was programmed to '1'.
4. The user data is modified.
5. A read back of the written data is performed.
6. If the read back has proven the successful programming of the user data, the *Security_Flag* is programmed back to '0'.
7. The content of the *Security_Flag* is read back, verifying it was programmed to '0'.

Successful execution of the EEPROM write procedure can be observed in the status register contents (refer to Table 5.21). If bit S0 is set (logic HIGH), the write process is not finished yet and the programming data is still volatile. If bit S3 (which is the *Security_Flag*) is set, the write procedure did not successfully complete either because the write cycle was interrupted or due to an internal error. In order to program the data correctly, the write request should be repeated. The status register can be read using the AS-i master call *Read_Status* (*RDST*).

In addition to a read out of the data areas, the *Security_Flag* of the EEPROM is also read and evaluated during SAP5 initialization. If the value of the *Security_Flag* equals '1' (e.g., due to an undesired interruption of a User Area write access), the entire User Area data is treated as corrupted (see section 5.16). The SAP5 returns to Slave Address "0" and the *ID_Code* as well as the *IO_Code* are set to F_{HEX}. As a result, the programming of the User Area data can be repeated.

Table 4.2 SAP5 EEPROM – User and Firmware Area Content

Internal EEPROM Address	Bit Position	EEPROM Cell Contents	Description
User Area			
0	4 to 0	*A [4:0]*	Slave address
1	2 to 0	*ID1_Bit [2:0]*	*ID_Code_Extension_1* (user-configurable)
	3	*ID1_Bit3*	*ID_Code_Extension_1*, A/B slave selection in Extended Address Mode
	4		Not implemented
2	3 to 0	*ID1_Bit [3:0]*	*ID_Code_Extension_1* (manufacturer-configurable)
	4		Not implemented
3	4 to 0		Not implemented

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Internal EEPROM Address	Bit Position	EEPROM Cell Contents	Description
Firmware Area			
4	4	*Synchronous_Data_IO*	Synchronized Data I/O Mode
	3 to 0	*ID_Bit [3:0]*	*ID_Code*
5	4	*Inhibit_Write_ID1*	*ID_Code_Extension_1* is manufacturer configurable; refer to section 5.20
	3 to 0	*ID2_Bit [3:0]*	*ID_Code_Extension_2*
6	4	*P1_Delay_Activation*	If flag is set, the logic value at the parameter pin P1 determines whether the *Delay_Mode* function is active or inactive; refer to Table 5.11
	3 to 0	*IO_Bit [3:0]*	*IO_Code*
7	4	*Lock_EE_PRG*	Programming of the EEPROM Firmware region is possible as long as this flag is **not** set (logic LOW).
	3	*Delay_Mode*	Activates the *Delay_Mode* function, refer to Table 5.11
	2	*Invert_Data_In*	All Data Port inputs are inverted.
	1	*Inhibit_BR01*	If flag is set, the master call *BR01* is not executed.
	0	*Inhibit_Watchdog*	If flag is set, the watchdog is **not** activated.
8	4	*P2_Sync_Activation*	The Synchronized Data I/O Mode can be activated by parameter bit P2 as described in Table 5.12.
	3	*Ext_Addr_4I/4O_Mode*	4 Input/ 4 Output Mode in Extended Address Mode
	2	*Parallel_Out_4I/4O*	Enables the parallel data output option in Extended Address 4I/4O Mode
	1	*Master_Mode*	*Master / Repeater Mode Flag*
	0	*P0_Watchdog_Activation*	The watchdog can be enabled / disabled by the logic value at the parameter pin P0
9	4 to 0	Analog circuitry trim information	
10			
11			

4.3. Firmware Area Programming

In order to program one of the 5-bit cells in addresses 4 to 8 in the Firmware Area, a special master call according to Table 4.3 must be applied, followed immediately by a *DEXG* or *WPAR* call. Write access to the Firmware Area is possible as long as the *Lock_EE_PRG* flag is not set. The write procedure is started after receipt of the *DEXG*/*WPAR* call. Completion of the write procedure can be observed at the status register S0 as described in section 4.2.

The analog circuitry trim information (address 9 to 11) can be written by special test mode operation only.

It is not possible to read out the EEPROM data directly. However, AS-i-related configuration data such as *ID_Code* can be read by the respective *Read_ID_Code* (*RDID*) master request.

Table 4.3 SAP5 EEPROM – User and Firmware Area Programming

Note: See table notes at the end of the table.

Internal EEPROM Address	EEPROM Cell Content		Programming Master Calls
User Area			
0	*A[4:0]*		*ADRA* master call
1	*ID1_Bit [3:0]*		*WID1* master call
2	*ID1_Bit [3:0]*		
3	Not implemented		
Firmware Area			
4	*Synchronous_Data_IO*	I4	Set ID Code (*RDIO*) master call [1)] + *DEXG/WPAR* master call [2)]
	ID_Bit [3:0]	I3 to I0	
5	*Inhibit_Write_ID1*	I4	Set ID Code 2 *(RID1)* master call [1)] + *DEXG/WPAR* master call [2)]
	ID2_Bit [3:0]	I3 to I0	
6	*P1_Delay_Activation*	I4	Set IO Config *(RDID)* master call [1)] + *DEXG/WPAR* master call [2)]
	IO_Bit [3:0]	I3 to I0	
7	*Lock_EE_PRG*	I4	Set Control Code *(RID2)* master call [1)] + *DEXG/WPAR* master call [2)]
	Delay_Mode	I3	
	Invert_Data_In	I2	
	Inhibit_BR01	I1	
	Inhibit_Watchdog	I0	

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Internal EEPROM Address	EEPROM Cell Content	Programming Master Calls	
8	*P2_Sync_Activation*	I4	Set Control Code 2 *(RES)* master call [1] + *DEXG/WPAR* master call [2]
	Ext_Addr_4I/4O_Mode	I3	
	Parallel_Out_4I/4O	I2	
	Master_Mode	I1	
	P0_Watchdog_Activation	I0	
9	Analog circuitry trim information	Accessible by IDT only	
10			
11			

1) According to Table 3.3.

2) According to Table 3.2 with information bits corresponding to the left column; *DEXG* if I4 = '0', *WPAR* if I4 = '1'. Note: In contrast to regular *WPAR*/*DEXG* calls, the slave always returns the received data bits I3 to I0 for these master calls.

4.4. Safety Area Programming (SAP5S only)

The *Safety Area* contains the cryptographic code table, which consists of 8 data words and one swap-flag each (refer to section 5.18 for an explanation of the SAP5 Safety Mode). Similar to the Firmware Area, it can be protected against undesired data modification by setting the *Safety_Program_Mode_Disable* flag; see address 31 in Table 4.4.

NOTE: Once the *Safety_Program_Mode_Disable* flag is set, the Safety Area of the EEPROM is *permanently* locked; i.e., write access to the Safety Area as described in Table 4.4 is possible only as long as the *Safety_Program_Mode_Disable* flag is not set.

Table 4.4 SAP5 EEPROM – Safety Area Content

Logical EEPROM Address	Bit Position	EEPROM Cell Content	Description
1	4	*S_flag_0*	Swap-flag 0
	3 to 0	*DI_S0 [3:0]*	Data Input word 0 from Safety Code Table
2	4	*S_flag_1*	Swap-flag 1
	3 to 0	*DI_S1 [3:0]*	Data Input word 1 from Safety Code Table
3	4	*S_flag_2*	Swap-flag 2
	3 to 0	*DI_S2 [3:0]*	Data Input word 2 from Safety Code Table
4	4	*S_flag_3*	Swap-flag 3
	3 to 0	*DI_S3 [3:0]*	Data Input word 3 from Safety Code Table
5	4	*S_flag_4*	Swap-flag 4
	3 to 0	*DI_S4 [3:0]*	Data Input word 4 from Safety Code Table

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Logical EEPROM Address	Bit Position	EEPROM Cell Content	Description
6	4	*S_flag_5*	Swap-flag 5
	3 to 0	*DI_S5 [3:0]*	Data Input word 5 from Safety Code Table
7	4	*S_flag_6*	Swap-flag 6
	3 to 0	*DI_S6 [3:0]*	Data Input word 6 from Safety Code Table
8	4	*S_flag_7*	Swap-flag 7
	3 to 0	*DI_S7 [3:0]*	Data Input word 7 from Safety Code Table
31	1	*Safety_Mode_Enable*	If set, Safety Mode is enabled
	0	*Safety_Program_Mode_Disable*	If set, Safety Area is protected against overwriting

Similar to the Firmware Area programming, Safety Area programming is intended to be used only during production set-up of a slave component at the manufacturer's site. Write access to the Safety Area of the EEPROM is possible in the Safety Program Mode. It can be entered only if the *Safety_Program_Mode_Disable* flag is not yet set to '1' and if the slave address has been set to 0_{HEX}. If the slave address equals 0_{HEX}, the reception of the *Enter_Program_Mode_Safety* (*PRGM*) call sets the SAP5 device into the Safety Program Mode. It should be noted that no response is generated to the *Enter_Program_Mode_Safety* call (refer to the *AS-Interface Complete Specification*).

In the Safety Program Mode, the *Write_Parameter* (*WPAR*) and *Data_Exchange* (*DEXG*) calls are used to transfer data words to the EEPROM similar to the Firmware Area write procedure described in section 4.3. However, the address bits A[4:0] of the master telegrams are used to address one of the memory locations of the EEPROM (refer to Table 4.4). The information bits I[4:0] (normally used for output data) carry the data to be stored.

Any *WPAR* or *DEXG* call initializes an autonomous write process within the SAP5. The status of the write process can be monitored by evaluating the status register of the SAP5 as described in section 4.1. Since the SAP5 is still in Safety Program Mode, the address within the *Read_Status* master call has the "don't care" status. In order to execute as many write procedures as desired, do not leave the Safety Program Mode until finished.

Note: The SAP5 will leave the Safety Program Mode and start its initialization procedure if it receives a *Reset_Slave* (*RES*) master call to any desired slave address.

Any attempt to access one of the unavailable EEPROM address locations (0, 9 to 30) of the Safety Area via a *Write_Parameter* (*WPAR*) or *Data_Exchange* (*DEXG*) command will be ignored.

There is no direct read access to the Safety Area data in Safety Program Mode.

After programming the Safety Area, an EEPROM verification procedure should be performed; i.e., by performing one complete AS-i safety cycle (8 *DEXG* calls at intervals of at least 250µs) in Safety Mode operation.

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5 Detailed Functional Description

5.1. Power Supply

The power supply block provides a sensor supply, which is inductively decoupled from the AS-i bus voltage, at the UOUT pin. The decoupling is realized by an electronic inductor circuit, which basically consists of a current source and a controlling low pass filter. The time constant of the low pass, which affects the resulting input impedance at the LTGP pin, can be adjusted by an external capacitor at the CDC pin.

A second function of the power supply block is to generate a regulated 5V supply for operation of the internal logic and some of the analog circuitry. The voltage is provided at the U5R pin and can be used to supply external circuitry as well if the current requirements stay within in the specified limits (see Table 2.2). Because the 5V supply is generated from the decoupled sensor supply at UOUT, the current drawn at U5R must be subtracted from the total available load current at UOUT.

The power supply dissipates most of the power (see Table 5.1):

$P_{tot} = V_{DROP} * (I_{UOUT} + I_{5V}) + (V_{UOUT}\text{-}5V) * I_{5V}$

In total, the power dissipation must not exceed the specified values in section 2.1.

To cope with fast internal and external load changes (spikes), external capacitors at UOUT and U5R are required. The LTGN pin defines the ground reference voltage for both UOUT and U5R.

5.1.1. Voltage Output Pins UOUT and U5R

Table 5.1 Properties of Voltage Output Pins UOUT and U5R

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Positive supply voltage for SAP5 operation [1)]	V_{LTGP}		16	34	V
Voltage drop from LTGP pin to UOUT pin	V_{DROP}	V_{LTGP} > 22V	5.2	7.8	V
UOUT output supply voltage	V_{UOUT}	$I_{UOUT} = I_{UOUTmax}$	V_{LTGP} - $V_{DROPmax}$	V_{LTGP} - $V_{DROPmin}$	V
UOUT output voltage pulse deviation [2)]	V_{UOUTp}	C_{UOUT} = 10µF		1.5	V
UOUT output voltage pulse deviation width [2)]	t_{UOUTp}	C_{UOUT} = 10µF		2	ms
5V supply voltage	V_{U5R}		4.75	5.25	V
UOUT output supply current	I_{UOUT}	I_{U5R} = 0 V_{LTGP} >24V	0	55	mA
U5R output supply current	I_{U5R}		0	4	mA
Total output current I_{UOUT} + I_{5V}	I_O			60	mA
Blocking capacitance at UOUT	C_{UOUT}		10	470	µF
Blocking capacitance at U5R	C_{U5R}		100		nF

1) Parameter is also given in Table 2.2.

2) C_{UOUT} = 10µF; output current switches from 0 to $I_{UOUTmax}$ and vice versa.

5.1.2. Input Impedance (AS-Interface Bus Load)

Table 5.2 AS-Interface Bus Load Properties

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Equivalent resistor of the SAP5 [1), 2)]	R_{IN1}		13.5		kΩ
Equivalent inductor of the SAP5 [1), 2)]	L_{IN1}		13.5		mH
Equivalent capacitor of the SAP5 [1), 2)]	C_{IN1}			30	pF
Equivalent resistor of the SAP5 [1), 2)]	R_{IN2}		13.5		kΩ
Equivalent inductor of the SAP5 [1), 2)]	L_{IN2}		12	13.5	mH
Equivalent capacitor of the SAP5 [1), 2)]	C_{IN2}			15 + (L-12mH)∗10pF/mH	pF
Parasitic capacitance of the external over-voltage protection diode (Zener diode) [1)]	C_{Zener}			20	pF

1) The equivalent circuit of a slave, which is calculated from the impedance of the SAP5 and the parallel external over-voltage protection diode (Zener diode), must satisfy the requirements of the *AS-Interface Complete Specification* for Extended Address Mode slaves.

2) After the maximum parasitic capacitance of the external over-voltage protection diode (20pF) has been subtracted, the specifications group including R_{IN1}, L_{IN1} and C_{IN1} or the specifications group including R_{IN2}, L_{IN2} and C_{IN2} must be met for compliance with the *AS-Interface Complete Specification V3.0*.

Table 5.3 CDC Pin Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	Typical	MAX	UNIT
Input voltage range	V_{CDC_IN}		-0.3		V_{U5R}	V
External decoupling capacitor	C_{CDC}			100		nF

Note: A decoupling capacitor defines the internal low-pass filter time constant; lower values decrease the impedance but improve the turn-on time. Higher values do not improve the impedance but do increase the turn-on time. The turn-on time also depends on the load capacitor at UOUT. After connecting the slave to the power, the capacitor is charged with the maximum current I_{UOUT}. The impedance will increase when the voltage allows the analog circuitry to fully operate.

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5.2. Thermal Protection

The SAP5 continuously monitors its silicon die temperature. If the temperature rises above approximately 140°C for more than 2 seconds, the SAP5 will cut off the UOUT output from the internal voltage reference. Thus the current consumption of the SAP5 will drop down to its operating current (refer to Table 2.2). In order to prevent an undesired drawing of transmitter current, the transmitter is also disabled if the over-temperature cut off condition occurs.

After an over-temperature cut-off, if the die temperature has cooled down by 10 to 20°C, the output voltage at UOUT will be restored and the SAP5 performs an initialization with an additional time delay of 1s.

Table 5.4 Cut-Off Temperature

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Chip temperature for over-temperature shut down	T_{CutOff}		125	160	°C

5.3. DC Characteristics – Digital Inputs

The following pins contain digital high-voltage input stages:

Input-only pin: **PFAULT**
I/O pins: **P1, P3, D1, D3, DSTBn, PSTBn, LED1** (PSTBn and LED1 are inputs for test purposes only)
3-level I/O pins: **P0, P2, D0, D2** (see table notes 1) and 2) in Table 5.5)

Table 5.5 DC Characteristics of Digital High Voltage Input Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Voltage range for input “offset_low” level 1), 2)	V_{OFL}		0	1.0	V
Voltage range for input “offset_high” level 1), 2)	V_{OFH}		1.6	V_{UOUT}	V
Voltage range for input “low” level 2)	V_{IL2}		0	2.5	V
Voltage range for input “high” level	V_{IH}		3.5	V_{UOUT}	V
Current range for input “low” level 3)	I_{IL}	V_{IN} = 1V	-12	-3	µA
Current range for input “high” level	I_{IH}	$V_0 \geq V_{U5R}$	-10	10	µA
Capacitance at pin DSTBn 4)	C_{DL}			10	pF

1) The P0, P2, D0, D2 pins are used as 3-level inputs, i.e. inputs with offset detection, in Safety Mode only; otherwise configuration depends on the slave profile. Refer to Table 5.15.

2) The 3-level input pads contain independent comparators for the detection of regular input data level and offset. Refer to Figure 5.8 for constraints to the externally applied voltages in Safety Mode.

3) The pull-up current is driven by a current source connected to U5R. It stays almost constant for input voltages ranging from 0 to 3.8V.

4) The internal pull-up current is sufficient to avoid accidental triggering of an SAP5 reset if the DSTBn pin remains unconnected. For external loads at DSTBn, a sufficient pull-up resistor is required to ensure $V_{IH} \geq 3.5V$ in less than 90ms after the beginning of a DSTBn = low pulse.

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5.4. DC Characteristics – Digital Outputs

The following pins contain digital high-voltage, open-drain output stages:

Output-only pin: **LED2**

I/O pins: **D[3:0], P[3:0], DSTBn, PSTBn, LED1** (PSTBn and LED1 are inputs for test purposes only)

Table 5.6 DC Characteristics of Digital High Voltage Output Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX.	UNIT
Voltage range for output “low” level	V_{OL1}	I_{OL1} = 10mA	0	1	V
Voltage range for output “low” level	V_{OL2}	I_{OL2} = 2mA	0	0.4	V
Output leakage current	I_{OH}	$V_{0H} \geq V_{U5R}$	-10	10	µA

A slew rate limitation is applied to each digital high voltage output driver that limits the rise and fall times for both high/low and low/high transitions to 40 to 50 ns.

NOTE: The rise time for a low/high transition is primarily influenced by the external pull-up resistor.

5.5. AS-i Receiver

The receiver detects (telegram) signals at the AS-i line, converts them to digital pulses, and forwards them to the UART for further processing. The receiver is internally connected between the LTGP and LTGN pins.

Functional, the receiver removes the DC value of the input signal, band-pass filters the AC signal, and extracts the digital output signals from the $\sin^2$-shaped input pulses via a set of comparators. The amplitude of the first pulse determines the threshold level for all following pulses. This amplitude is digitally filtered to guarantee stable conditions and to suppress burst spikes. This approach combines a fast adaptation to changing signal amplitudes with a high detection safety. The comparators are reset after every detection of a telegram pause at the AS-i line.

When the receiver is turned on, the transmitter is turned off to reduce the power consumption.

Table 5.7 Receiver Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
AC signal peak-peak amplitude (between LTGP and LTGN)	V_{SIG}		3	8	V_{PP}
Receiver comparator threshold level (refer to Figure 5.1)	V_{LSIGon}	Relative to first pulse amplitude	45	55	%

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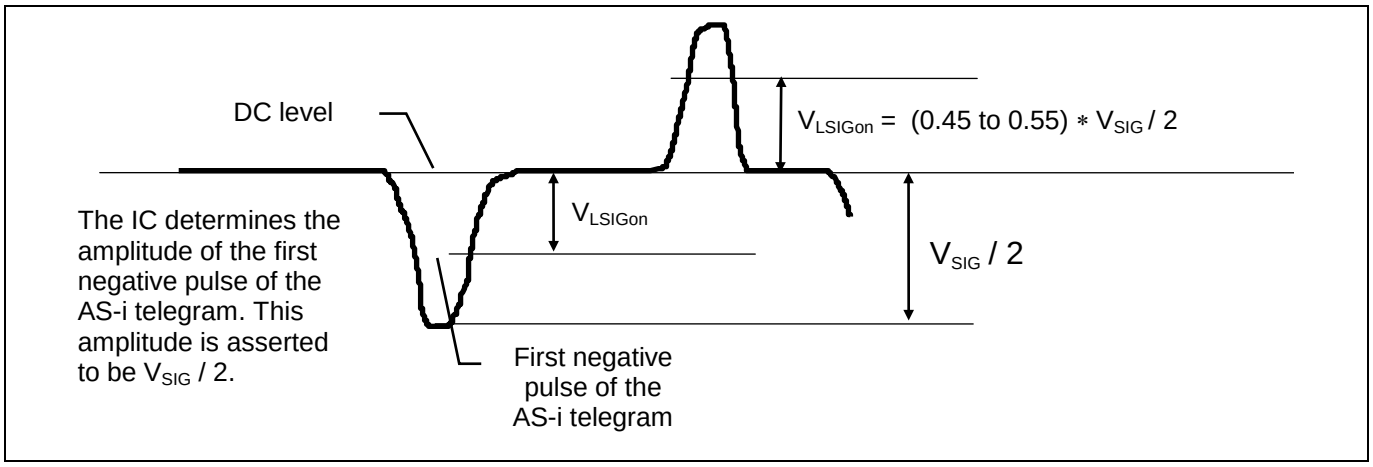
5.6. AS-i Transmitter

Figure 5.1 Basic Receiver Comparator Threshold Set-up Principles



The transmitter draws a modulated current between LTGP and LTGN to generate the communication signals. The shape of the current corresponds to the integral of a $\sin^2$-function. The transmitter comprises a current DAC and a high-current driver. The driver requires a small bias current to flow. The bias current is ramped up slowly for a specific time before the transmission starts so that any false voltage pulses on the AS-i line are avoided.

When the transmitter is turned on, the receiver is turned off to reduce the power consumption. The SAP5 includes a Clock Watchdog that becomes activated once the clock signal is stopped for approximately 100µs to 150µs so that the transmitter is prevented from being permanently switched on in case the clock signal is missing.

Table 5.8 Transmitter Current Amplitude

PARAMETER	SYMBOL	MIN	MAX	UNIT
Modulated transmitter peak current swing (between LTGP and LTGN)	I_{SIG}	55	68	mA_P

5.7. Parameter Port and PSTBn

The parameter port is always configured for continuous bi-directional operation. However, if *IO_Code*=7_{HEX} (see Table 5.14), the parameter ports will return to high impedance state immediately after a *WPAR* request because they act as data input ports or safety data ports for a subsequent *DEXG* master call.

Every pin contains an NMOS open-drain output driver plus a high-voltage, high-impedance digital input stage. Received parameter output data is stored in the Parameter Output Register and subsequently forwarded to the open-drain output drivers. A specific time ($t_{PI\text{-}latch}$) after new output data has arrived at the port, the corresponding inputs are sampled. Due to the open-drain of the output driver, the input value results from a wired AND combination of the parameter output value and such signals driven to the port by external sources.

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The availability of new parameter output data is signaled by the Parameter Strobe (PSTBn) signal as shown in Figure 5.2.

In addition to the basic I/O function, the first parameter output event after an SAP5 reset has an additional effect. It enables the data exchange functionality.

Any SAP5 reset sets the Parameter Output Register to F_{HEX} and forces the parameter output drivers to the high impedance state. Simultaneously, a Parameter Strobe is generated with the same t_{setup} timing and t_{PSTBn} pulse width as would be used to drive new output data.

Table 5.9 Timing for Parameter Ports

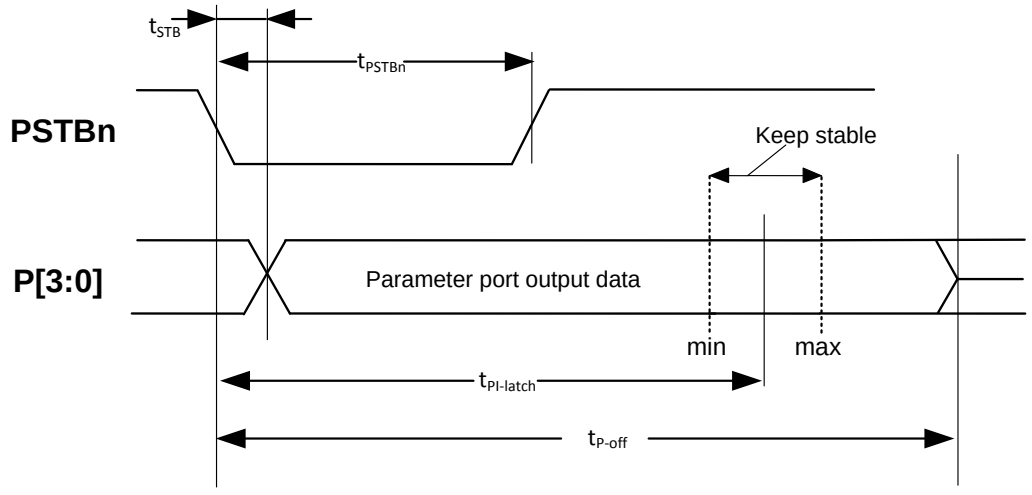
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Output data is valid after PSTBn high-low edge	t_{STB}		0.0	1.5	µs
Pulse width of Parameter Strobe (PSTBn) [1)]	t_{PSTBn}		6.0	6.8	µs
Acceptance of input data [2)]	$t_{PI\text{-}latch}$		10.5	12.5	µs
Parameter Port is at high impedance state after PSTBn high-low edge [3)]	$t_{P\text{-}off}$		56.0	64.5	µs

1) The timing of the resulting voltage signal also depends on the external pull up resistor.

2) The parameter input data must be stable within the period defined by min. and max. values of $t_{PI\text{-}latch}$.

3) Concerns the IO configuration “7” only (see Table 5.14).

Figure 5.2 Timing Diagram for Parameter Port P[3:0], PSTBn



Parameter input value (PIx) = Parameter output value (POx) (wired AND with external signal source value)

5.8. Data Port and DSTBn

5.8.1. Timing of Data I/O and DSTBn

Every data pin (D0 to D3) contains an NMOS open-drain output driver as well as a high-voltage, high-impedance input stage. Received output data is stored in the Data Output Register and subsequently forwarded to the data pins. A specific time ($t_{DI\text{-}latch}$) after new output data has been written to the port the input data is sampled.

The availability of new output data is signaled by the Data Strobe (DSTBn) signal as shown in Figure 5.3. The DSTBn pin has an additional reset input function, which is described further in section 5.13.

Any SAP5 reset sets the Data Output Register to F_{HEX} and forces the data output drivers to the high-impedance state. Simultaneously, a Data Strobe is generated with the same t_{setup} timing and t_{DSTBn} pulse width as would be used to drive new output data.

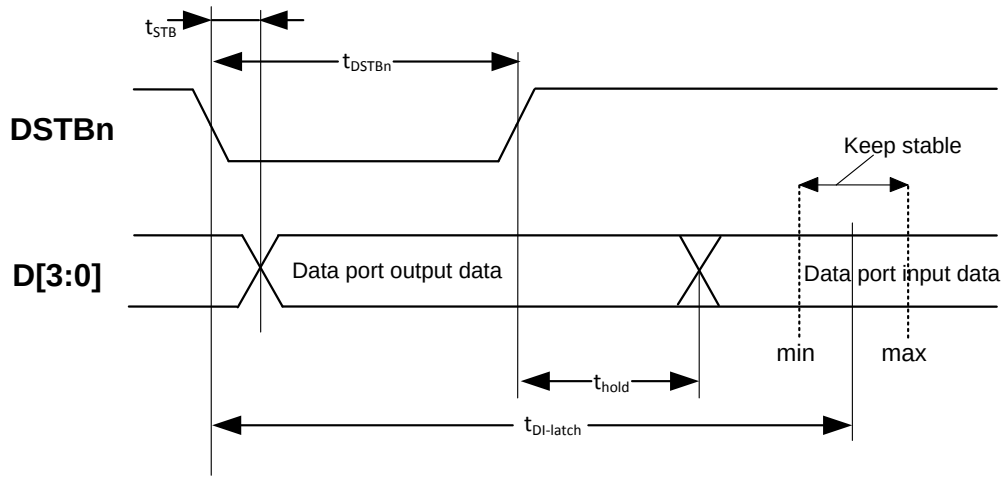
Table 5.10 Timing for Data Port Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Output data is valid after DSTBn high/low edge	t_{STB}		0.0	1.5	µs
Output driver is at high impedance state after DSTBn low/high [1)]	t_{hold}		0.2	1.0	µs
Pulse width of Data Strobe (DSTBn) [2)]	t_{DSTBn}		6.0	6.8	µs
Acceptance of input data [3)]	$t_{DI\text{-}latch}$		10.5	12.5	µs

1) Parameter is only valid if the respective data port is configured as an I/O pin.
2) The timing of the resulting voltage signal also depends on the external pull-up resistor.
3) The input data must be stable within the period defined by minimum and maximum values of $t_{DI\text{-}latch}$.

5.8.2. Input Data Pre-Processing

Figure 5.3 Timing Diagram for Data Port D[3:0] and DSTBn

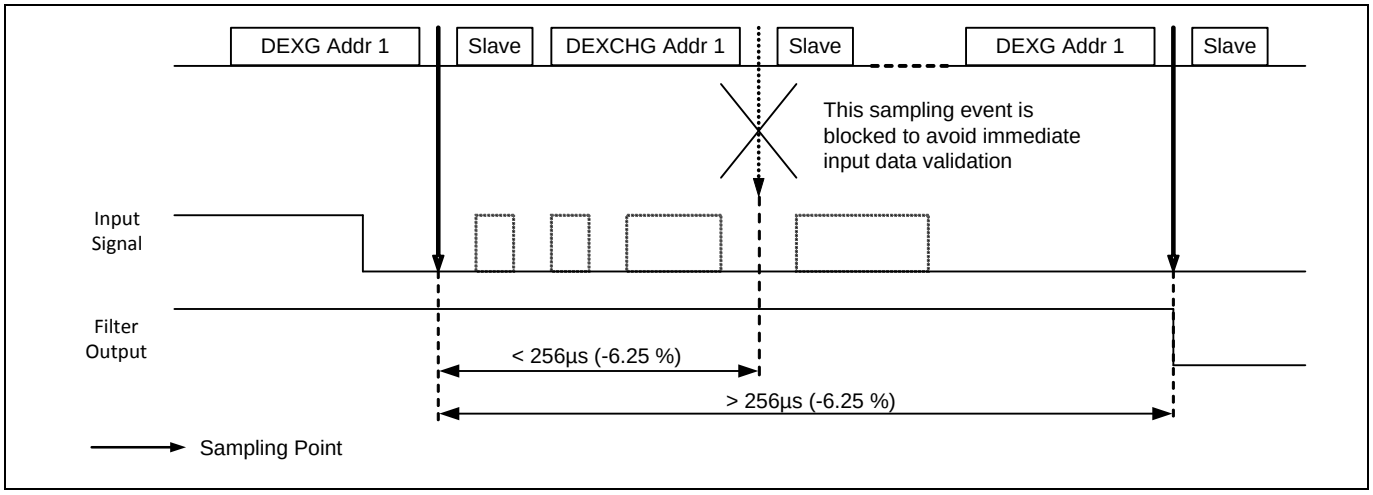


In addition to the standard input function, the Data Port has data pre-processing features that can be activated by setting corresponding flags in the Firmware Area of the EEPROM.

- **Input Inverting:** The input values of all four data input channels are inverted if the *Invert_Data_In* flag is '1'
- **Input Delay:** If the Delay Mode is activated, a new input value is returned to the master if equal input data was sampled for two consecutive *Data_Exchange* cycles. As long as the condition is not true, previous valid data is returned. To suppress undesired input data validation in the event of immediately repeated *Data_Exchange* calls (i.e., AS-i masters immediately repeat a *Data_Exchange* request if no valid slave response was received on the first request), input data sampling is blocked for 256µs (-6.25%) after every sampling event.

The filter output of each data port is preset to "0" after reset or as long as the *Data_Exchange_Disable* flag is set.

Figure 5.4 Principles of Delay Mode Input Filtering – Example for Slave with Address 1_{HEX}



Activation of Delay Mode depends on the EEPROM flags *Delay_Mode* and *P1_Delay_Activation* and the value of the Parameter Port P1 Output Register as shown in Table 5.11. Delay Mode cannot be activated when Safety Mode is enabled.

Note: The input signal at Parameter Port P1 does not affect activation of Input Delay Mode. Only the master can change the activation status by sending a corresponding *Write_Parameter* (*WPAR*) request.

***Table 5.11 Activation of* Delay Mode**

Delay_Mode	P1_Delay_Activation	Parameter P1 Output Register	Delay Mode
0	X	X	OFF
1	0	X	ON
1	1	1	OFF
1	1	0	ON

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5.8.3. Synchronous Data I/O Mode

Since the slaves in an AS-i network are called successively by the master, the data input and output operations of different slaves are not normally synchronized. If there is, however, an application that requires accurate synchronized data I/O timing, the respective slaves can be operated in the Synchronous Data I/O Mode. With respect to communication with the master, slaves running in the Synchronous Data I/O Mode behave like regular slaves. However, the input data sampling as well as the output data driving is determined by the polling cycle of the respective AS-i network as described below.

Activation of the SAP5 Synchronous Data I/O Mode is related to the EEPROM flags *Synchronous_Data_IO* and *P2_Sync_Activation* (refer to Table 4.2) and the value of the Parameter Port P2 Output Register as follows:

NOTE: The input signal at Parameter Port P2 does not affect activation of Synchronous Data I/O Mode. Only the master can change the activation status by sending a corresponding *Write_Parameter* (*WPAR*) request.

Table 5.12 Activation of the Synchronous Data I/O Mode

Synchronous_Data_IO	P2_Sync_Activation	Parameter P2 Output Register	Synchronous Data I/O Mode
0	X	X	OFF
1	0	X	ON
1	1	1	OFF
1	1	0	ON

NOTE: The Synchronous Data I/O Mode is not available if the Safety Mode is enabled.

If Synchronous Data I/O Mode is activated, input data sampling as well as the output data driving events are moved to different times *synchronized* to the polling cycle of the AS-i network. Nevertheless, the communication principles between master and slave remain unchanged compared to regular operation. The following rules apply:

- Data I/O is triggered by the *DEXG* call to the slave with the lowest slave address in the network. Based on the fact that a master is calling slaves successively with rising slave addresses, the SAP5 considers the trigger condition true if the slave address of a received *DEXG* call is less than the slave address of the previous correctly received *DEXG* call.
- Data I/O is only triggered if the slave has correctly received data during the last cycle. If the slave did not receive data (i.e., due to a communication error), the Data Outputs are not changed and no Data Strobe is generated (the “arm+fire” principle). The inputs however, are always sampled at the trigger event.
- *If the slave with the lowest address in the network* is operated in the Synchronous Data I/O Mode, it postpones the output event for the received data for a full AS-i cycle. This is to keep all output data of a particular cycle image together.

  Note: To make this feature useful, the master must generate a data output cycle image once before the start of every AS-i cycle. The image is derived from the input data of the previous cycle(s) and other control events. Once an AS-i cycle has started, the image must not change. If A and B slaves are installed in parallel at one address, the master must address all A-Slaves in one cycle and all B-Slaves in the other cycle.

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- The input data, sampled at the slave with the lowest slave address in the network, is sent back to the master without any delay. Thus, the input data cycle image is fully captured at the end of an AS-i cycle, just as in networks without any Synchronous Data I/O Mode slaves. In other words, the input data sampling point has simply moved to the beginning of the AS-i cycle for all Synchronous Data I/O Mode slaves.
- If the Synchronous Data IO Mode is enabled through EEPROM setting (*Synchronous_Data_IO* = '1', *P2_Sync_Activation* = '0'), the *first DEXG call* that is received by a particular slave after the activation of the Data Port (*Data_Exchange_Disable* flag was cleared by a *WPAR* call) is processed as in standard operation. This is to capture valid input data for the first slave response and to activate the outputs as quickly as possible.
- The Data I/O operation is repeated together with the I/O cycle of the other Synchronous Data I/O Mode slaves in the network at the common trigger event. As a result, the particular slave is now in the Synchronous Data I/O Mode.
- *If the P2_Sync_Activation flag is set to '1,'* the Synchronous Data IO Mode can be activated or deactivated during normal operation by sending *Write_Parameter* calls containing the appropriate value in P2 (see Table 5.12).
- If the P2 output register changes from '1' to '0,' the Synchronous Data IO Mode is immediately enabled. Actual synchronous data I/O operation is reached after reception of the next *DEXG* call addressing the slave and the occurrence of the common trigger event. As in standard operation (Synchronous Data IO Mode is activated by the EEPROM setting), the first *DEXG* call still processes a data IO operation immediately. This is to capture valid input data for the slave response and to activate the outputs as quickly as possible.
- The Data I/O operation is repeated together with the I/O cycle of the other Synchronous Data I/O Mode slaves in the network at the common trigger event. As a result, the particular slave is now in the Synchronous Data I/O Mode.
- If the P2 output register changes from '0' to '1,' the Synchronous Data IO Mode is deactivated and disabled immediately. If a synchronous data I/O event was already scheduled but not yet processed (armed but not fired) before the Synchronous Data I/O Mode has become deactivated, the associated data output value is lost.
- If P2 changes back to '0,' reactivation of the Synchronous Data I/O Mode occurs in same manner as described above.
- To avoid a general suppression of Data I/O in the special case that a slave in Synchronous Data I/O Mode receives *DEXG calls only to its own address* (i.e., employment of a handheld programming device), the Synchronous Data I/O Mode becomes deactivated if the SAP5 receives three consecutive *DEXG* calls to its own slave address. The SAP5 resumes to Synchronous Data I/O Mode operation after it has observed a *DEXG* call to a slave address that is different from its own. The reactivation of the Synchronous Data I/O Mode is handled in the same manner for the first *DEXG* call after activation of the Data Port or after activation of the Synchronous Data I/O Mode by P2 changing to '0' (see description above).

If any of the data ports D0 to D3 is configured as a pure output (designated as "OUT" in Table 5.14), the SAP5 returns the output data that was received from the master immediately in its slave response. Since there is no input function available at such ports, the return value is independent from a possible Synchronous Data I/O Mode operation.

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When running in Synchronous Data I/O Mode, the SAP5 also generates the Data Strobe (DSTBn) signal; whereas the timing of input sampling and output buffering corresponds exactly to the standard operation (refer to Figure 5.3 and Table 5.10).

5.8.4. Support of 4I/4O Signaling in Extended Address Mode

In Extended Address Mode, the information bit I3 of the AS-i master telegram is used to distinguish between A and B slaves that operate in parallel at the same AS-i slave address. For more detailed information, refer to the *AS-Interface Complete Specification V3.0*.

In addition to the benefit of an increased address range, the cycle time per slave is increased in Extended Address Mode from 5ms to 10ms and the useable output data is reduced from 4 to 3 bits. Because of the reduced data bits, Extended Address Mode slaves can usually control a maximum of only 3 data outputs. The input data transmission is not affected since the slave response still carries 4 data information bits in Extended Address Mode.

Additionally, the SAP5 supports applications that require 4-bit wide output data in Extended Address Mode if the application can tolerate further increased cycle times (e.g., push buttons and pilot lights). Such applications must be directly characterized by a new Slave Profile 7.A.x.7, which is defined in the *AS-Interface Complete Specification* (see section 9).

If the SAP5 is operated in Extended Address Mode and the *Ext_Addr_4I/4O_Mode* flag is set (= '1') in the EEPROM (refer to Table 4.2), it treats information bit I2 as the selector for two 2-bit wide data output banks:

- *Bank_1* = D0/D1
- *Bank_2* = D2/D3.

A master must consecutively transmit data to *Bank_1* and *Bank_2*, toggling the information bit I2 in the respective master calls. However, the SAP5 triggers a data output event (modification of the Data Output Ports and generation of Data Strobe) as follows (see Table 5.13):

- If the *Parallel_Out_4I/4O* flag is set (= '1') in the EEPROM (refer to Table 4.2), the SAP5 triggers a data output event only if information bit I2 is equal to '0,' in which case, new output data is issued at the Data Port synchronously for both banks at the same time.
- If the *Parallel_Out_4I/4O* flag is not set (= '0'), the SAP5 triggers a data output event at every cycle. However, depending on the information bit I2, only one bank of the Data Port gets refreshed.

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Table 5.13 Meaning of Master Call Bits I[3:0] with Ext_Addr_4I/4O_Mode = '1'

Master Call Bit	Operation / Meaning			
	***Parallel_Out_4I/4O* = '0'**		***Parallel_Out_4I/4O* = '1'**	
	I2 = '0'	**I2 = '1'**	**I2 = '0'**	**I2 = '1'**
I0 I1	D2 = I0 D3 = I1 D1 = unchanged D0 = unchanged	D2 = unchanged D3 = unchanged D1 = I1 D0 = I0	D2 = I0 D3 = I1 D1 = *DO1_tmp* 2) D0 = *DO0_tmp* 2)	D2 = unchanged 1) D3 = unchanged 1) D1 = unchanged 1) D0 = unchanged 1) *DO1_tmp* = I1 *DO0_tmp* = I0
I2	I2 = $\overline{\text{Sel}}$-bit for transmission to *Bank_1* (D0/D1) / *Bank_2* (D2/D3)			
I3	I3 = $\overline{\text{Sel}}$-bit for A-Slave/B-Slave addressing (see Table 3.2)			

1) If I2 = '1' then I0/I1 are directed to temporary data output registers *DO0_tmp*/*DO1_tmp*.

2) If I2 = '0' then I0/I1 are directed to the data output registers D2/D3 and *DO0_tmp*/*DO1_tmp* are directed to data output registers D0/D1.

In order to ensure that both *Bank_1* and *Bank_2* data are refreshed continuously, the SAP5 supervises the alternation of the I2 Sel-bit by use of the 4I/4O Watchdog.

The 4I/4O Watchdog gets activated as soon as

- The Communication Watchdog is activated (refer to section 5.17 and Table 5.22).
- The SAP5 is operated in Extended Address Mode and the *Ext_Addr_4I/4O_Mode* flag is set (= '1') in the EEPROM.
- Slave address is not equal to zero (0_{HEX}).
- No EEPROM write access is active.
- The slave is activated, i.e. the *Data_Exchange_Disable* flag is cleared ('0').

If there is no alternation of the I2 bit for more than 327ms (+16ms) after the activation of the slave, the 4I/4O Watchdog takes the following actions:

- It generates Data and Parameter Strobe signals at the DSTBn and PSTBn pins with timing according to Figure 5.2 and Figure 5.3.
- After DSTBn and PSTBn strobe generation has finished, the 4I/4O Watchdog invokes an unconditioned SAP5 reset. It sets the *Data_Exchange_Disable* flag and *afterwards* starts the SAP5 initialization procedure, switching all Data and Parameter Outputs inactive.

Input data is captured and returned to the master at every cycle, independent of the value of information bit I2.

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5.8.5. Special Function of DSTBn

In addition to the standard output function, the Data Strobe Pin serves as an external reset input for all operational modes of the SAP5. Pulling the DSTBn pin low for more than a minimum reset time generates an unconditioned reset of the SAP5, which is immediately followed by an initialization of the State Machine (EEPROM read out).

For further information on the SAP5 reset behavior, especially in regard to the signal timing, see section 5.13.

5.9. Data and Parameter Port Configuration

Data and Parameter Ports are configured by programming the *IO_Code* in the EEPROM (see Table 4.2). The configuration also depends on the *Safety_Mode_Enable* setting (see Table 4.4). Table 5.14 lists the different configurations selected by the *IO_Code* settings.

NOTE: Table 5.14 refers to slaves that are *not* running in Safety Mode (for Safety Mode details, see section 5.18)

The following configurations are possible:

- **OUT**: output only; data are valid up to the next DSTBn/PSTBn strobe pulse
- **IN**: input only; open-drain output is fixed at the high-impedance state
- **I/O**: bi-directional port with timing according to Figure 5.2 and Figure 5.3
- **INOUT**: If *IO_Code* = 7, the Parameter Ports are configured as outputs after *WPAR* master calls and as inputs after *DEXG* master calls, respectively.
- **PASSIV**: no input function and open-drain output is fixed at the high-impedance state

If any of the D0 to D3 Data Ports is configured as OUT, the SAP5 slave answer to a *DEXG* master request contains the respective information bit I[3:0] received from the master. However, Parameter Ports P[3:0] are always operated as bi-directional, including a read-back of the actual port level as described in section 5.8.

Table 5.14 Data and Parameter Port Configuration for Non-Safety-Mode Operation

Note: See important table notes at the end of the table.

IO_Code	D0	D1	D2	D3 [1)]	P0	P1	P2	P3 [1)]
0	IN	IN	IN	IN	OUT	OUT	OUT	OUT
1	IN	IN	IN	OUT	OUT	OUT	OUT	OUT
2	IN	IN	IN	I/O	OUT	OUT	OUT	OUT
3	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT
4	IN	IN	I/O	I/O	OUT	OUT	OUT	OUT
5	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT
6	IN	I/O	I/O	I/O	OUT	OUT	OUT	OUT
7 [2)]	OUT	OUT	OUT	OUT	INOUT	INOUT	INOUT	INOUT
8	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
9	OUT	OUT	OUT	IN	OUT	OUT	OUT	OUT
A	OUT	OUT	OUT	I/O	OUT	OUT	OUT	OUT

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IO_Code	D0	D1	D2	D3 [1)]	P0	P1	P2	P3 [1)]
B	OUT	OUT	IN	IN	OUT	OUT	OUT	OUT
C	OUT	OUT	I/O	I/O	OUT	OUT	OUT	OUT
D	OUT	IN	IN	IN	OUT	OUT	OUT	OUT
E	OUT	I/O	I/O	I/O	OUT	OUT	OUT	OUT
F [3)]	PASSIV	PASSIV	PASSIV	PASSIV	OUT	OUT	OUT	OUT

1) Slaves running in *Extended_Address_Mode* (*ID_Code* = A_{HEX}) will output the respective select bit (I3) at the P3 pin and also at the D3 pin if it is configured as OUT or I/O.

2) The special case *IO_Code* = 7_{HEX} causes the Parameter Ports to act as Data Inputs after *DEXG* master calls. Thus a bi-directional data exchange with separate data inputs and outputs is possible. Parameter Ports are always outputs after *WPAR* master calls. NOTE: *IO_Code* = 7_{HEX} is not allowed for the 16-pin version of the SAP5.

3) There is no data exchange possible if *IO_Code* = F_{HEX}; i.e. Data Outputs are always at the high impedance state, and no slave answer is generated upon reception of *DEXG* master calls.

Table 5.15 Data and Parameter Port Configuration in Safety Mode

Note: See section 5.18 for an explanation of F-Dx.

Package	IO_Code	D0	D1	D2	D3	P0	P1	P2	P3 [1)]
16 Pin	0 to 6 8 to F	F-D0* IN	D0* OUT	F-D2* IN	D2* OUT	don't care	don't care	don't care	don't care
16 Pin	7 [1)]	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care
20 Pin	0 to 6 8 to F	F-D0* IN	D0* OUT	F-D2* IN	D2* OUT	P0 OUT	P1 OUT	P2 OUT	P3 OUT
20 Pin	7 [2)]	D0 OUT	D1 OUT	D2 OUT	D3 OUT	F-D0* IN P0 OUT	D0* OUT P1 OUT	F-D2* IN P2 OUT	D2* OUT P3 OUT

1) *IO_Code* = 7_{HEX} is not allowed for the 16-pin version for the SAP5.

2) Parameter Ports are parameter outputs during *WPAR* master calls and after *DEXG* master calls. They are in the high impedance state after *WPAR* master calls and act as inputs when a *DEXG* master call is performed.

5.10. Fault Indication Input PFAULT

The PFAULT fault indication input pin is provided for sensing a periphery fault-messaging signal. It contains a high-voltage, high-impedance input stage that sets the status bit S1 of the AS-i Slave to '1' if it detects a low level at the PFAULT pin. The DC properties of the pin are specified in Table 5.5.

Signal transitions at the PFAULT pin are indicated in S1 with a slight delay because the signal is first processed by a clock synchronizing circuit.

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5.11. LED Outputs

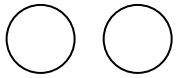
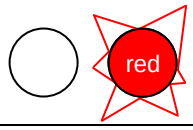
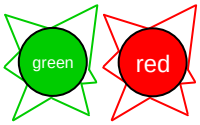
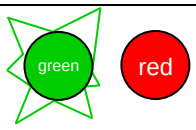
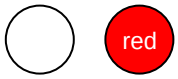
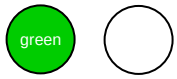
5.11.1. Slave Mode

The SAP5 provides two LED pins for enhanced status indication. LED1 and LED2 both comprise NMOS open-drain output drivers. In addition, LED2 contains a high-voltage, high-impedance input stage for purposes of the SAP5 production test.

Note: In order to comply with the signaling schemes defined in the *AS-Interface Complete Specification,* a red LED must be connected to LED2 and a green LED must be connected to LED1.

The following status indication is supported:

Table 5.16 LED Status Indication

Priority/Status	LED1 / LED 2	Notes
1. Power off		No power supply available.
2. External reset		DSTRBn pin driven low for more than 90ms.
3. Periphery fault	 Alternating	Periphery fault signal generated at PFAULT input pin as described in section 5.10.
4. No data exchange (Address = 0)		Slave is waiting for address assignment. Data Port communication is not possible.
5. No data exchange		The SAP5 was reset by the Communication Watchdog or by *RES* or *BR01* master calls; thus the *Data_Exchange_Disable* flag is still set, prohibiting Data Port communication. The SAP5 is waiting for a *Write_Parameter* request. This status is not signaled if the Communication Watchdog is not activated (see section 5.17).
6. Normal operation		Data communication is established.

The flashing frequency of any flashing status indication is approximately 2Hz.

In the case of a simultaneous occurrence of several states, the status with the highest priority is signaled.

5.11.2. Master/Repeater Mode

In the Master/Repeater Mode, LED1 provides the Manchester-II-coded, re-synchronized equivalent of the telegram signal received at the AS-i input channel.

Every AS-i telegram received is checked for consistency with the protocol specifications, and timing jitters are removed if they stay within the specified limits. If a telegram error is detected, the output becomes inactive for a certain time period; see section 5.19.3 for details.

LED2 is always logic HIGH (high impedance) in Master/Repeater. In such applications, the green LED must be connected to the UOUT pin or different supply levels.

5.12. Oscillator Pins OSC1 and OSC2

Table 5.17 Oscillator Pin Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	V_{OSC_IN}		-0.3		V_{U5R}	V
External parasitic capacitor at oscillator pins OSC1, OSC2	C_{OSC}		0		8	pF
Dedicated load capacity	C_{LOAD}			12		pF
Input ”low” voltage for external clock applied to OSC1	V_{IL}		0		1.5	V
Input ”high” voltage for external clock applied to OSC1	V_{IH}		3.5		V_{U5R}	V

The oscillator supports direct connection of 5.33MHz or 16.000MHz crystals with a dedicated load capacity of 12pF and parasitic pin capacities of up to 8pF. The SAP5 automatically detects the oscillation frequency of the connected crystal and controls the internal clock generator circuit accordingly. The oscillator unit also contains a Clock Watchdog circuit that can generate an unconditioned SAP5 reset if there has been no clock oscillation for more than about 20µs. This is to prevent the SAP5 from unpredictable behavior if the clock signal is no longer available.

5.13. SAP5 Reset

Any SAP5 reset sets the Data Output and Parameter Output Registers to F_{HEX} and forces the corresponding output drivers to the high impedance state. Except on Power-On Reset, the Data Strobe (DSTBn) and Parameter Strobe (PSTBn) signals are simultaneously generated to indicate possibly changed output data to external circuitry.

The *Data_Exchange_Disable* flag is set during an SAP5 reset, prohibiting any Data Port activity immediately after SAP5 initialization and as long as the external circuitry was not pre-conditioned by valid parameter output data. Consequently the AS-i master must send a *Write_Parameter* call in advance of the first *Data_Exchange* request to an initialized slave. The SAP5 initialization times are given in Table 5.18.

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Table 5.18 SAP5 Initialization Times

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Initialization time after Software Reset (generated by master calls *Reset_Slave* or *Broadcast_Reset*) or external reset via DSTBn [1)]	t_{INIT}			2	ms
Initialization time after power on [2)]	t_{INIT2}	$C_{UOUT} \leq 10\mu F$		30	ms
Initialization time after power-on with high capacitive load [1)]	t_{INIT3}	$C_{UOUT} = 470\mu F$		1000	ms

1) Guaranteed by design.

2) Power starts when $V_{LTGP} = 18V$ at the latest.

5.13.1. Power-On Reset

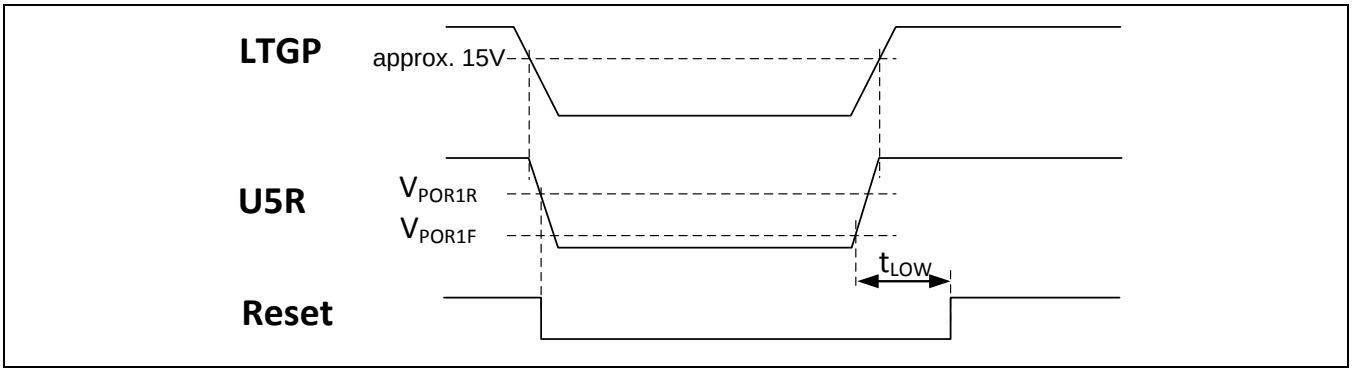
In order to force the SAP5 into a defined state after power-on and to avoid uncontrolled switching of the digital logic if the 5V supply (U5R) falls below a specified minimum level, a Power-On Reset is executed under the conditions given in Table 5.19.

Table 5.19 Power-On Reset (POR) Threshold Voltages

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
V_{U5R} voltage to trigger internal reset procedure, falling voltage [1)]	V_{POR1F}		1.2	1.7	V
V_{U5R} voltage to trigger initialization procedure, rising voltage [1)]	V_{POR1R}		3.5	4.3	V
Power-On Reset pulse width	t_{LOW}		4	6	µs

1) Guaranteed by design.

Figure 5.5 Power-On Behavior (all modes)



Note: The Power-On Reset circuit has a threshold voltage reference. This reference matches the process tolerance of the logic levels and therefore is not accurate. All values depend slightly on the rise and fall time of the supply voltage.

5.13.2. Logic Controlled Reset

The SAP5 also becomes reset after reception of *Reset_Slave* or *Broadcast_Reset* commands, expiration of the (enabled) Communication Watchdog, or entering a prohibited state machine state (i.e., due to heavy EMI).

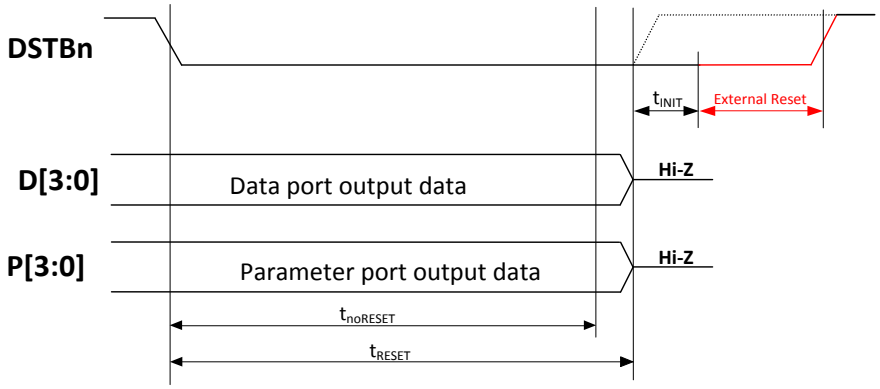
5.13.3. External Reset

The SAP5 can be reset externally by pulling the DSTBn pin LOW for more than the minimum reset time. The external reset input function is provided in every operational mode of the SAP5: Slave Mode and Master/Repeater Mode. The signal timings are given in Table 5.20.

Table 5.20 Timing of External Reset

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
DSTBn low time for no reset initiation	$t_{noRESET}$			90	ms
Reset execution time: DSTBn H/L transition to Hi-Z output drives at DO[3:0], P[3:0]	t_{RESET}			99	ms
State Machine initialization time after reset (EEPROM read out)	t_{INIT}			2	ms

Figure 5.6 Timing Diagram External Reset via DSTBn



The external reset is generated as “edge sensitive” to the expiration of the t_{RESET} timer. The initialization procedure is starting immediately after the event, independent of the state of DSTBn. The external reset state persists if DSTBn still remains low after $t_{RESET} + t_{INIT}$. The corresponding error state display is described in section 5.11.

5.14. UART

The UART performs a syntactical and timing analysis of the telegrams received at the AS-i input channel. It converts the pulse-coded AS-i input signal into a Manchester-II-coded bit stream and provides the receive register with decoded telegram bits. The UART also realizes the Manchester-II-coding of a slave answer.

In Master/Repeater Mode, the output signal of the Manchester coder (AS-i pulse to MAN signal conversion) is resynchronized and forwarded to the LED1 pin. Any pulse timing jitters of the received AS-i signal are removed if they are within the specified maximum limits. If the received AS-i telegram does not pass one of the error checks (see detailed description below), the LED1 output becomes inactive for a certain time period; see section 5.19.3.

The comparator stages at the AS-i line receiver generate two pulse-coded output signals (*p_pulse*, *n_pulse*) disjoining the positive and negative telegram pulses for further processing. To reduce UART sensitivity to erroneous spike pulses, pulse filters suppress any *p_pulse*, *n_pulse* activity of less than 750ns width. After filtering, the *p_pulse* and *n_pulse* signals are checked in accordance with the *AS-Interface Complete Specification* for the following telegram transmission errors:

Start_bit_error The initial pulse following a pause must have negative polarity. Violation of this rule is detected as a *Start_bit_error*. The first pulse is the reference for bit decoding. The first bit detected must be the value 0.

Alternating_error Two consecutive pulses must have different polarity. Violation of this rule is detected as an *Alternating_error*.

Note: A negative pulse must be followed by a positive pulse and vice versa.

Timing_error Within any master request or slave response, the digital pulses that are generated by the receiver are checked to start in periods of $(n * 3\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 to 26 for a master request and n = 1 to 12 for a slave response. Violation of this rule is detected as a *Timing_error.*

Note: There is a certain pulse timing jitter associated with the receiver output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages. In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the *AS-Interface Complete Specification*.

No_information_error Derived from the Manchester-II-Coding rule, either a positive or negative pulse must be detected in periods of $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 to 13 for a master request and n = 1 to 6 for a slave response. Violation of this rule is detected as a *No_information_error*.

Note: The timing specification relates to the receiver comparator output signals. There is a certain pulse timing jitter in the digital output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages. In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the *AS-Interface Complete Specification*.

Parity_error The sum of all information bits in master requests or slave responses (excluding the start and end bits, including the parity bit) must be even. Violation of this rule is detected as a *Parity_error.*

End_bit_error The pulse to be detected $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start pulse must be of positive polarity, where n = 13 (78µs) for a master request and n = 6 (36µs) for a slave response. Violation of this rule is detected as an *End_bit_error.*

Note: This stop pulse must finish a master request or slave response.

Length_error Telegram length supervision is processed as follows. If during the first bit time after the end pulse of a master request (equivalent to the 15th bit time) for synchronized slaves, or during the first three bit times for non-synchronized slaves (equivalent to the bit times 15 to 17), or during the first bit time after the end pulse of a slave response (equivalent to the 8th bit time), a signal other than a pause is detected, a *Length_error* is detected.

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If one or more of these errors occurs, the received telegram is treated as invalid. In this case, the UART will not generate a Receive Strobe signal. It moves to asynchronous state and waits for a pause at the AS-i line input. After a pause has been detected, the UART is ready to receive the next telegram.

Receive Strobe signals are generally used to validate the correctness of the received data. A Receive Strobe starts the internal processing of a master request. If the UART was in asynchronous state before the signal was generated, it transforms to synchronous state afterwards. If the received slave address matches the stored address of the SAP5, the transmitter is turned on by the Receive Strobe pulse, allowing the output driver to settle smoothly at the operation point (avoiding false pulses at the AS-i line).

5.15. Main State Machine

The Main State Machine controls the overall behavior of the SAP5. Depending on the configuration data stored in the EEPROM, the State Machine activates one of the different SAP5 operational modes and controls the digital I/O ports accordingly. In Slave Mode, it processes the received master telegrams and computes the contents of the slave answer if required. Table 3.2 lists all master calls that are decoded by the SAP5 in Slave Mode. To prevent the critical situation in which the SAP5 becomes locked in a prohibited state (e.g., due to exposure to strong electromagnetic radiation), which could jeopardize the entire system, all prohibited states of the state machine will lead to an unconditioned logic reset which is comparable to the AS-i call *Reset_Slave* (*RES*).

5.16. Status Registers

Table 5.21 shows the SAP5 status register content. The use of status bits S0, S1, and S3 is compliant with the *AS-Interface Complete Specification*. Status bit S2 is not used. The status register content can be determined by use of a *Read_Status* (*RDST*) master request (refer to Table 3.2).

Table 5.21 Status Register Content

Status Register Bit	Sx = 0	Sx = 1
S0	EEPROM write accessible	Stored slave address volatile and/or EEPROM access blocked (write in progress) [1)]
S1	No Periphery Fault detected; EEPROM Firmware Area and Safety Area content consistent	Periphery fault detected; parity bit error in EEPROM Firmware Area or Safety Area
S2	Static zero	N/A
S3	EEPROM content consistent [2)]	EEPROM contains corrupted data [2)]

1) Status bit S0 is set to ‘1’ as soon as a *DELA* master request was received and the slave address was not equal to “0” before the request. It is also set for the entire duration of each EEPROM write access.

2) See section 4.2.

5.17. Communication Monitor/Watchdog

The SAP5 contains an independent Communication Monitor that observes the processing of *Data_Exchange* (*DEXG*) and *Write_Parameter* (*WPAR*) requests. If no such requests have been processed for more than 94.2ms (+4ms) the Communication Monitor recognizes a No Data/Parameter Exchange status and turns the red status LED (i.e., LED2) on. Any subsequent *Data_Exchange* or *Write_Parameter* request will allow the Communication Monitor to start over and will turn the red status LED off.

The Communication Monitor is only activated for a slave addresses not equal to zero (0_{HEX}) and while the SAP5 is processing the first *Write_Parameter* request after initialization. It becomes deactivated at any SAP5 reset or after the reception of a *Delete_Address* request.

Activation of the Communication Watchdog depends on several EEPROM flags and the Parameter Port P0 output register.

Note: The value of the Parameter Port P0 input does not have any influence on the Communication Watchdog activation. Only the master can change the activation status by sending a corresponding *Write_Parameter* (*WPAR*) request. This allows using the feature even if *IO_Code* = 7 is selected. In this case, the Parameter Port pins are mapped into Data Input pins. However, since the activation of the Communication Watchdog only depends on the value of the parameter output register, the watchdog functionality still remains controlled by the master.

Watchdog activation through the value of the Parameter Port P0 is not available in Safety Mode.

***Table 5.22 Activation of the SAP5* Communication Watchdog**

***Lock_EE_PRG* EEPROM flag**	***Inhibit_Watchdog* EEPROM flag**	***P0_Watchdog_Activation* EEPROM flag**	***Safety_Mode_ Enable***	**Parameter Port P0 Output Register**	**Watchdog Activation**
0	X	X	X	X	OFF
1	1	X	X	X	OFF
1	0	0	X	X	ON
1	0	1	1	X	ON
1	0	1	0	0	OFF
1	0	1	0	1	ON

The Communication Watchdog recognizes a No Data Exchange status if all of the following conditions are true:

- The Communication Watchdog is activated.
- No DEXG or WPAR request has been processed for more than 94.2ms (+4ms).
- Slave address is not equal to zero (0_{HEX}).
- No EEPROM write access is active.

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If the Communication Watchdog detects a No Data Exchange status, it takes the following actions:

- It concurrently generates the Data and Parameter Strobe signals at the DSTBn and PSTBn pins with timing according to Figure 5.3 and Figure 5.2 respectively. NOTE: At this time, the data and parameter output values still comply with the values received with the last *DEXG* and *WPAR* master call, respectively.
- After the DSTBn and PSTBn strobe generation has finished, the Communication Watchdog invokes an unconditioned SAP5 reset. It sets the *Data_Exchange_Disable* flag and *afterwards* starts the SAP5 initialization procedure, switching all Data and Parameter Outputs inactive.

In order to resume normal Data Port communication after a Watchdog SAP5 Reset, the *Data_Exchange_Disable* flag must be cleared again. Therefore, the master must send a *WPAR* request again before the Data Port communication can be re-established. This ensures new parameter setup of any connected external circuitry.

The state until the *Data_Exchange_Disable* flag returns to '0' is signaled by a certain LED1 and LED2 status indication (refer to section 5.11).

5.18. Safety Mode (SAP5S only)

The Safety Mode is active as soon as the EEPROM flag *Safety_Mode_Enable* is set to '1' (logic high). Thus, it is basically independent of the slave profile; whereas the assignment of the 3-level-input pins discussed below to either the Data or Parameter Port depends on the *IO_Code* as described in Table 5.15.

Furthermore, in order to fulfill specific security requirements, the Safety Mode is not combinable with any of the following SAP5 features:

- Delay Mode (section 5.8.2)
- Synchronous Data I/O Mode (section 5.8.3)
- Ext_Addr_4I/4O_Mode (section 5.8.4)
- P0 Watchdog Activation (section 5.17)

The Safety Mode of the SAP5 is of relevance to the actions following an *DEXG* master request. Instead of the regular input data provided at the data ports, a 4-bit data word from a specific $8 * 4$ bit code table as described in the third-party document *Specification of safe AS-i transmission* (see section 9.2) is transmitted to the master. Cycling the code table is used to transmit another data word with each *DEXG* master call.

In order to meet specific safety requirements, the data words transmitted to the master pass through a special pre-processing. Therefore, the code table stored within the Safety Area of the EEPROM (refer to Table 4.4) does not match the reference code table as specified in the *Specification of Safe AS-i Transmission* but is derived from a special coding scheme as described in Table 5.23. See the requirements below the table for the explanation of the asterisks in the table.

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Table 5.23 Example for Cryptographic Code Table

Note: an asterisk (*) is used to indicate bits that have changed from the original bit.

Reference Code Table				**Step 1: Cycle D0/D2 by One Cycle**				**Step 2: Invert D0/D2**				**Step 3: Swap D1 – D3 Code Table Written to the EEPROM**				
D3	D2	D1	D0	D3	D2	D1	D0	D3	D2*	D1	D0*	D3*	D2*	D1*	D0*	*swap_flag*
0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1
0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0
0	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	1
1	0	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0
1	1	1	0	1	0	1	1	1	1	1	0	1	1	1	0	0
1	0	1	1	1	1	1	0	1	0	1	1	1	0	1	1	1
1	1	0	0	1	1	0	1	1	0	0	0	0	0	1	0	1
0	1	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0

The EEPROM code table must be derived from a Reference Code Table that meets the following requirements:

1. Looking up in the Reference Code Table, the data bit vectors D0 and D2 are scrolled forward by one cycle. Refer to Table 5.23 for an example.
2. Data bit vectors D0 and D2 are inverted and stored as D0* and D2* in the EEPROM.
3. Four out of eight data bits from the vector D1 are interchanged with the respective data bits from vector D3. The respective bits are marked with *swap_flag* = ‘1’. Unchanged data bit pairs are marked with *swap_flag* = ‘0’. Coded in such a way, the vectors are stored as D1* and D3* in the EEPROM.
4. The additional *swap_flag* attached to each data word is stored in the EEPROM as well.

Running in Safety Mode, the EEPROM data bits D0* and D2* are put out at the port D1/D3 or P1/P3, respectively (for port configuration, refer to Table 5.15). An external circuit must invert these signals, which adds a voltage offset (refer to Figure 5.8) and delays it for about 20µs. Thus the data actually will be transmitted with the subsequent AS-i cycle. Furthermore, the safety-related switches are connected between the external circuitry and the SAP5 safety inputs F-D0* and F-D2* (refer to Figure 5.7).

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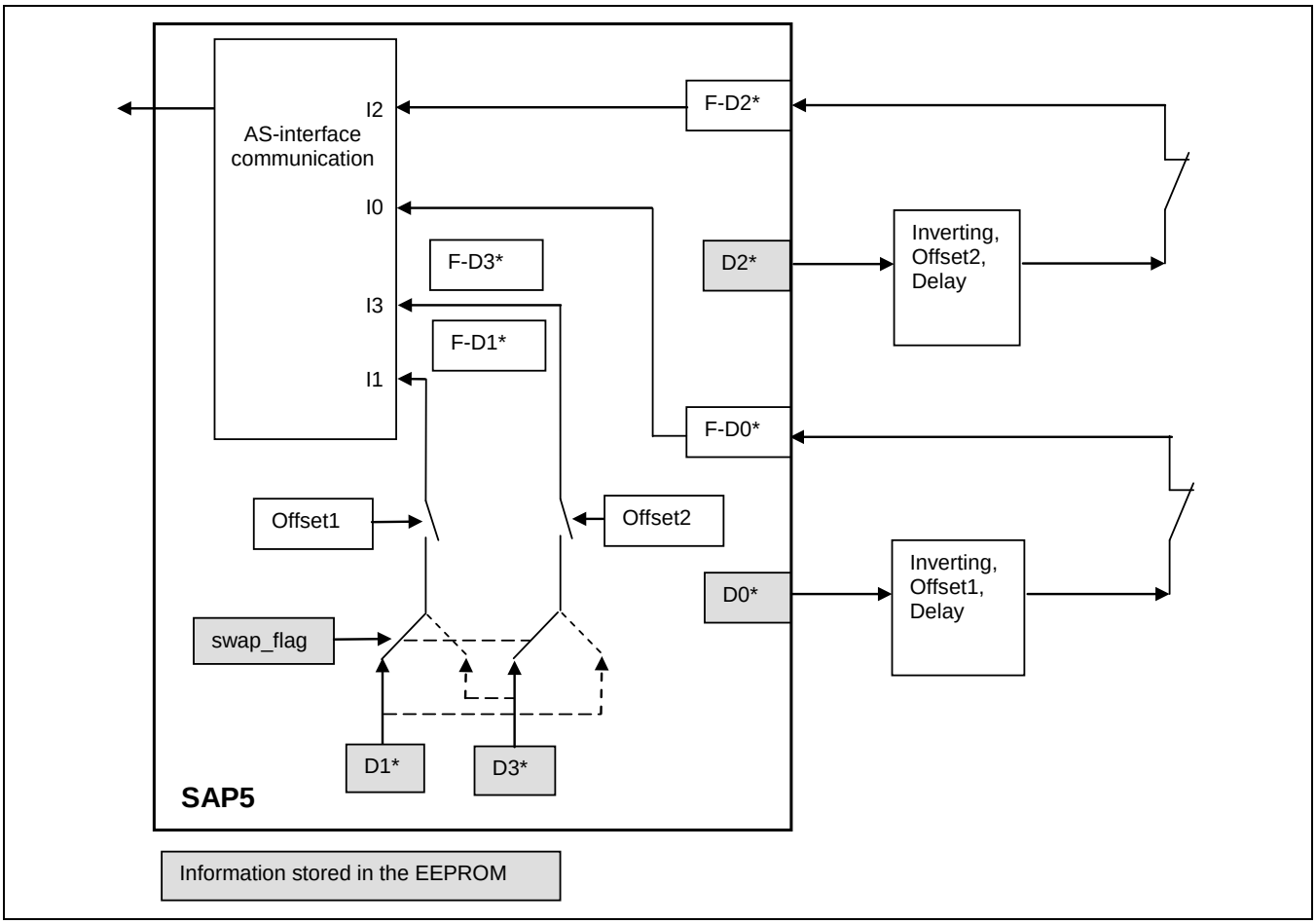
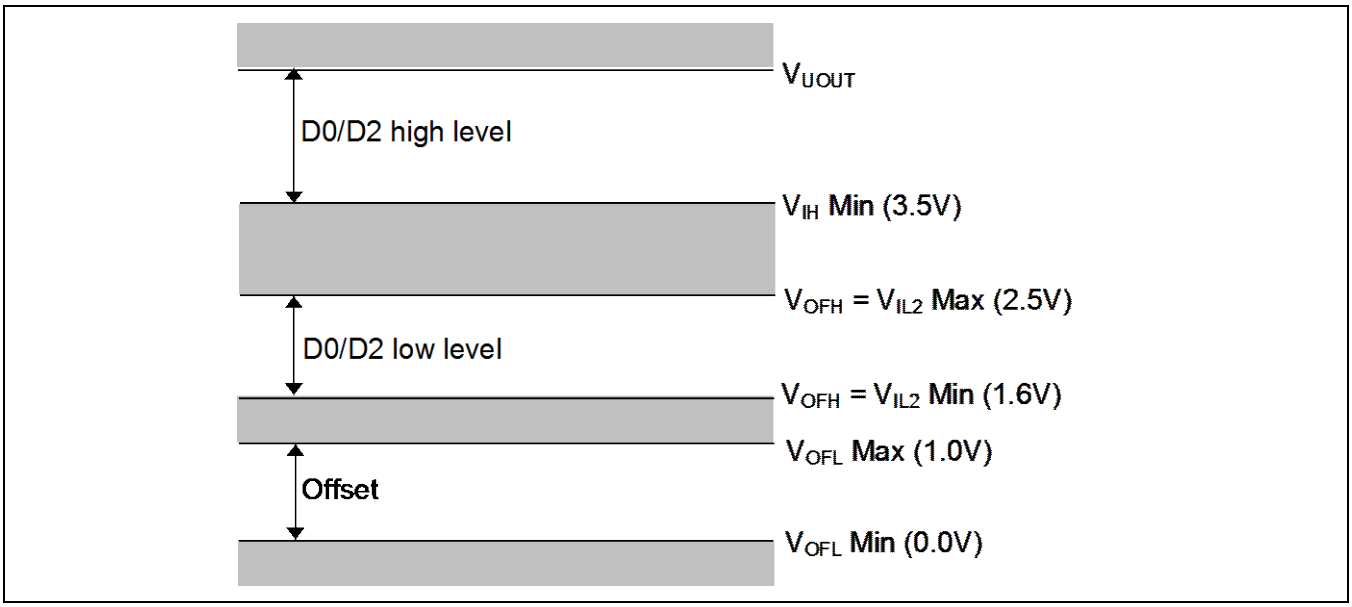
Figure 5.7 Safety Mode Data Processing



The special input ports F-D0* and F-D2* act as 3-level-input pins in Safety Mode. In order to ensure proper decoding of input data, the voltages must satisfy requirements as specified in below Figure 5.8 and in Table 5.5.

Figure 5.8 Data Input Voltage Constraints in Safety Mode



As soon as the F-D0* input pad detects an offset level less than V_{OFL}(Max), the SAP5 resets the data input for D1 (F-D1*), signaling an OPEN state at the safety switch connected to D0*. The input data for D3 (F-D3*) will be reset if F-D2* detects an offset level less than V_{OFL}(Max).

Provided that the offset levels are not missing, the EEPROM bits D1* and D3* are transmitted as data bits D1 and D3 if *swap_flag* = '0'; otherwise they are swapped.

In order to avoid desynchronization with the safety monitor in case the AS-i master repeats a *DEXG* call, the SAP5 will not update the data code word for 224µs (+16µs) after a *DEXG* call had been processed.

5.19. Master and Repeater Modes

5.19.1. Master/ Repeater Mode Activation

The SAP5 Master/Repeater Mode functionality is enabled via the *Master_Mode* EEPROM flag (refer to Table 4.2). In order to activate the *Master_Mode*, an SAP5 Reset (see section 5.13) must be performed after programming the EEPROM *Master_Mode* flag.

For the distinction between Master and Repeater Mode, the *ID_Code* can be set to a specific value as described in Table 5.24.

NOTE: The *ID_Code* must be programmed **before** activation of the *Master_Mode* flag. Once the *Master_Mode* flag is set to logic high, the slave functionality of the SAP5 is no longer available, preventing any write access to the EEPROM by use of AS-i master requests as described in section 4.3.

Moreover, the Master and Repeater Mode functionality can be disabled generally by use of a hidden EEPROM flag. This flag is inaccessible by the user, but can be set during the IDT production test.

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Table 5.24 Activation of the SAP5 **Master/Repeater Mode**

Master_Mode EEPROM flag	ID_Code	Master Mode 1	Master Mode 2	Repeater Mode
0	x	OFF	OFF	OFF
1	0 to 4	ON	OFF	OFF
1	6 to F_{HEX}	OFF	ON	OFF
1	5	OFF	OFF	ON

5.19.2. Pin Assignment in Master and Repeater Modes

In Master and Repeater Mode, the SAP5 pins are configured as follows. Pins that are not used are kept at logic high (high impedance) state in order to reduce internal power dissipation of the SAP5.

Figure 5.9 SAP Package Pin Assignment in Master/Repeater Mode

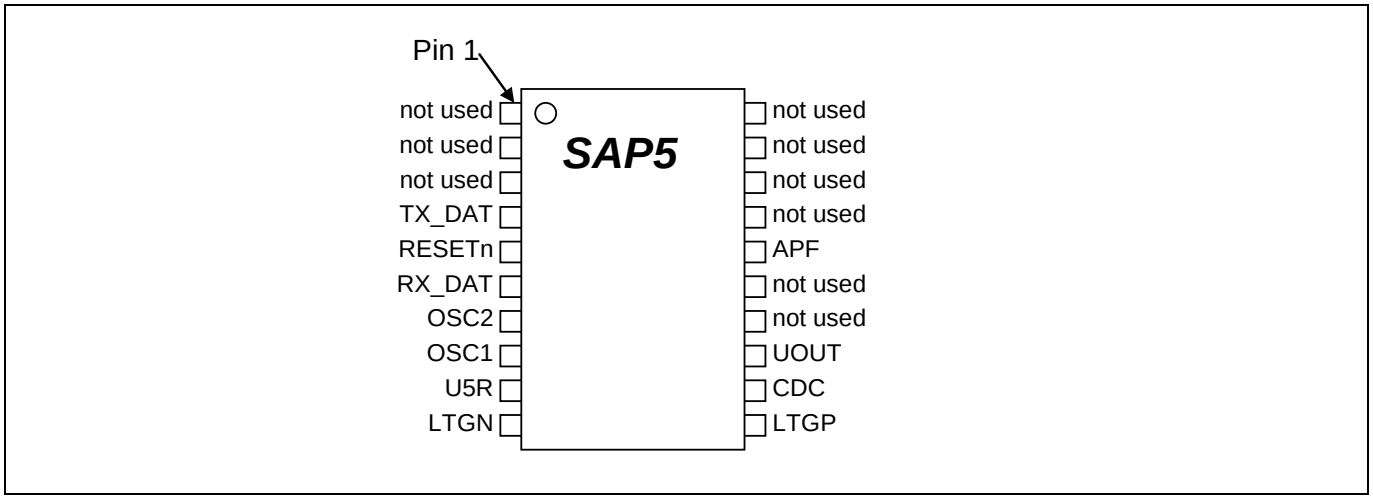

Table 5.25 SAP5 Pin Assignment in Master and Repeater Modes

SOP 20 Pin #	SOP 16 Pin #	Name	Signal Name	Pin Configuration	Description
			in Master/Repeater Mode		
1	-	P1	None	I/O	Not used
2	-	P0	None	I/O	Not used
3	1	D1	None	I/O	Not used
4	2	D0	TX_DAT	IN	Transmit signal (Manchester II signal)
5	3	DSTBn	RESETn	IN	External reset input (active LOW)
6	4	LED1	RX_DAT	OUT	Receive signal (Manchester II signal)
7	5	OSC2	OSC2	OUT	Crystal oscillator

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SOP 20 Pin #	SOP 16 Pin #	Name	Signal Name	Pin Configuration	Description
			in Master/Repeater Mode		
8	6	OSC1	OSC1	IN	Crystal oscillator / external clock input
9	7	U5R	U5R	OUT	Regulated 5V power supply
10	8	LTGN	LTGN	IN	AS-i Transmitter/Receiver output; to be connected to ASi-
11	9	LTGP	LTGP	IN	AS-i Transmitter/Receiver input, to be connected to ASi+ via reverse polarity protection diode; input for the power fail comparator
12	10	CDC	CDC	OUT	External buffer capacitor
13	11	UOUT	UOUT	OUT	Decoupled actuator/sensor power supply
14	12	PFAULT	None	IN	Not used
15	13	LED2	None	OUT	Not used
16	14	PSTBn	APF	OUT	AS-i power fail signal
17	15	D3	None	I/O	Not used
18	16	D2	None	I/O	Not used
19	-	P3	None	I/O	Not used
20	-	P2	None	I/O	Not used

5.19.3. Functional Description

In Master/Repeater Mode, the SAP5 provides a simple physical-layer interface function between the AS-i line and an external binary channel.

The signal *RX_DAT* represents the Manchester-II-coded, re-synchronized equivalent of the telegram signal received at the AS-i input channel. Polarity of that bit stream depends on the programmed operation mode according to Table 5.26.

Table 5.26 Functional Differences between SAP5 Master and Repeater Modes

	Modulation of Signal *RX_DAT* if AS-i Power Fails	Loopback Mode	Polarity of signal RX_DAT
Master Mode 1	ON	ON	Active HIGH
Master Mode 2	OFF	ON	Active HIGH
Repeater Mode	OFF	OFF	Active LOW

Every AS-i telegram received is checked for consistency with the protocol specifications and timing jitters are removed if they are within the specified limits. If a telegram error is detected, the output signal becomes inactive for a time period defined by t_{BREAK} (refer to Table 5.28).

The signal *TX_DAT* is directly forwarded to the AS-i line transmitter avoiding any additional logic delays.

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If the Loopback Mode is not active, the AS-i receiver is disabled while the SAP5 is transmitting an AS-i signal. Otherwise, the transmitted signal is read back in parallel and provided at the *RX_DAT* output for checkup purposes.

The loopback time $t_{LOOPBACK}$ is mainly defined by the analog signal processing within the Receiver and the Transmitter. However, an additional delay of up to 1875ns can be inserted if necessary. Therefore, the ID_*Code_Extension_2* EEPROM register must be programmed as described below.

NOTE: The *ID_Code_Extension_2* must be programmed *before* programming of the *Master_Mode* flag. Once the *Master_Mode* flag is set to logic high, the slave functionality of the SAP5 is no longer available, preventing any write access to the EEPROM by use of AS-i master requests as described in section 4.3.

Table 5.27 Programmable Variation of the Loopback Time

ID_Code_Extension_2 **(*ID2_Bit3* to *ID2_Bit0*)**	$\Delta t_{loopback}$
0000	0
0001	+125ns
0010	+250ns
0011	+375ns
0100	+500ns
0101	+625ns
0110	+750ns
0111	+875ns
1000	+1000ns
1001	+1125ns
1010	+1250ns
1011	+1375ns
1100	+1500ns
1101	+1625ns
1110	+1750ns
1111	+1875ns

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In Master/Repeater Mode, the SAP5 provides an AS-i power-fail detector. It consists of a comparator directly connected to the LTGP pin that generates a logic signal if the voltage at the LTGP pin drops below V_{APF} (refer to Table 5.28).

A subsequent digital signal processing of the comparator output signal is performed as follows:

- An anti-bouncing filter removes any signal states shorter than 6µs. This is to eliminate the influence of AS-i telegrams that are added onto the AS-i DC voltage.
- An additional anti-bouncing filter with different filter times for activation and deactivation of the power-fail signal removes short power-fail pulses.
- The AS-i power-fail signal is provided directly active high as the signal *APF*.
- Additionally, in Master Mode, the AS-i power-fail signal modulates the *RX_DAT* signal; whereas the active state is signaled by logic high level.

Table 5.28 Master/Repeater Mode Parameter

Parameter	Symbol	Min	Max	Unit
Loopback time in *Master Mode* [1)]	$t_{LOOPBACK}$	4.9	6.5	µs
AS-i Power Fail voltage threshold	V_{APF}	21.5	23.5	V
Minimum activation time for signaling of AS-i Power Fail by use of the *RX_DAT* signal [2)]	$t_{APF\_RX\_DAT}$	640	704	µs
Release time of the AS-i Power Fail state within the *RX_DAT* signal [2)]	$t_{APF\_ON\_RX\_DAT}$	64		µs
Minimum activation time for signaling of AS-i Power Fail by use of the APF signal [2)]	t_{APF_APF}	704	768	µs
AS-i Power Fail hold time	t_{HOLD_APF}	64		µs
Delay time after return of the AS-i power	t_{APF_OFF}	64	128	µs
Break time in case of an erroneous AS-i signal	t_{BREAK}	9	15	µs

1) Loopback time is the time difference between an edge in the MAN code of signal *TX_DAT* and the corresponding edge in the Manchester-code of the signal RX_DAT. The voltage trigger level for measurement of the edge time is defined by $V_{U5R}/2$. The actual loopback time may be adjusted by programming the *ID_Code_Extension_2* EEPROM register as described in Table 5.27.

2) In Master Mode, the AS-i Power Fail state is already signaled by the *RX_DAT* signal as soon as the power fail condition is true for a time more than $t_{APF\_RX\_DAT}$. However, in order to start the APF minimum hold state (t_{HOLD_APF}), the power fail condition must remain true for another time period defined by $t_{APF\_ON\_RX\_DAT}$. Otherwise, the *RX_DAT* signal returns to its idle state (logic low) immediately.

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5.20. Write Protection of *ID_Code_Extension_1*

The *ID_Code_Extension_1* register of the SAP5 can either be manufacturer configurable or user configurable. As soon as the *Lock_EE_PRG* flag is set, access to the *ID_Code_Extension_1* is handled as follows:

- If the flag *Inhibit_Write_ID1* is set ('1') in the Firmware Area of the EEPROM, *ID_Code_Extension_1* is manufacturer configurable (refer to Table 4.2).
- In this case, the slave response to a *Read_ID_Code_1* (*RID1*) request is constructed out of the data stored on the internal EEPROM address 2 in User Area of the EEPROM.
- It does not matter which data is stored in the *ID_Code_Extension_1* register in EEPROM address 1 in the User Area. The SAP5 will always respond with the protected manufacturer programmed value.
- There is one exception to this principle. If the SAP5 is operated in Extended Address Mode, bit 3 of the returned slave response is taken from the EEPROM address 1 register in the User Area. This is because bit 3 functions as the A/B Slave selector bit in this case and must remain user configurable.
- To ensure consistency of the *ID_Code_Extension_1* stored in the data image of Master as well as in the EEPROM of the slave, the SAP5 *will not process a Write_Extended_ID_Code_1 request* if the data sent does not match the data that is stored in the protected part of the *ID_Code_Extension_1* register. It will neither access the EEPROM nor send a slave response in this case.
- Note: As defined in the *AS-Interface Complete Specification*, a modification of the A/B Slave selector bit must be performed bit selective. That means the AS-i master must read the *ID_Code_Extension_1* first, modify bit 3, and send the new 4-bit word that consists of the modified bit 3 and the unmodified bits 2 to 0 back to the slave.
- If the *Inhibit_Write_ID1* flag is *not* set ('0'), *ID_Code_Extension_1* is completely user configurable. The data to construct the slave response to a *Read_ID_Code_1* request is completely taken from the *ID_Code_Extension_1* register on EEPROM address 1 in the User Area.
- A *Write_Extended_ID_Code_1* request will always be answered and initiate an EEPROM write access procedure in this case.

Manufacturer configuration of the *ID_Code_Extension_1* register is only possible as long as the *Lock_EE_PRG* flag is not yet set. In this case, the *Write_Extended_ID_Code_1* request causes a write access that differs from the procedure described on page 20. Instead of the *Security_Flag* procedure, the *ID_Code_Extension_1* is written to both EEPROM addresses 1 and 2 in the User Area of the EEPROM. This method of duplicate saving ensures data consistency even in the case of an accidental interruption of the EEPROM write process during modification of bit 3 in Extended Address Mode. Refer to Table 5.29 for an overview of the different programming and read out options of *ID_Code_Extension_1.*

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Table 5.29 Write Protection of ID_Code_Extension_1

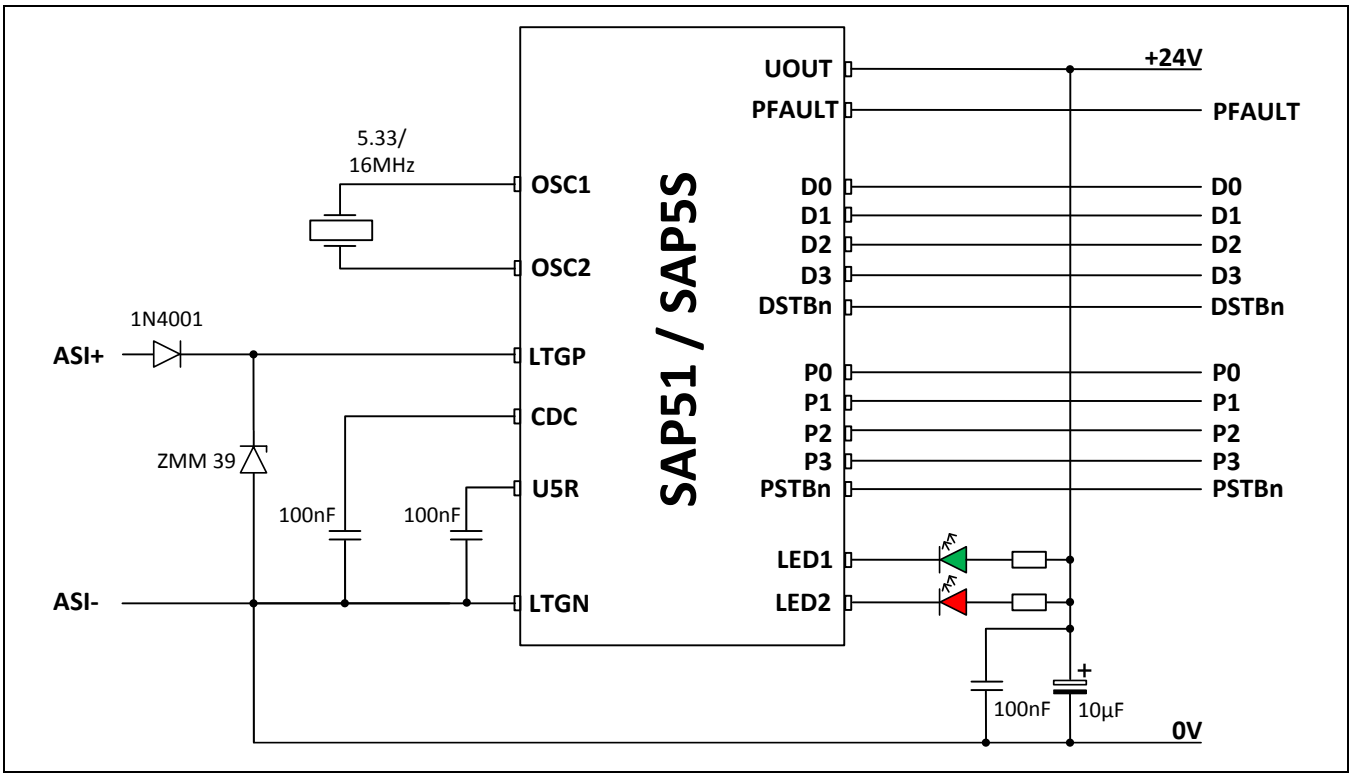
Master Call	*ID_Code*	*Lock_EE_PRG*	*Inhibit_Write_ID1*	Reaction	Slave Answer
WID1	≠ A_{HEX}	0	0	Write *ID1_user* + *ID1_manufacturer* (User Area address 1 and 2)	Yes
			1	New ID1 matches *ID1_manufacturer*: write *ID1_user* + *ID1_manufacturer*	Yes
				New ID1 does not match *ID1_manufacturer*: No action	No
		1	0	Write *ID1_user*	Yes
			1	New ID1 matches *ID1_manufacturer*: Write *ID1_user*	Yes
				New ID1 does not match *ID1_manufacturer*: No action	No
	A_{HEX}	0	0	Write *ID1_user* + *ID1_manufacturer*	Yes
			1	New ID1[2:0] matches *ID1_manufacturer*[2:0]: write *ID1_user* + *ID1_manufacturer*	Yes
				New ID1[2:0] does not match *ID1_manufacturer*[2:0]: No action	No
		1	0	Write *ID1_user*	Yes
			1	New ID1[2:0] matches *ID1_manufacturer*[2:0]: write *ID1_user*	Yes
				New ID1[2:0] does not match *ID1_manufacturer*[2:0]: No action	No
RID1	≠ A_{HEX}	0	0	Return *ID1_user*	Yes
			1	Return *ID1_manufacturer*	
		1	0	Return *ID1_user*	
			1	Return *ID1_manufacturer*	
	A_{HEX}	0	0	Return *ID1_user*	
			1	Return *ID1_user*[3], *ID1_manufacturer*[2:0]	
		1	0	Return *ID1_user*	
			1	Return *ID1_user*[3], *ID1_manufacturer*[2:0]	

The slave answer to a *Write_ID_Code1* request is ‘0’ in any case as specified in Table 3.2.

6 Application Circuits

The following figures show typical application cases of the SAP5. Note that these schematics show only basic circuits principles. For more detailed application information, see the separate *SAP51/SAP5S Application Notes* document. Figure 6.1 outlines a standard slave application circuit. Figure 6.2 shows a Safety Mode application circuit. A Master Mode application is shown in Figure 6.3.

Figure 6.1 Standard Application Circuit, Direction of Data I/O Depends on IO_Code



For the circuit shown in Figure 6.2, R1 and C1 form a low-pass-filter for the delay of the output of the SAP5 for about 20µs. The transistor performs the inversion; the voltage divider R2/R3 shifts the low level in the range of 1.5V to 2.5V. The high level is provided from the pin's pull-up feature.

Figure 6.2 Safety Mode Application

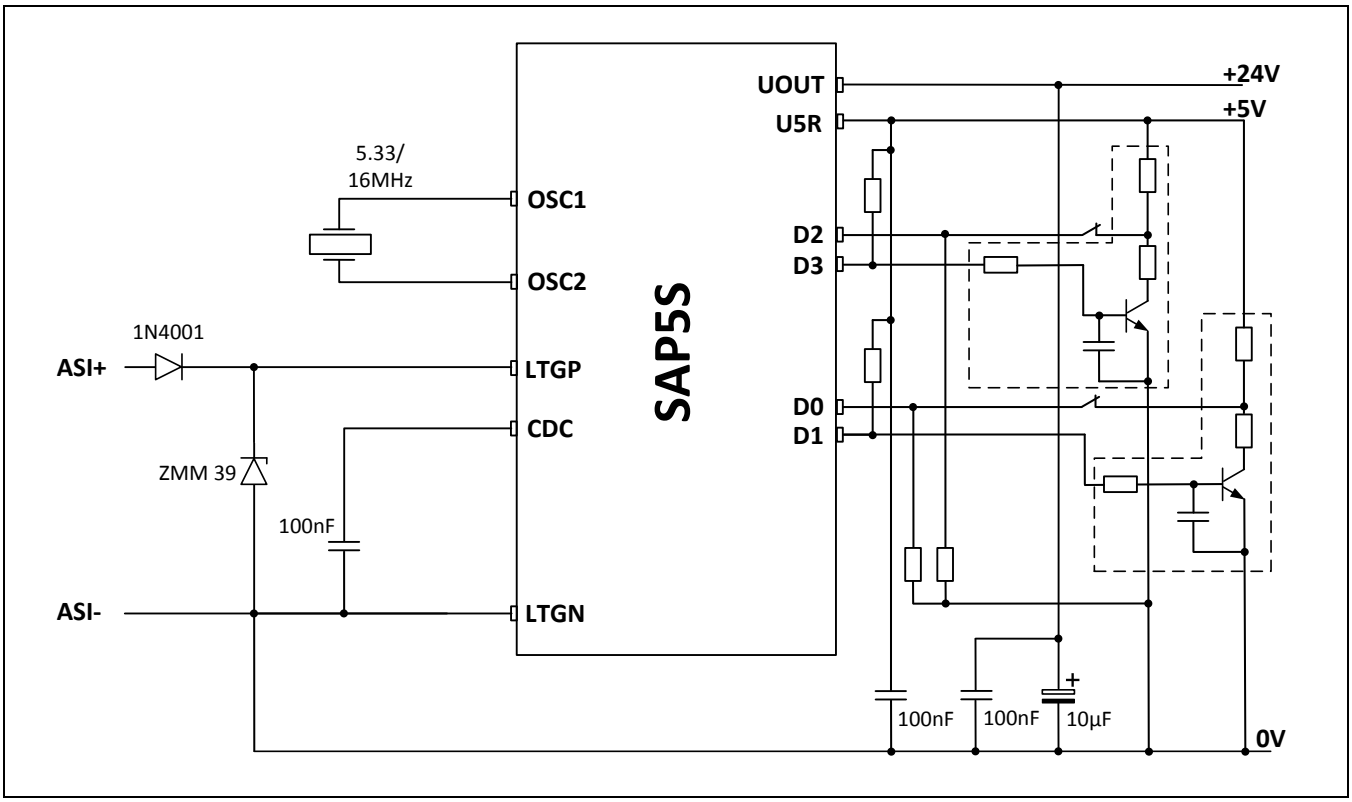
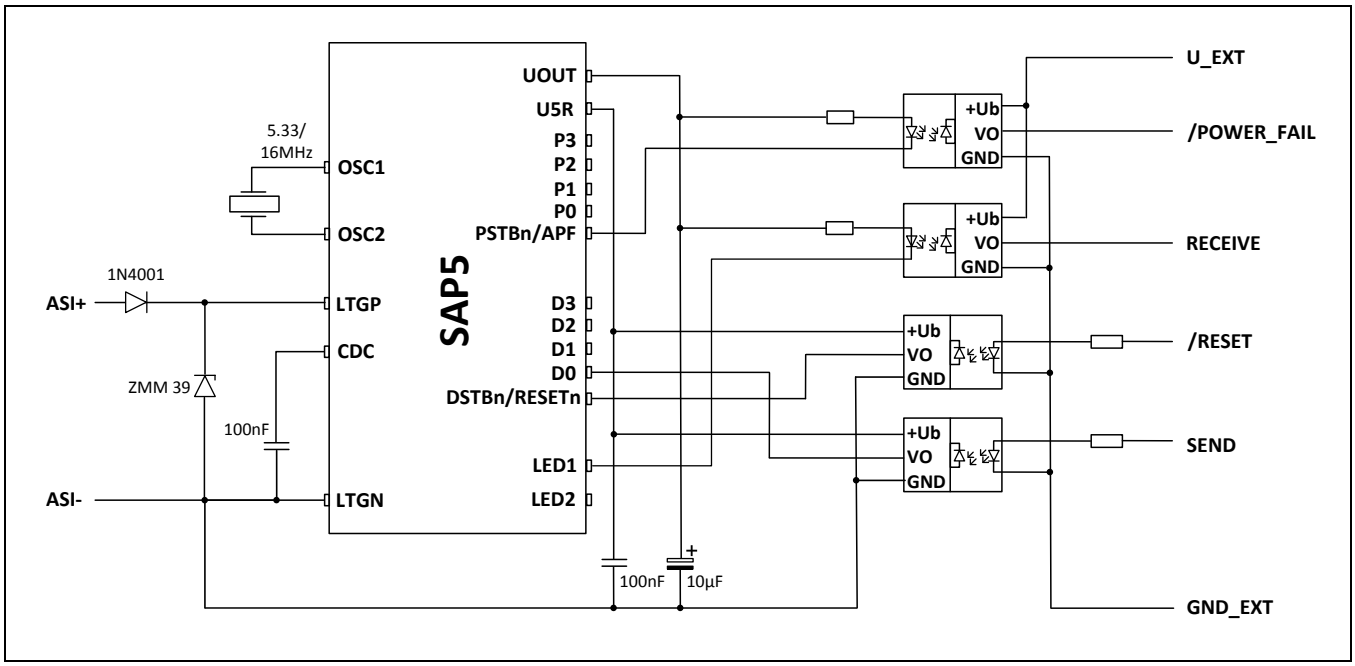


Figure 6.3 SAP5 Master Mode Application



7 Package Specifications

7.1. Package Pin Assignment

Table 7.1 SAP51/SAP5S Package Pin List

SOP 20 Pin	SOP 16 pin	Name	Direction	Type	Description
1	-	P1	I/O	Pull-up / open-drain (*)	Parameter Port P1 / Data Input Port 1 if *IO_config* = 7
2	-	P0	I/O	Pull-up / open-drain (*)	Parameter Port P0 / Data Input Port 0 if *IO_config* = 7
3	1	D1	I/O	Pull-up / open-drain	Data Port D2
4	2	D0	I/O	Pull-up / open-drain	Data Port D0
5	3	DSTBn	I/O	Pull-up / open-drain	Data Strobe Output / Reset Input
6	4	LED1	OUT	Open-drain	LED 1 Status Indication
7	5	OSC2	OUT	Analog (5V)	Crystal Oscillator
8	6	OSC1	IN	Analog / CMOS (5V)	Crystal Oscillator / External Clock Input
9	7	U5R	OUT	Analog	Regulated 5V Power Supply
10	8	LTGN	IN	Analog / Supply	AS-i Transmitter/Receiver Output; to be connected to ASi-
11	9	LTGP	IN	Analog / Supply	AS-i Transmitter/Receiver Input; to be connected to ASi+ via reverse polarity protection diode
12	10	CDC	OUT	Analog	External Buffer Capacitor
13	11	UOUT	OUT	Analog	Decoupled Actuator/Sensor Power Supply
14	12	PFAULT	IN	Pull-up	Periphery Fault Input (Low = Periphery Fault)
15	13	LED2	OUT	Open drain	LED 2 Status Indication
16	14	PSTBn	I/O	Pull-up / open-drain	Parameter Strobe Output
17	15	D3	I/O	Pull-up / open-drain	Data Port D3
18	16	D2	I/O	Pull-up / open-drain	Data Port D2
19	-	P3	I/O	Pull-up / open-drain (*)	Parameter Port P3 / Data Input Port 3 if *IO_config* = 7
20	-	P2	I/O	Pull-up / open-drain (*)	Parameter Port P2 / Data Input Port 2 if *IO_config* = 7
(*) The pull-up current source on these parameter ports is switched off if the slave device is programmed with I/O configuration code 7 and a *DEXG* master call is processed.					

All open-drain outputs are NMOS-based. Pull-up properties at input stages are achieved by current sources referenced to U5R.

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Figure 7.1 SAP51/SAP5S SOP20 Package Pin Assignment

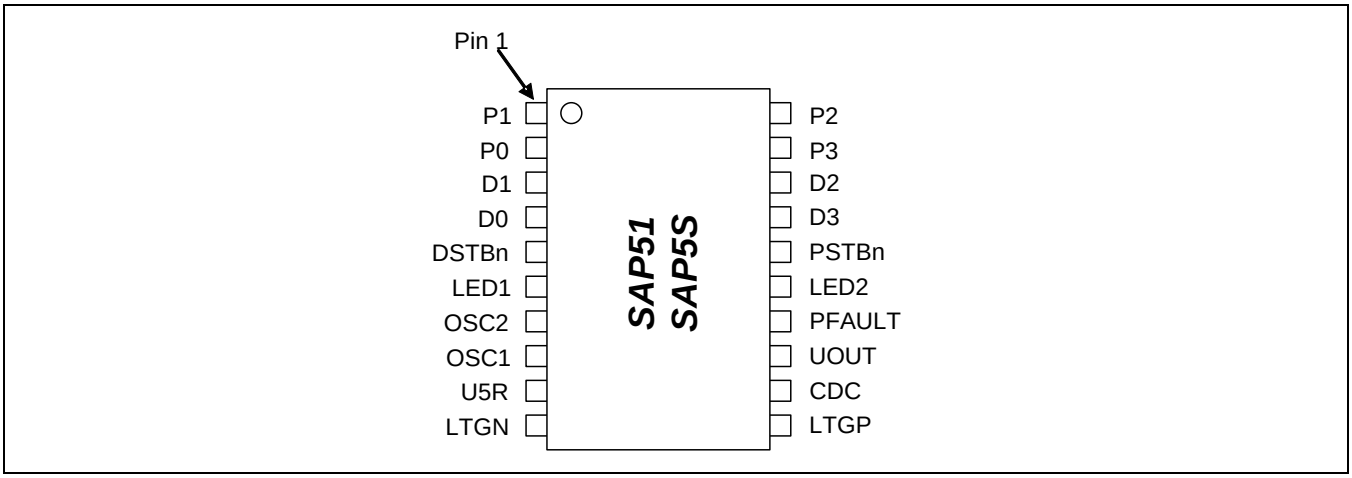
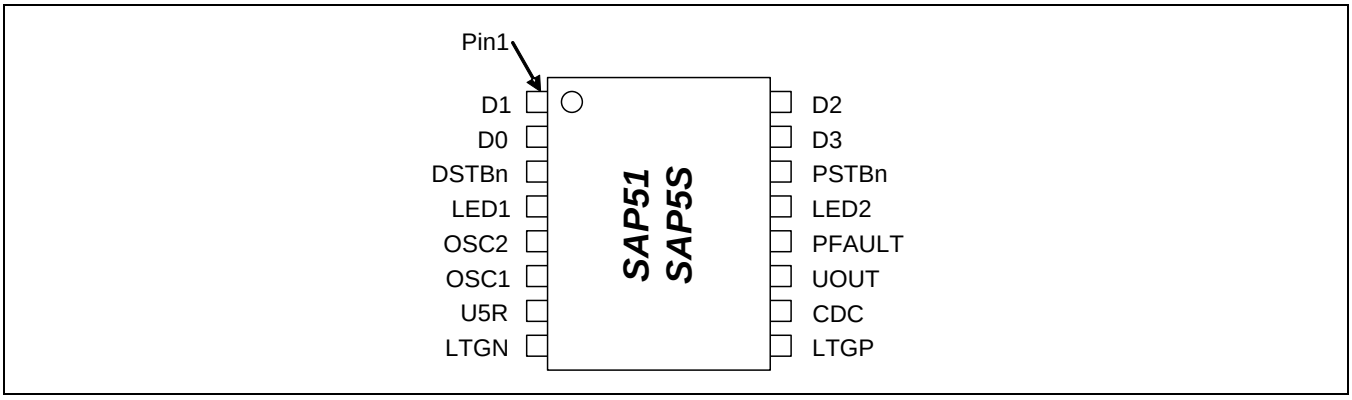


Figure 7.2 SAP51 / SAP5S SOP16 Package Pin Assignment



7.2. SOP16 (300 mil) Package Outline

The SAP51/SAP5S is available in a 16-pin SOP package. Its dimensions are given in Figure 7.3 and Table 7.2.

Figure 7.3 SOP16 Package Outline Dimensions

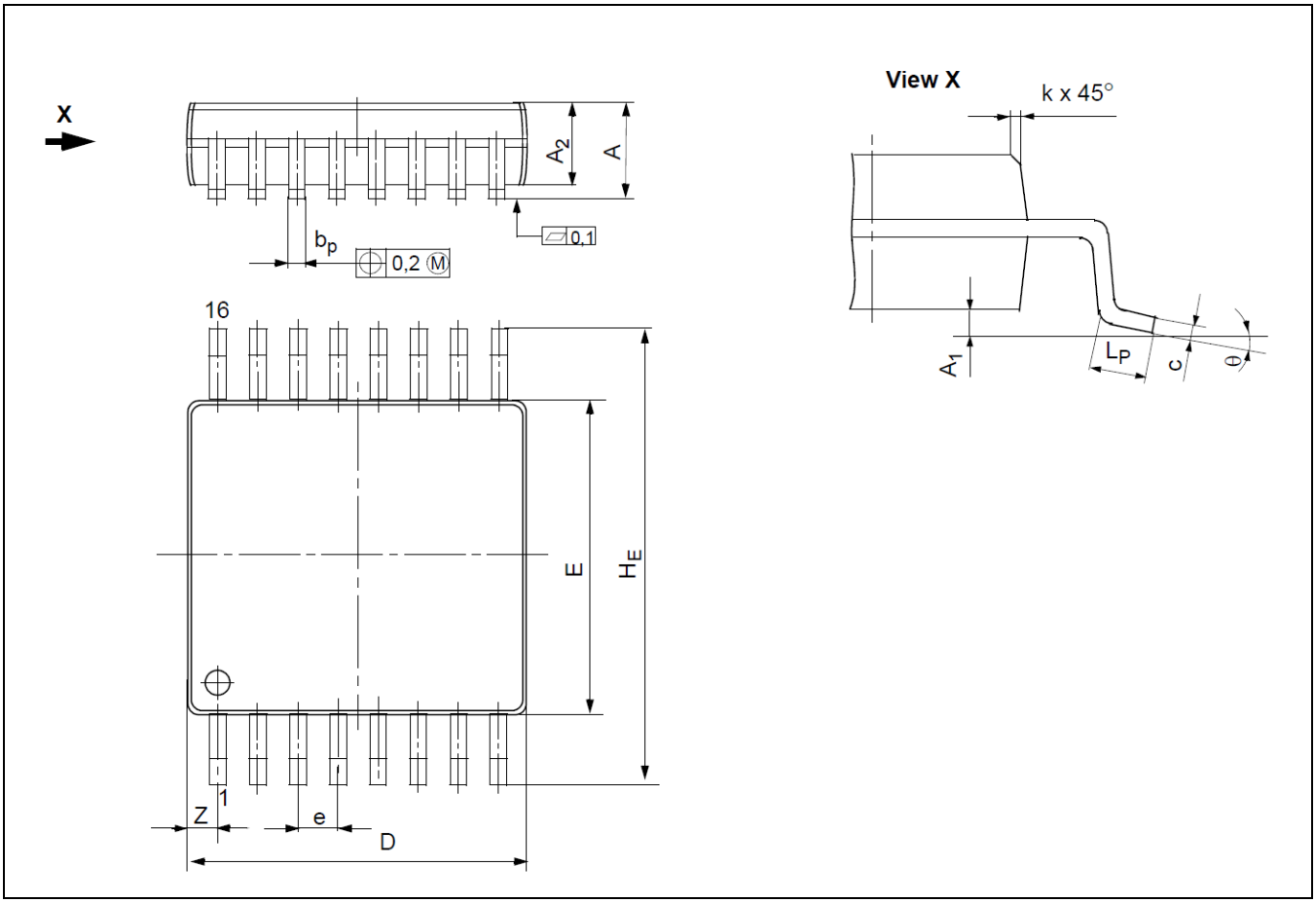


Table 7.2 SOP16 Package Dimensions (mm)

SYMBOL	A	A_1	A_2	b_P	c	e	D	E	H_E	k	L_P	Z	θ
Nominal						1.27							
Minimum	2.35	0.10	2.25	0.35	0.23		10.21	7.40	10.00	0.25	0.61		0°
Maximum	2.65	0.30	2.45	0.49	0.32		10.46	7.60	10.65			0.79	8°

7.3. SOP20 (300 mil) Package Outline

The SAP51/SAP5S is available in a 20-pin SOP package. The dimensions are given in Figure 7.4 and Table 7.3.

Figure 7.4 SOP20 Package Outline Dimensions

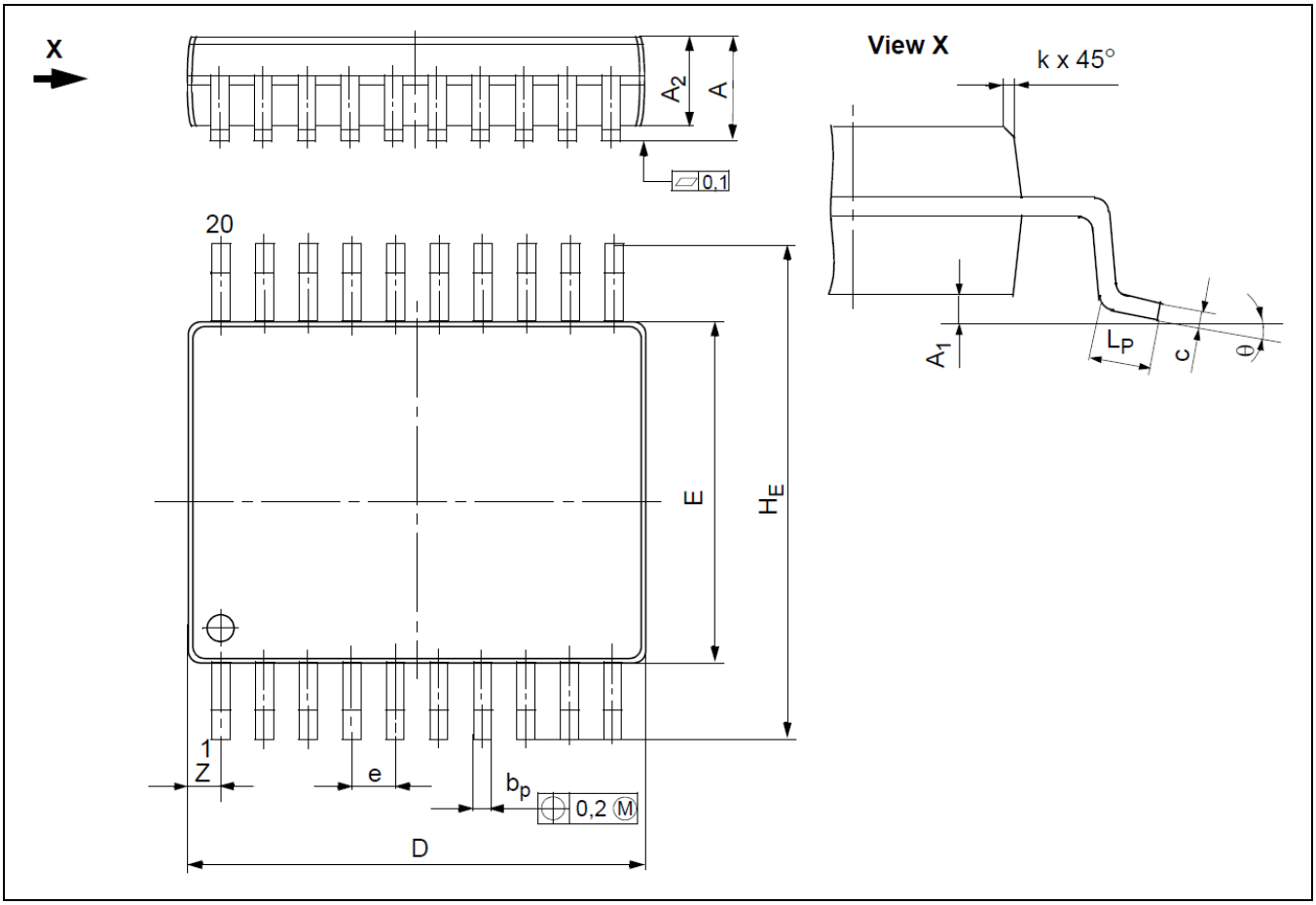


Table 7.3 SOP20 Package Dimensions (mm)

SYMBOL	A	A_1	A_2	b_P	c	e	D	E	H_E	k	L_P	Z	θ
Nominal						1.27							
Minimum	2.35	0.10	2.25	0.35	0.23		12.60	7.40	10.00	0.25	0.40		0°
Maximum	2.65	0.30	2.45	0.49	0.32		13.00	7.60	10.65			0.81	8°

7.4. Package Marking

Figure 7.5 Package Marking 20-Pin Version

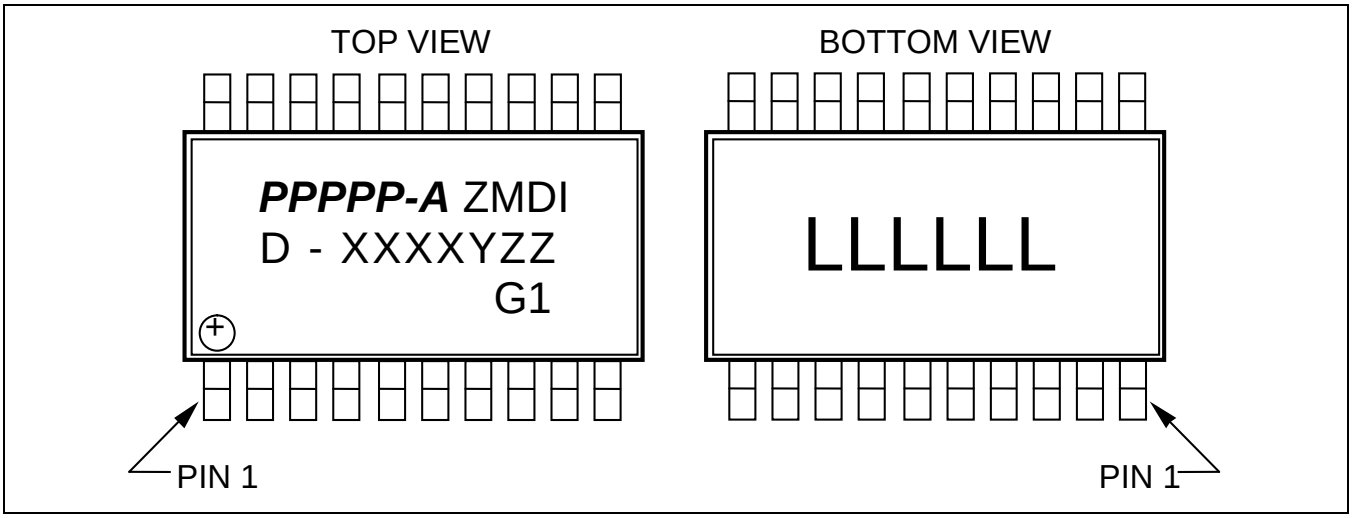
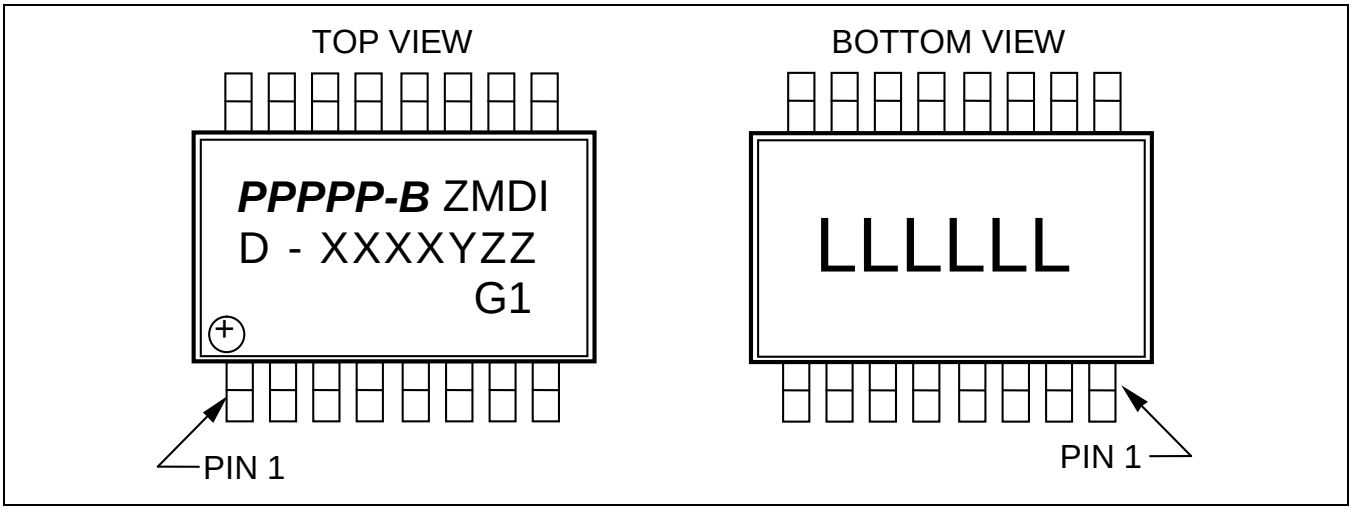


Figure 7.6 Package Marking 16-Pin Version



Top Marking:

PPPPP-A	Product name SOP20 Package
PPPPP-B	Product name SOP16 Package
ZMDI	Manufacturer
D	Revision code
YYWW	Date code (year and week)
L	Assembly location
ZZ	Traceability code

Bottom Marking:

LLLLLL	IDT Lot Number

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8 Ordering Information

Ordering Code	Operating Temperature	Package Type	RoHS?	Packaging
SAP5SD-A-G1-T	-25°C to +85°C	SOP20 / 300 mil	Yes	Tubes (37 parts/tube)
SAP51D-A-G1-T				
SAP5SD-A-G1-R	-25°C to +85°C	SOP20 / 300 mil	Yes	Tape and Reel (1000 parts/reel)
SAP51D-A-G1-R				
SAP5SD-B-G1-T	-25°C to +85°C	SOP16 / 300 mil	Yes	Tubes (46 parts/tube)
SAP51D-B-G1-T				
SAP5SD-B-G1-R	-25°C to +85°C	SOP16 / 300 mil	Yes	Tape and Reel (1000 parts/reel)
SAP51D-B-G1-R				

9 Related Documents

9.1. Related IDT Documents

Document
SAP5 /SAP5S Feature Sheet
SAP51/SAP5S Application Notes *
SAP51/SAP5S Release Note Rev D
SAP51/SAP5S Errata Sheet
Management Regulation: 0410 Product Development Procedure **
Process Specification: IDT C7D 0.6µm Technology **

Visit the *SAP5S/SAP51* web page at http://www.IDT.com/products/as-interface/SAP5 or contact your nearest sales office for the latest version of these documents.

* Documents marked with an asterisk (*) require a free customer login for access.

** Documents marked with two asterisks (**) are available only on request.

9.2. Related Third-Party Documents

Document	Related Web Site
AS-Interface Complete Specification Version 3.0 Rev5, 11.12.2013	www.as-interface.net
Specification of Safe AS-i Transmission V2.01, 12.05.2000	www.as-interface.net

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10 Glossary

Term	Description
AS-i	Actuator Sensor Interface
PLC	Programmable logic controller
PLL	Phase-Lock Loop
UART	Universal Asynchronous Receiver/Transmitter

11 Document Revision History

Revision	Date	Description
1.00	September 13, 2005	First release.
2.00	March 21, 2007	IC Revision C introduced
2.10	April 2, 2007	Update ordering information
2.20	April 11, 2008	Update to JEDEC-020D
3.00	March 20, 2011	New template and minor changes.
3.10	July 17, 2012	IC Revision D added
3.20	June 17, 2015	New template applied. Update for contact information. Addition of definitions for absolute maximum ratings and operating conditions for section 2. Correction of references to UIN and DSR pins, which are not applicable. Revisions for formatting. Minor edits for clarity.
	January 28, 2016	Changed to IDT branding.

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