

**FEATURES**

- ▶ JESD204B (Subclass 1) coded serial digital outputs
  - ▶ Lane rates up to 15 Gbps
- ▶ 1.66 W total power dissipation at 500 MSPS
  - ▶ 415 mW per ADC channel
- ▶ SFDR = 82 dBFS at 305 MHz (1.80 V p-p input range)
- ▶ SNR = 66.8 dBFS at 305 MHz (1.80 V p-p input range)
- ▶ Noise density = -151.5 dBFS/Hz (1.80 V p-p input range)
- ▶ 0.975 V, 1.8 V, and 2.5 V dc supply operation
- ▶ No missing codes
- ▶ Internal ADC voltage reference
- ▶ Analog input buffer
- ▶ On-chip dithering to improve small signal linearity
- ▶ Flexible differential input range
  - ▶ 1.44 V p-p to 2.16 V p-p (1.80 V p-p nominal)
- ▶ 1.4 GHz analog input full power bandwidth
- ▶ Amplitude detect bits for efficient AGC implementation
- ▶ 4 integrated wideband digital processors
  - ▶ 48-bit NCO, up to 4 cascaded half-band filters
- ▶ Differential clock input
- ▶ Integer clock divide by 1, 2, 4, or 8 (see Figure 1)
- ▶ On-chip temperature diode

- ▶ Flexible JESD204B lane configurations

**ENHANCED PRODUCT FEATURES**

- ▶ Supports defense and aerospace applications (AQEC standard)
- ▶ Military temperature range (-55°C to +105°C)
- ▶ Controlled manufacturing baseline
- ▶ One assembly/test site
- ▶ One fabrication site
- ▶ Product change notification
- ▶ Qualification data available on request

**APPLICATIONS**

- ▶ Communications
  - ▶ Diversity multiband, multimode digital receivers
    - ▶ 3G/4G, W-CDMA, GSM, LTE, LTE-A
- ▶ General-purpose software radios
- ▶ Ultrawideband satellite receivers
- ▶ Instrumentation
- ▶ Radars
- ▶ Signals intelligence (SIGINT)

**FUNCTIONAL BLOCK DIAGRAM**

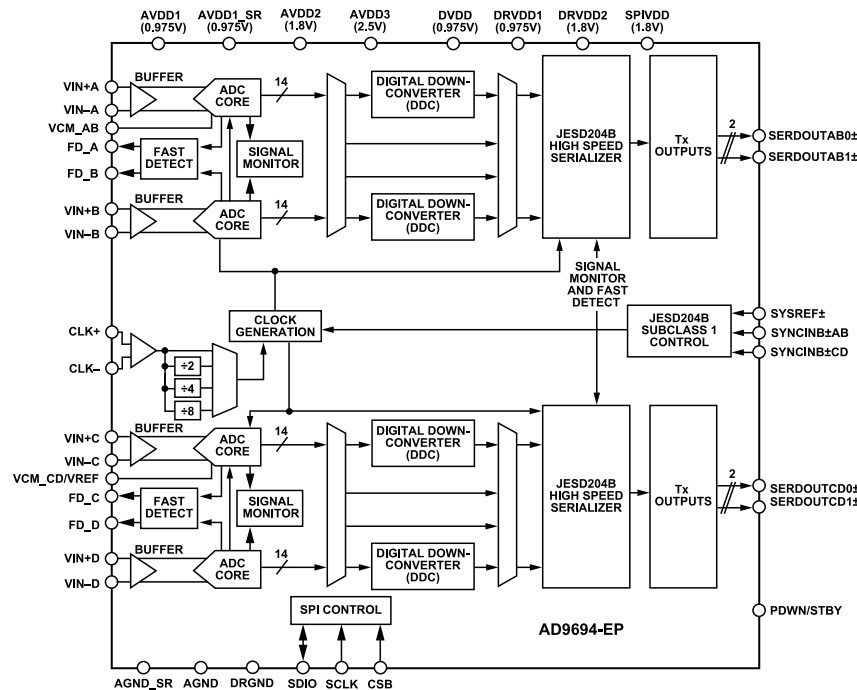


Figure 1. Functional Block Diagram

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**REVISION HISTORY****5/2023—Rev. 0 to Rev. A**

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**3/2023—Revision 0: Initial Version**

## GENERAL DESCRIPTION

The AD9694-EP is a quad, 14-bit, 500 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide bandwidth analog signals of up to 1.4 GHz. The AD9694-EP is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The quad ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog inputs and clock signals are differential inputs. Each pair of ADC data outputs is internally connected to two digital down-converters (DDCs) through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 48-bit frequency translator, numerically controlled oscillator (NCO) and up to four half-band decimation filters.

In addition to the DDC blocks, the AD9694-EP has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure each pair of intermediate frequency (IF) receiver outputs onto either one or two lanes of Subclass 1 JESD204B-based, high speed serialized outputs, depending on the decimation ratio and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF $\pm$ , SYNCINB $\pm$ AB, and SYNCINB $\pm$ CD input pins.

The AD9694-EP has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using the 1.8 V capable, 3-wire serial port interface (SPI).

The AD9694-EP is available in a Pb-free, 72-lead LFCSP and is specified over the  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  ambient temperature range.

Additional application and technical information can be found in the [AD9694](#) data sheet.

## PRODUCT HIGHLIGHTS

1. Low power consumption per channel.
2. JESD204B lane rate support up to 15 Gbps.
3. Wide full power bandwidth supports IF sampling of signals up to 1.4 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

## SPECIFICATIONS

## DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1\_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and analog input ( $A_{IN}$ ) = -1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating  $T_A$  range of -55°C to +105°C. Typical specifications represent performance at  $T_A = 25^\circ\text{C}$ .

Table 1. DC Specifications

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY		Guaranteed		
No Missing Codes				
Offset Error		0		% FSR
Offset Matching		0		% FSR
Gain Error	16		24	% FSR
Gain Matching		1.0	3.7	% FSR
Differential Nonlinearity (DNL)	-0.7	±0.4	+0.7	LSB
Integral Nonlinearity (INL)	-5.1	±1.0	+5.1	LSB
TEMPERATURE DRIFT				
Offset Error		8		ppm/°C
Gain Error		214		ppm/°C
INTERNAL VOLTAGE REFERENCE		0.5		V
INPUT REFERRED NOISE		2.6		LSB RMS
ANALOG INPUTS				
Differential Input Voltage Range (Programmable)	1.44	1.80	2.16	V p-p
Common-Mode Voltage ( $V_{CM}$ )		1.34		V
Differential Input Capacitance <sup>1</sup>		1.75		pF
Differential Input Resistance		200		Ω
Analog Input Full Power Bandwidth		1.4		GHz
POWER SUPPLY				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
AVDD1 Current ( $I_{AVDD1}$ )		319	482	mA
AVDD1_SR Current ( $I_{AVDD1\_SR}$ )		21	53	mA
AVDD2 Current ( $I_{AVDD2}$ )		438	473	mA
AVDD3 Current ( $I_{AVDD3}$ )		87	103	mA
DVDD Current ( $I_{DVDD}$ ) <sup>2</sup>		121	180	mA
DRVDD1 Current ( $I_{DRVDD1}$ ) <sup>1</sup>		162	207	mA
DRVDD2 Current ( $I_{DRVDD2}$ ) <sup>1</sup>		23	29	mA
SPIVDD Current ( $I_{SPIVDD}$ )		1	1.6	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers) <sup>2</sup>		1.66	2.07	W
Power-Down Dissipation		325		mW
Standby <sup>3</sup>		1.20		W

## SPECIFICATIONS

- <sup>1</sup> All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.  
<sup>2</sup> Full bandwidth mode.  
<sup>3</sup> Standby mode is controlled by the SPI.

## AC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1\_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and  $A_{IN} = -1.0$  dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating  $T_A$  range of  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . Typical specifications represent performance at  $T_A = 25^{\circ}\text{C}$ .

Table 2. 500 MSPS AC Specifications

Parameter <sup>1</sup>	$A_{IN}$ Full Scale = 1.44 V p-p			$A_{IN}$ Full Scale = 1.80 V p-p			$A_{IN}$ Full Scale = 2.16 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ANALOG INPUT FULL SCALE		1.44			1.80			2.16		V p-p
NOISE DENSITY <sup>2</sup>		-149.7			-151.5			-153.0		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR) <sup>3</sup>										
Input frequency ( $f_{IN}$ ) = 10 MHz		65.4			67.1			68.4		dBFS
$f_{IN} = 155$ MHz		65.3		64.8	67.0			68.3		dBFS
$f_{IN} = 305$ MHz		65.2			66.8			68.0		dBFS
$f_{IN} = 450$ MHz		65.0			66.6			67.8		dBFS
$f_{IN} = 765$ MHz		64.8			66.5			67.5		dBFS
$f_{IN} = 985$ MHz		64.5			66.0			66.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
$f_{IN} = 10$ MHz		65.3			67.0			68.2		dBFS
$f_{IN} = 155$ MHz		65.2		64.5	66.8			67.9		dBFS
$f_{IN} = 305$ MHz		65.1			66.6			67.6		dBFS
$f_{IN} = 450$ MHz		65.0			66.4			67.3		dBFS
$f_{IN} = 765$ MHz		64.7			66.1			66.9		dBFS
$f_{IN} = 985$ MHz		64.2			65.5			66.2		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
$f_{IN} = 10$ MHz		10.5			10.8			11.0		Bits
$f_{IN} = 155$ MHz		10.5		10.4	10.8			10.9		Bits
$f_{IN} = 305$ MHz		10.5			10.7			10.9		Bits
$f_{IN} = 450$ MHz		10.5			10.7			10.8		Bits
$f_{IN} = 765$ MHz		10.4			10.6			10.8		Bits
$f_{IN} = 985$ MHz		10.3			10.6			10.7		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)										
$f_{IN} = 10$ MHz		89			90			80		dBFS
$f_{IN} = 155$ MHz		89		75	85			77		dBFS
$f_{IN} = 305$ MHz		82			82			78		dBFS
$f_{IN} = 450$ MHz		82			83			77		dBFS
$f_{IN} = 765$ MHz		77			75			72		dBFS
$f_{IN} = 985$ MHz		82			79			76		dBFS
SFDR AT $-3$ dBFS										
$f_{IN} = 10$ MHz		94			94			86		dBFS
$f_{IN} = 155$ MHz		94			90			82		dBFS
$f_{IN} = 305$ MHz		89			90			83		dBFS
$f_{IN} = 450$ MHz		87			86			84		dBFS
$f_{IN} = 765$ MHz		82			80			77		dBFS

## SPECIFICATIONS

Table 2. 500 MSPS AC Specifications (Continued)

Parameter <sup>1</sup>	$A_{IN}$ Full Scale = 1.44 V p-p			$A_{IN}$ Full Scale = 1.80 V p-p			$A_{IN}$ Full Scale = 2.16 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{IN} = 985$ MHz		85			82			79		dBFS
WORST HARMONIC, SECOND OR THIRD										
$f_{IN} = 10$ MHz		-89			-90			-80		dBFS
$f_{IN} = 155$ MHz		-89			-85	-75		-77		dBFS
$f_{IN} = 305$ MHz		-82			-82			-78		dBFS
$f_{IN} = 450$ MHz		-82			-83			-77		dBFS
$f_{IN} = 765$ MHz		-77			-75			-72		dBFS
$f_{IN} = 985$ MHz		-82			-79			-76		dBFS
WORST HARMONIC, SECOND OR THIRD AT -3 dBFS										
$f_{IN} = 10$ MHz		-94			-94			-86		dBFS
$f_{IN} = 155$ MHz		-94			-90			-82		dBFS
$f_{IN} = 305$ MHz		-89			-90			-83		dBFS
$f_{IN} = 450$ MHz		-87			-86			-84		dBFS
$f_{IN} = 765$ MHz		-82			-80			-77		dBFS
$f_{IN} = 985$ MHz		-85			-82			-79		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC										
$f_{IN} = 10$ MHz		-96			-98			-99		dBFS
$f_{IN} = 155$ MHz		-97			-97	-86		-97		dBFS
$f_{IN} = 305$ MHz		-97			-98			-97		dBFS
$f_{IN} = 450$ MHz		-95			-96			-96		dBFS
$f_{IN} = 765$ MHz		-92			-91			-88		dBFS
$f_{IN} = 985$ MHz		-90			-89			-86		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), $A_{IN1}$ AND $A_{IN2} = -7$ dBFS										
$f_{IN1} = 154$ MHz and $f_{IN2} = 157$ MHz		-93			-90			-84		dBFS
$f_{IN1} = 302$ MHz and $f_{IN2} = 305$ MHz		-90			-90			-84		dBFS
CROSSTALK <sup>4</sup>		82			82			82		dB
FULL POWER BANDWIDTH <sup>3</sup>		1.4			1.4			1.4		GHz

<sup>1</sup> See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

<sup>2</sup> Noise density is measured at a low  $A_{IN}$  frequency (30 MHz).

<sup>3</sup> See the [AD9694](#) data sheet for more details.

<sup>4</sup> Crosstalk is measured at 155 MHz with a -1.0 dBFS  $A_{IN}$  on one channel and no input on the adjacent channel.

Table 3. 600 MSPS AC Specifications,  $A_{IN} = 1.80$  V p-p

Parameter <sup>1</sup>	Min	Typ	Max	Unit
$A_{IN}$ FULL SCALE		1.80		V p-p
SNR				
$f_{IN} = 10$ MHz		66.6		dBFS
$f_{IN} = 155$ MHz		67		dBFS
$f_{IN} = 305$ MHz		66.8		dBFS
$f_{IN} = 450$ MHz		66.4		dBFS
$f_{IN} = 765$ MHz		66		dBFS
$f_{IN} = 985$ MHz		65.5		dBFS
SINAD				
$f_{IN} = 10$ MHz		66.5		dBFS

## SPECIFICATIONS

Table 3. 600 MSPS AC Specifications,  $A_{IN} = 1.80$  V p-p (Continued)

Parameter <sup>1</sup>	Min	Typ	Max	Unit
$f_{IN} = 155$ MHz		66.8		dBFS
$f_{IN} = 305$ MHz		66.5		dBFS
$f_{IN} = 450$ MHz		66.3		dBFS
$f_{IN} = 765$ MHz		65.4		dBFS
$f_{IN} = 985$ MHz		64.8		dBFS
SFDR				
$f_{IN} = 10$ MHz		86		dBFS
$f_{IN} = 155$ MHz		81		dBFS
$f_{IN} = 305$ MHz		81		dBFS
$f_{IN} = 450$ MHz		84		dBFS
$f_{IN} = 765$ MHz		76		dBFS
$f_{IN} = 985$ MHz		75		dBFS
WORST HARMONIC, SECOND OR THIRD				
$f_{IN} = 10$ MHz		-86		dBFS
$f_{IN} = 155$ MHz		-81		dBFS
$f_{IN} = 305$ MHz		-81		dBFS
$f_{IN} = 450$ MHz		-84		dBFS
$f_{IN} = 765$ MHz		-76		dBFS
$f_{IN} = 985$ MHz		-75		dBFS

<sup>1</sup> See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

Table 4. 600 MSPS Power Consumption

Parameter	Min	Typ	Max	Unit
POWER SUPPLY				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
$I_{AVDD1}$		352	513	mA
$I_{AVDD1\_SR}$		23	55	mA
$I_{AVDD2}$		443	478	mA
$I_{AVDD3}$		87	104	mA
$I_{DVDD}$ <sup>1</sup>		146	200	mA
$I_{DRVDD1}$ <sup>2</sup>		183	235	mA
$I_{DRVDD2}$		23	28	mA
$I_{SPIVDD}$		1	1.6	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)		1.75	2.16	W

<sup>1</sup> Full bandwidth mode.

<sup>2</sup> All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.

## SPECIFICATIONS

## DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1\_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference,  $A_{IN} = -1.0$  dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating  $T_A$  range of  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . Typical specifications represent performance at  $T_A = 25^{\circ}\text{C}$ .

Table 5. Digital Specifications

Parameter	Min	Typ	Max	Unit
<b>CLOCK INPUTS (CLK+AND CLK-)</b>				
Logic Compliance		LVDS/LVPECL <sup>1</sup>		
Differential Input Voltage	600	800	1600	mV p-p
Input Common-Mode Voltage		0.69		V
Input Resistance (Differential)		32		k $\Omega$
Input Capacitance			0.9	pF
<b>SYSTEM REFERENCE INPUTS (SYSREF<math>\pm</math>)<sup>2</sup></b>				
Logic Compliance		LVDS/LVPECL <sup>1</sup>		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		k $\Omega$
Input Capacitance (Single-Ended per Pin)		0.7		pF
<b>LOGIC INPUTS (PDWN/STBY)</b>				
Logic Compliance		CMOS <sup>3</sup>		
Logic 1 Voltage	$0.65 \times \text{SPIVDD}$			V
Logic 0 Voltage	0		$0.35 \times \text{SPIVDD}$	V
Input Resistance		10		M $\Omega$
<b>LOGIC INPUTS (SDIO, SCLK, AND CSB)</b>				
Logic Compliance		CMOS <sup>3</sup>		
Logic 1 Voltage	$0.65 \times \text{SPIVDD}$			V
Logic 0 Voltage	0		$0.35 \times \text{SPIVDD}$	V
Input Resistance		56		k $\Omega$
<b>LOGIC OUTPUT (SDIO)</b>				
Logic Compliance		CMOS <sup>3</sup>		
Logic 1 Voltage ( $I_{OH} = 800 \mu\text{A}$ )	$\text{SPIVDD} - 0.45 \text{ V}$			V
Logic 0 Voltage ( $I_{OL} = 50 \mu\text{A}$ )	0		0.45	V
<b>SYNCIN INPUT (SYNCINB<math>\pm</math>AB AND SYNCINB<math>\pm</math>CD)</b>				
Logic Compliance		LVDS/LVPECL/CMOS <sup>1,3</sup>		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		k $\Omega$
Input Capacitance (Single Ended per Pin)		0.7		pF
<b>LOGIC OUTPUTS (FD_A, FD_B, FD_C, AND FD_D)</b>				
Logic Compliance		CMOS <sup>3</sup>		
Logic 1 Voltage	$0.8 \times \text{SPIVDD}$			V
Logic 0 Voltage	0		0.5	V
Input Resistance		56		k $\Omega$
<b>DIGITAL OUTPUTS (SERDOUTAB<math>\pm</math> AND SERDOUTCD<math>\pm</math>, x = 0 OR 1)</b>				
Logic Compliance		CML <sup>4</sup>		
Differential Output Voltage		455.8		mV p-p
Short-Circuit Current ( $I_{D \text{ SHORT}}$ )		15		mA
Differential Termination Impedance		100		$\Omega$



## SPECIFICATIONS

- <sup>1</sup> LVDS is low voltage differential signaling, and LVPECL is low voltage positive emitter-coupled logic.
- <sup>2</sup> DC-coupled input only.
- <sup>3</sup> CMOS is a complementary metal-oxide semiconductor.
- <sup>4</sup> CML is current mode logic.

## SWITCHING SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1\_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and  $A_{IN} = -1.0$  dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating  $T_A$  range of  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . Typical specifications represent performance at  $T_A = 25^{\circ}\text{C}$ .

**Table 6. Switching Specifications**

Parameter	Min	Typ	Max	Unit
<b>CLOCK</b>				
Clock Rate at CLK+ and CLK- Pins	0.3		2.4	GHz
Maximum Sample Rate <sup>1</sup>	600			MSPS
Minimum Sample Rate <sup>2</sup>	240			MSPS
Clock Pulse Width High	125			ps
Clock Pulse Width Low	125			ps
<b>OUTPUT</b>				
Unit Interval (UI) <sup>3</sup>	66.67	100	593	ps
Rise Time ( $t_R$ ), 20% to 80% into 100 $\Omega$ Load		31.25		ps
Fall Time ( $t_F$ ), 20% to 80% into 100 $\Omega$ Load		31.37		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Data Rate per Channel (Nonreturn to Zero (NRZ)) <sup>4</sup>	1.6875	10	15	Gbps
<b>LATENCY<sup>5</sup></b>				
Pipeline Latency		54		Sample clock cycles
Fast Detect Latency			30	Sample clock cycles
<b>WAKE-UP TIME</b>				
From Standby		3		ms
From Power-Down		10		ms
<b>APERTURE</b>				
Aperture Delay ( $t_A$ )		160		ps
Aperture Uncertainty (Jitter, $t_j$ )		44		fs rms
Out of Range Recovery Time		1		Sample clock cycles

- <sup>1</sup> The maximum sample rate is the clock rate after the divider.
- <sup>2</sup> The minimum sample rate operates at 240 MSPS with number of lanes (L) = 2 or L = 1. See SPI Register 0x011A in the AD9694 data sheet to reduce the threshold of the clock detection circuit.
- <sup>3</sup> Baud rate = 1/UI. A subset of this range can be supported.
- <sup>4</sup> Default L = 2 for each link. This number can be changed based on the sample rate and decimation ratio.
- <sup>5</sup> No DDCs used. L = 2, number of converters (M) = 2, and number of octets/frames (F) = 2 for each link.

## TIMING SPECIFICATIONS

**Table 7. Timing Specifications**

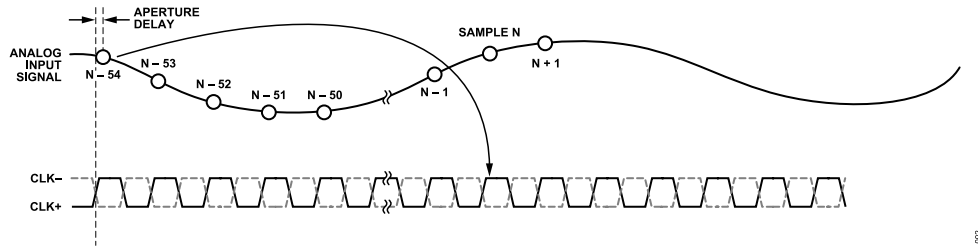
Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>CLK+ to SYSREF+ TIMING REQUIREMENTS</b>					
$t_{SU\_SR}$	See Figure 3 Device clock to SYSREF+ setup time		-44.8		ps
$t_{H\_SR}$	Device clock to SYSREF+ hold time		64.4		ps

**SPECIFICATIONS**

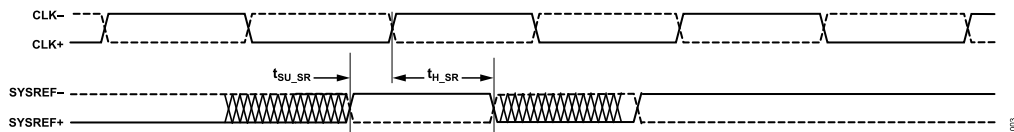
**Table 7. Timing Specifications (Continued)**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>SPI TIMING REQUIREMENTS</b>					
	See <a href="#">Figure 4</a>				
$t_{DS}$	Setup time between the data and the rising edge of SCLK	4			ns
$t_{DH}$	Hold time between the data and the rising edge of SCLK	2			ns
$t_{CLK}$	Period of the SCLK	40			ns
$t_S$	Setup time between CSB and SCLK	2			ns
$t_H$	Hold time between CSB and SCLK	2			ns
$t_{HIGH}$	Minimum period that SCLK must be in a logic high state	10			ns
$t_{LOW}$	Minimum period that SCLK must be in a logic low state	10			ns
$t_{ACCESS}$	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
$t_{DIS\_SDIO}$	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in <a href="#">Figure 4</a> )	10			ns

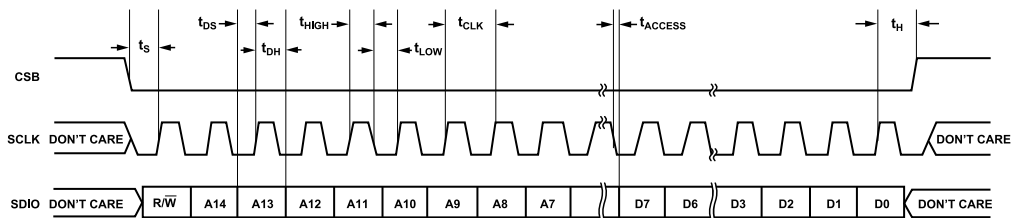
**Timing Diagrams**



**Figure 2. Data Output Timing (Full Bandwidth Mode, L = 4, M = 2, and F = 1)**



**Figure 3. SYSREF± Setup and Hold Timing**



**Figure 4. Serial Port Interface Timing Diagram**

## ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to AGND	2.00 V
VIN±x to AGND	-0.3 V to AVDD3 + 0.3 V
CLK± to AGND	-0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	-0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	-0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND_SR	0 V to 2.5 V
SYNCINB±AB/SYNCINB±CD to DRGND	0 V to 2.5 V
Environmental	
Operating T <sub>A</sub> Range	-55°C to +105°C
Maximum T <sub>J</sub>	125°C
Storage Temperature Range (Ambient)	-65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure,  $\theta_{JC\_BOT}$  is the bottom junction to case thermal resistance,  $\psi_{JT}$  is the junction-to-top thermal characterization, and  $\psi_{JB}$  is the junction-to-board thermal characterization.

Table 9. Thermal Resistance

PCB Type	$\theta_{JA}$	$\theta_{JC\_BOT}$	$\psi_{JT}$	$\psi_{JB}$	Unit
JEDEC					
2s2p Board	20.69 <sup>1</sup>	0.41	0.07	6.75	°C/W

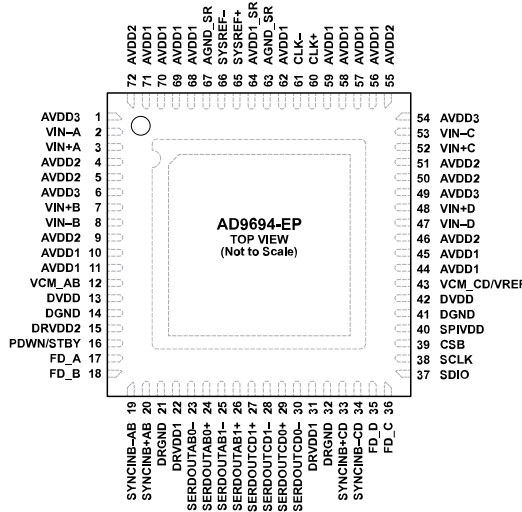
<sup>1</sup> Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
 1. EXPOSED PAD. ANALOG GROUND. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDDx, SPIVDD, DVDD, DRVDD1, AND DRVDD2. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 5. Pin Configuration (Top View)

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	AGND/EPAD	Ground	Exposed Pad. Analog Ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx, SPIVDD, DVDD, DRVDD1, and DRVDD2. This exposed pad must be connected to ground for proper operation.
1, 6, 49, 54	AVDD3	Supply	Analog Power Supply (2.5 V Nominal).
2, 3	VIN-A, VIN+A	Input	ADC A Analog Input Complement/True.
4, 5, 9, 46, 50, 51, 55, 72	AVDD2	Supply	Analog Power Supply (1.8 V Nominal).
7, 8	VIN+B, VIN-B	Input	ADC B Analog Input True/Complement.
10, 11, 44, 45, 56 to 59, 62, 68 to 71	AVDD1	Supply	Analog Power Supply (0.975 V Nominal).
12	VCM_AB	Output	Common-Mode Level Bias Output for Analog Input Channel A and Channel B.
13, 42	DVDD	Supply	Digital Power Supply (0.975 V Nominal).
14, 41	DGND	Ground	Ground Reference for DVDD and SPIVDD.
15	DRVDD2	Supply	Digital Power Supply for JESD204B PLL (1.8 V Nominal).
16	PDWN/STBY	Input	Power-Down Input/Standby (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. This pin requires an external 10 kΩ pull-down resistor.
17, 18, 35, 36	FD_A, FD_B, FD_D, FD_C	Output	Fast Detect Outputs for Channel A, Channel B, Channel C, and Channel D.
19	SYNCINB-AB	Input	Active Low JESD204B LVDS Sync Input Complement for Channel A and Channel B.
20	SYNCINB+AB	Input	Active Low JESD204B LVDS/CMOS Sync Input True for Channel A and Channel B.
21, 32	DRGND	Ground	Ground Reference for DRVDD1 and DRVDD2.
22, 31	DRVDD1	Supply	Digital Power Supply for SERDOUTABx±/SERDOUTCDx± Pins (0.975 V Nominal).
23, 24	SERDOUTAB0-, SERDOUTAB0+	Output	Lane 0 Output Data Complement/True for Channel A and Channel B.
25, 26	SERDOUTAB1-, SERDOUTAB1+	Output	Lane 1 Output Data Complement/True for Channel A and Channel B.
27, 28	SERDOUTCD1+, SERDOUTCD1-	Output	Lane 1 Output Data True/Complement for Channel C and Channel D.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
29, 30	SERDOUTCD0+, SERDOUTCD0-	Output	Lane 0 Output Data True/Complement for Channel C and Channel D.
33	SYNCINB+CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input True for Channel C and Channel D.
34	SYNCINB-CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input Complement for Channel C and Channel D.
37	SDIO	Input/output	SPI Serial Data Input/Output.
38	SCLK	Input	SPI Serial Clock.
39	CSB	Input	SPI Chip Select (Active Low).
40	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V Nominal).
43	VCM_CD/VREF	Output/input	Common-Mode Level Bias Output for Analog Input Channel C and Channel D/0.5 V Reference Voltage Input. This pin is configurable through the SPI as an output or an input. Use this pin as the common-mode level bias output if using the internal reference. This pin requires a 0.5 V reference voltage input if using an external voltage reference source.
47, 48	VIN-D, VIN+D	Input	ADC D Analog Input Complement/True.
52, 53	VIN+C, VIN-C	Input	ADC C Analog Input True/Complement.
60, 61	CLK+, CLK-	Input	Clock Input True/Complement.
63, 67	AGND_SR	Ground	Ground Reference for SYSREF±.
64	AVDD1_SR	Supply	Analog Power Supply for SYSREF± (0.975 V Nominal).
65, 66	SYSREF+, SYSREF-	Input	Active Low JESD204B LVDS System Reference Input True/Complement. DC-coupled input only.

**TYPICAL PERFORMANCE CHARACTERISTICS**

AVDD1 = 0.975 V, AVDD1\_SR = 0.975 V, AVDD2 = 1.80 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and  $A_{IN} = -1.0$  dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating  $T_A$  range of  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . Typical specifications represent performance at  $T_A = 25^{\circ}\text{C}$ . See the [AD9694](#) data sheet for a full set of Typical Performance Characteristics plots.

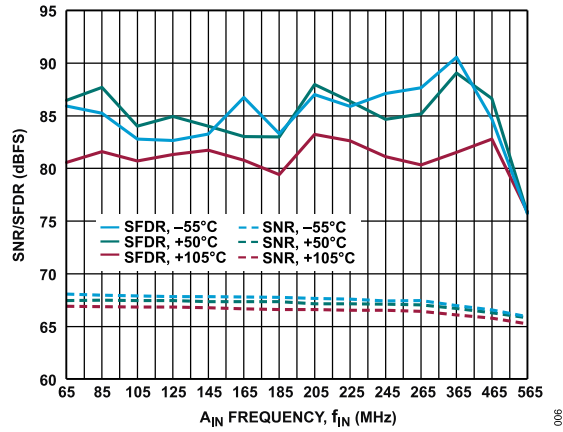


Figure 6. SNR/SFDR vs.  $A_{IN}$  Frequency ( $f_{IN}$ )

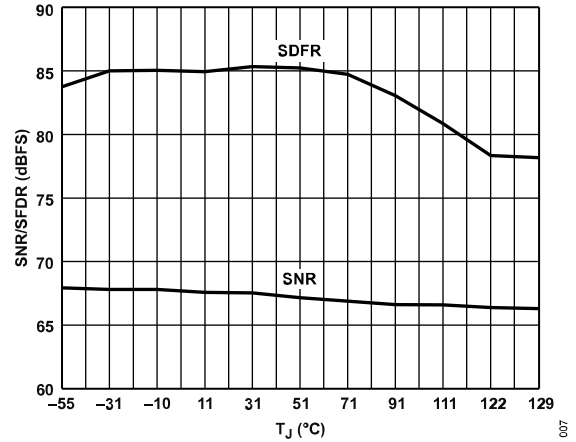
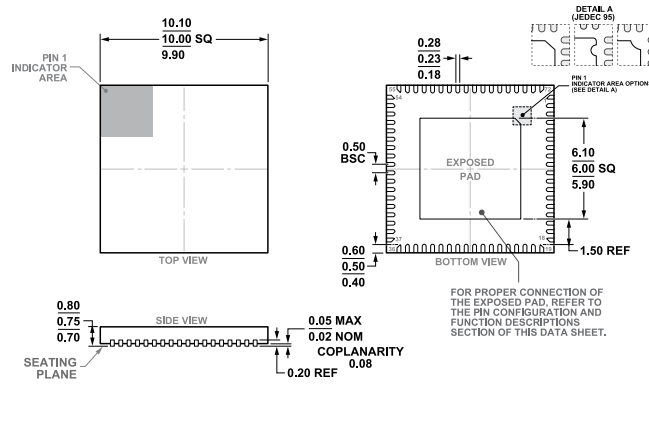


Figure 7. SNR/SFDR vs.  $T_J$ ,  $f_{IN} = 155$  MHz

OUTLINE DIMENSIONS



ORDERING GUIDE

Model <sup>1</sup>	Ambient Temperature Range	Package Description	Package Option
AD9694TCPZ-500-EP	-55°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP]	CP-72-13

<sup>1</sup> Z = RoHS Compliant Part.