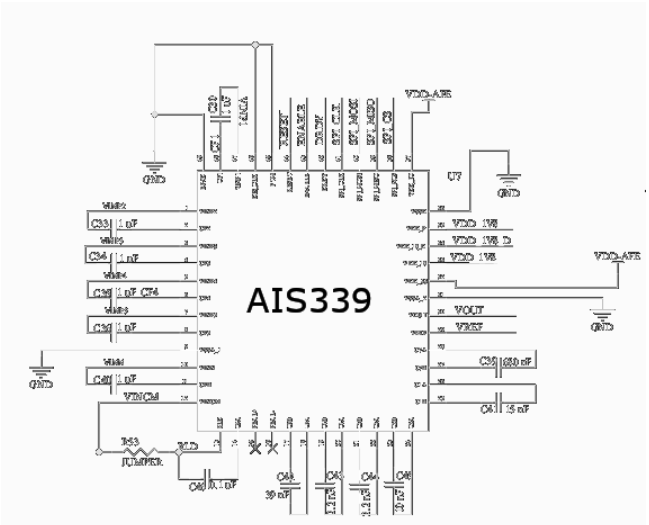
AIS339 Chameleon

Description

The AIS339 Chameleon is an AFE designed to enable signal capture in difficult real world environments. Baseline capture, common mode accelerated recapture, noise rejection, nuisance signal nulling, multi-order analog filtering, and an up to 3rd order almost all pass (Bessel) with mHz bandpass low end corner are example capabilities. To accomplish this the AIS339 includes: i) five input channels and a single reference channel; ii) a programmable gain amplifier (PGA); iii) differential voltage input or transconductor current mode input; iv) a high common mode rejection driver; v) a fast programmable local loop to allow fast caprture & recapture of the common mode; vi) a sample and hold circuit allowing fast recovery from events which move the baseline; viii) an up to 6th order]high order programmable filter response; ix) a buffered differential voltage input between the negative terminals of the instrumentation amplifier to null nuisance signals*; x) analog or ADC outputs; xi) an optional two terminal common mode driver; xii) amplifier offset and shift registers. Between the amplifier and the ADC the AIS339 compares to sigma delta solutions with an ENOB of 18 bits but requires substantially less current. The AIS339 is capable of nyquist rate sampling between multiple different sensors*. Sample & Hold and fast drift recovery circuitry is provided to remember each sensor's common mode and return to it when a channel is selected. Also included is a precision on chip analog reference and charge pump to maximize the input common mode range. The AIS339 will operate with a supply voltage as low as 2.7V up to 3.6V and is available in a 5x5x0.75 48-pin QFN package. *Patents issued or Pending

AIS339 Typical Circuit



System Features

- Offers multiple systems to ease capture of sensor data:
  - Programmable Gain Amplifier (PGA)
  - up to 18 bit ENOB overall accuracy (between Amplifier & ADC)
  - ＞120dB CMRR rejection
  - SPI based time constant loop adjust for fast signal recapture
  - INA tap to allow nulling, lattice wave prediction or DSP in the loop
  - Baseline Sample & Hold for each channel to allow multi-channel nyquist rate sampling
- Allows Closed Loop DSP Around INA
- 6 Input (5xMultiplexer, One Ref Channel)
- Voltage Gain or Transconductor Mode
- Low Noise INA with Digitally Programmed AGC
- SPI Interface
- Charge Pump to expand Input Range
- Precision Analog Reference
- 10-Bit ADC with Separate Enable/Fast Wakeup
- Multi-order Bandpass Filter Response
- 150uV Maximum Offset Voltage
- 5uV inband input referred noise
- 170uA Supply Current
- 48 pin QFN 5x5x0.75

Applications

- Optical PPG (Pulse) or Electrical (ECG) sensing
- ECG, PPG, SPO2, Biometric Extraction
- Heart & Muscle ID
- Real time wavelet processing
- Gas Sensors
- Vibration Monitoring
- Audio Monitoring

Product Description

The primary subsystems are as follows:

- Five Input Differential Multiplexer
  - Full Channel Sample & Hold
- Input Instrumentation Amplifier
  - Programmable Gain (PGA)
  - 5uV Input Referred Noise
  - 150uV Trimmed Input Offset
  - Programmable Common Mode Feedback Loop (102dB CMR)
  - Common Mode Loop Time Constant Acceleration
  - Charge Pump to Maximize Input Range
- On Board Terminator (120dB CMR)
  - Integrated Resistors
  - RLD return without a Third Terminal (Programmable)
- Filters
  - Integrator Loop Around Amplifier Chain (LF Pole)
  - 3rd Order MFB Filter (Component Configured)
  - Programmable Differential to Single Ended Conversion
- 10 bit ADC (up to 12 bit with multiple sampling)
- Overall ENOB=18 bits compared to Digital Solutions
- Analog or Digital Single Ended Output

Multiplexer

The AIS339 accepts up to give input channels (CFx) against a single reference channel (CFB). Connecting a differential input signal to these inputs allows multiple signal paths to be connected to the gain, filter and digitization path of the AIS339 relative to the same common terminal. This can be useful for example in applications like a five lead ECG.

To choose the input channel CFx, write the channel number to be coupled to the first three bits of the Config 1 Register (0x4) as illustrated in Figure 1.

In addition to selecting the multiplexer, the AIS339 contains a number of sample of holds across the entire signal chain corresponding to the desired channel. The purpose of these sample and holds is to hold different nodes throughout the signal chain to their previous values the next time that the channel is selected. This reduces any excusions if one returns to the channel which could otherwise cause glitches or delays in recovery. It also allows nyquist rate sampling such that the AIS339 may be used for multiple channel continuous signal acquisition even though it only offers a single signal path, saving money vs. others solutions. For example, in a five lead ECG the AIS339 can be used to continously acquire ECG data from five leads "simultaneously" not just one channel at a time, replicating a system which otherwise would require five distinct channels and the costs involved therein. As most biometric signals are slow, the multiplexer and sample and hold circuitry can be switched at or above the nyquist rate required to reconstruct the signal from the digital sample.

Figure 2 further illustrates the Sample and Hold system. The multiplexer itself provides a sample and hold capability at the input and other nodes such as the integrator differential loop are separately held. When a previously used channel is selected the previous values are reapplied so that the loop can return to its previous value prior to actuating the multiplexer to the input channel. In this way we do not lose the common mode of each channel and do not have to recapture the operating point.

Offset & Noise

The AIS339 is trimmed to ensure a very low input offset voltage, and designed to minimize input referred noise. Specifically, the AIS339 is trimmed to approximately 150uV of input offset voltage, making it ideal for measuring extremely small signals such as ECG or EEG. Input referred noise will vary with the gain settings of the system, however, typical values are as shown in Table 1.

Symbol	Max	Units
Input Referred Noise 0.01Hz-250Hz		
$0x6_{xxx00000}$	3.91	uV
$0x6_{xxx00001}$	1.65	uV
$0x6_{xxx00100}$	6.69	uV
$0x6_{xxx00110}$	1.34	uV
$0x6_{xxx01000}$	1.02	uV
$0x6_{xxx10000}$	6.54	uV

Table 1. Input Referred Offset at Various Settings

Differential Signal Channel Gain

Figure 3 shows the three gain stages representing the differential path of the AIS339. The AIS339 accepts one of five multiplexer inputs into the CFx pins, with the other differential input being the CFB pin. The first gain stage is an instrumentation amplifier (PGA) with programmable gain. The second gain stage is fixed by the an MFB filter. The final differential to single ended buffer stage with programmable gain. The output of this stage is buffered to an analog output and also presented to the internal analog to digital converter. At maximum gain, the overall equivalent ENOB compared

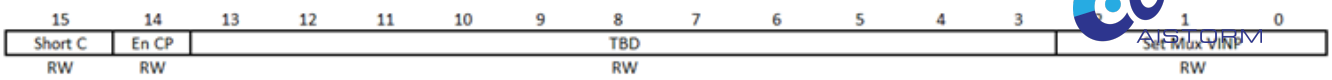


Figure 1. Config 1 Register

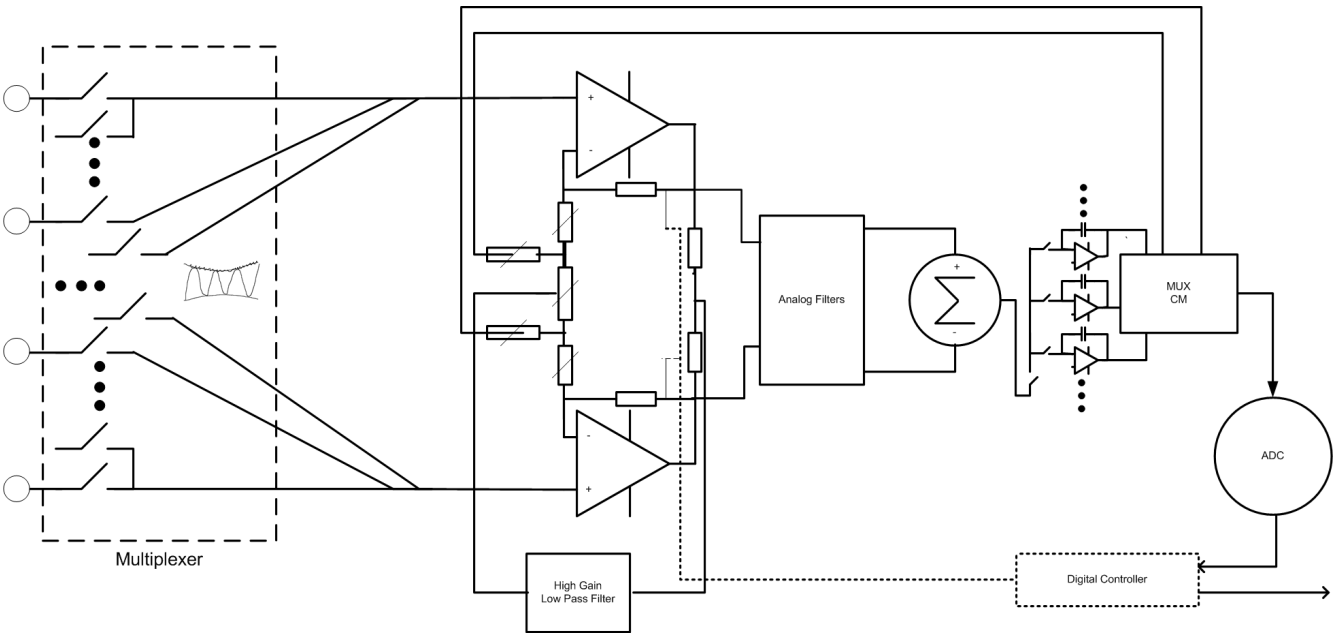


Figure 2. Sample and Hold

to a fully differential converter is 18 bits. In other words it would take 18 bits of accuracy from a completely digital ADC to match the combined gain and ADC of the AIS339. The first stage flat-band gain settings are shown in Table 2

Symbol	Gain	Units
Flat-band Gain of 1st Gain Stage		
$0x6_{xxx00000}$	39.53	dB
$0x6_{xxx00001}$	22.88	dB
$0x6_{xxx00010}$	18.00	dB
$0x6_{xxx00011}$	15.19	dB
$0x6_{xxx00100}$	13.27	dB
$0x6_{xxx00101}$	11.84	dB
$0x6_{xxx00110}$	10.72	dB
$0x6_{xxx00111}$	9.81	dB
$0x6_{xxx01000}$	9.06	dB
$0x6_{xxx01001}$	8.42	dB
$0x6_{xxx01010}$	7.88	dB
$0x6_{xxx01011}$	7.40	dB
$0x6_{xxx01100}$	6.98	dB
$0x6_{xxx01101}$	6.61	dB
$0x6_{xxx01110}$	6.27	dB
$0x6_{xxx01111}$	5.97	dB
$0x6_{xxx1xxxx}$	0.09	dB

Table 2. Flat-band Gain of 1st Gain Stage

The second gain stage, the MFB filter, has a fixed gain which is shown in Table 3. To program the gain set $R4_{MFB}$ to the desired gain according to $\frac{R4_{MFB}}{1870}$ but ensure that filter

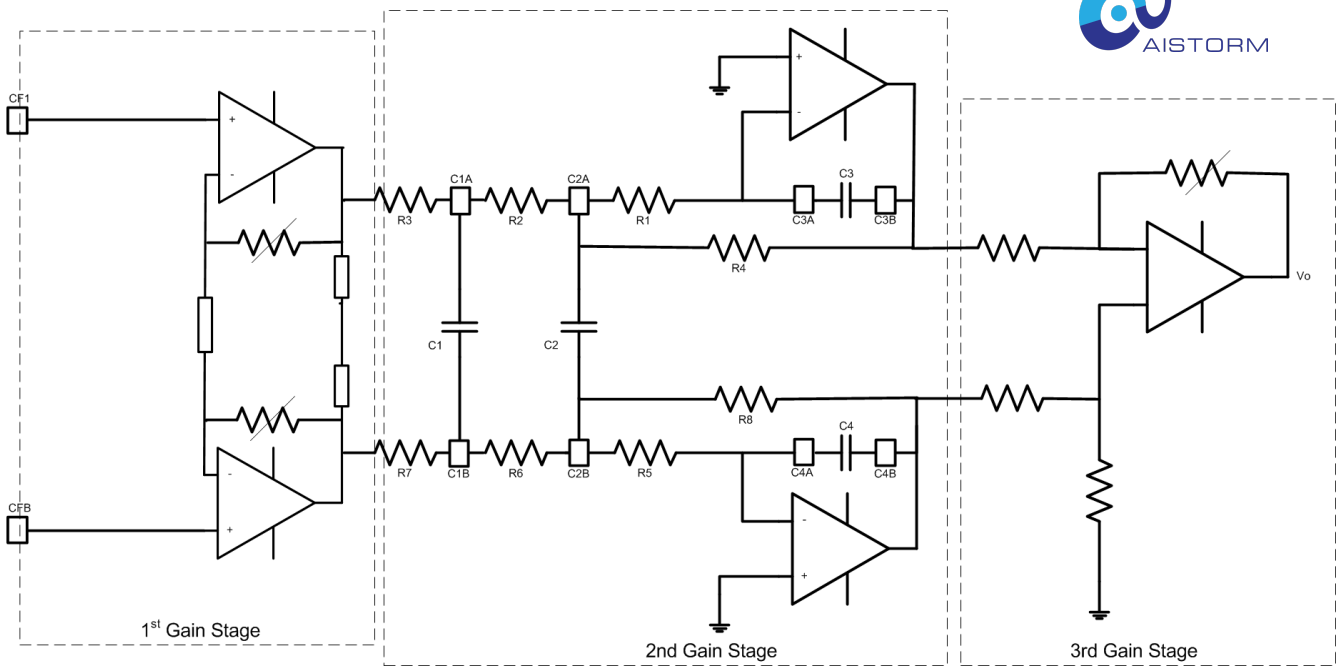


Figure 3. AIS339 Differential Gain Path

coefficients are re-calculated.

Symbol	Gain	Units
Flat-band Gain of 2nd Stage		
$\frac{R4_{MFB}}{1870}$	17.79(-7.75 V/V for R_4=14.5kΩ)	dB

Table 3. Flat-band Gain of 2nd Gain Stage

The third stage of gain, the differential to single ended converter, has can be set per Table 4.

Symbol	Gain	Units
Flat-band Gain of 3rd Stage		
$0x6_{000xxxxx}$	18.06	dB
$0x6_{001xxxxx}$	12.04	dB
$0x6_{010xxxxx}$	6.02	dB
$0x6_{011xxxxx}$	0	dB
$0x6_{100xxxxx}$	-1.94	dB
$0x6_{101xxxxx}$	-6.02	dB
$0x6_{110xxxxx}$	-10.88	dB
$0x6_{111xxxxx}$	-18.06	dB

Table 4. Flat-band Gain of 3rd Gain Stage

The overall DC gain can be calculated by adding the 1st stage, 2nd stage filter and 3rd stage DC gain settings to produce A_{DC}.

Charge Pump

The AIS339 includes a charge pump that may be used to extend the common mode range of the internal amplifiers throughout the entire input operating range, otherwise there will be headroom loss. To enable the CP write a '1' to bit 14 of the Config 1 Register (0x4) shown in Figure 1. In some cases the noise from the charge pump may interfere with extremely sensitive measurements in which case writing a '0' to bit 14 will disable the charge pump.

Startup Sequence

1. Apply an external 3.3V power supply.
2 Wait until Bit 15 of the Status Register (0x10) goes high to indicate boot completed.
2. Set Config 1 Register (0x4) to: i) set Bit 15 to short terminator resistors if terminator is not being used; ii) set Bit 14 to enable the charge pump if it is to be used; iii) set Bits 2-0 to select the appropriate initial multipiexer channel.
3. Set Config 2 Register (0x6) to: i) set Bits 12-9 to set the CM filter feedback resistor.
4. Set Config 3 Register (0x8) to: i) set Bit 15 to '1' to enable transconductor input if used or '0' to enable voltage mode input; ii) set Config 2 or Config 3 register to set appropriate gain settings depending on the selected mode.
5. Set the Sampling Rate Register (0xC) as follows: i) set bits 15-12 to set a clock prescale and; ii) set a count for bits 11-0 to set the actual sampling rate. Note that default sampling rate is 250Hz. The clock rate is 2.5MHz.
6. If Sample and Hold (SAH) is to be used enable the sample and hold system using Config Register 4 (0xA). Set Bit 15 to '1' to enable the SAH and '0' to disable the system. Use Bits

4-0 to force sample of the SAH and Bits 11-7 when we want to load the previously held SAH values.
7. Set pin ENABLE to logic high (depending on VDD_IO voltage) to enable the device.
8. Set Start Register (0x2) to either: i) bit 0 to high to enable continuous sampling at the sample rate or; ii) bit 0 to low to disable continous sample mode and toggle Bit 15 each time a sample is desired.
9. Await interrupt on pin 42 (DREADY) and read value in Result Register (0x10) bits 9-0 for measured ADC value or read output on VOUT pin 30.

Oscillator

To enable the clock raise the DIS_CLK pin high, or to save power connect it low. The clock is trimmed to 2.5MHz, however, it is divided by default by four. This scaling can be changed using the prescale register, which will be 0 by default. Use Bits 15-12 of the Sampling Rate Register (0x47D0) to set the prescaling. Note that the prescaling (Prescale+1)*(Sampling Rate+1) must be greater than 100 (equivalent to 40us), otherwise the system may not operate as the ADC conversion tim eis 13us and the SPI takes 20us (48x400ns). This means we need 33us to ensure operation.

Differential Operation without MFB Filter

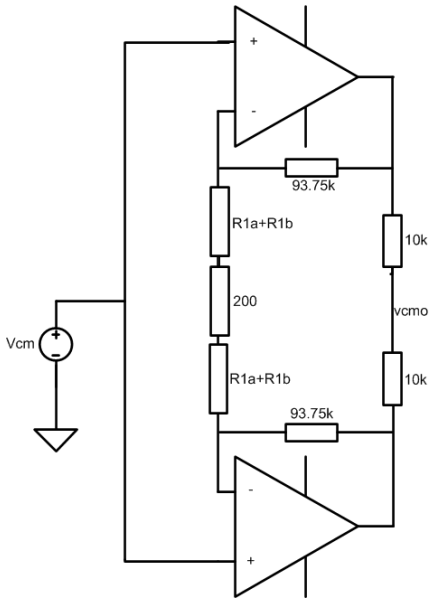


Figure 4. AIS339 INA Gain Stage

Figure 4 shows the details of the instrumentation amplifier. In this case we have written a '1' to Bit 15 of the Config 1 register (0x4) which is further illustrated in Figure 1. The 200ohms in the center is the input tap for the PEAL system and differential filters. These resistors are also held at a specific voltage corresponding to the fast common mode rejection loop.

Resistor R2 is always 93.75k. Resistor R1 is broken up into R1a+R1b+100 ohms such that the total R1 is set according to the table below excluding the 100 ohms.

We can set the resistor values in the differential input amplifier stage using the following table:

R1b				R1a			
R7	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**
76k	51k	26k	1.5k	18.7k	12.5k	6.25k	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0

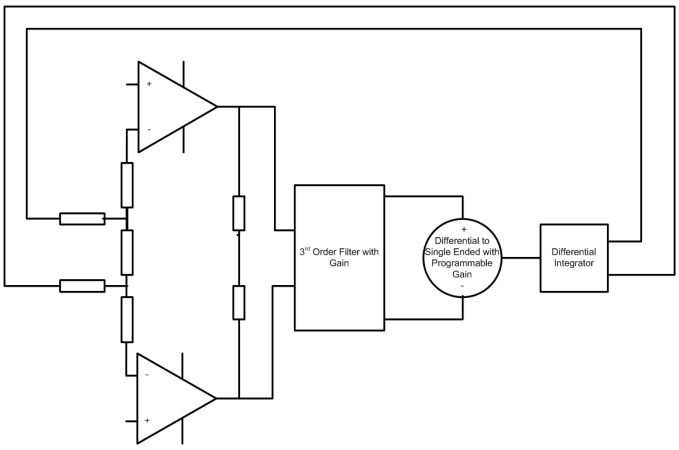


Figure 5. Differential Integrator Loop

Figure 5 shows the conceptual differential gain which includes a differential integrator in the feedback path of the differential amplifier.

We will begin with use of the AIS339 without use of the 3rd order programmable filter. To make use of this configuration do not connect the filter capacitors between C1A and C1B or C2A and C2B. Leave these pins floating, do not GROUND or device will not function!

The differential frequency response transfer function is given in the case without the Bessel filter by:

$$A_D = \frac{V_o(s)}{V_d(s)} \approx \frac{A_{DC} \cdot s}{s + 2 \cdot K_1 \cdot A_{DC}} \qquad (1)$$

Where K_1 is given by:

$$K_1 = 4.492e-6 \cdot \frac{1}{20k \cdot C7} \qquad (2)$$

where C7 is the capacitor connected from C7A to C7B.

The low end high pass filter cutoff frequency created by the integrator loop will be:

$$f_c = \frac{K_1 \cdot A_{DC}}{\pi} \tag{3}$$

For example if we maximize the gain according to the tables for the 1st and 3rd gain stages (36db-1.94db) and add the filter flatband gain of 17.8db) then our total gain is 36db+18db+17.8db=71.8db, and we make C7 a 680nF capacitor then we can expect a corner frequency of about 0.2Hz. The corner frequency can be lowered by either increasing C7 or reducing the gain.

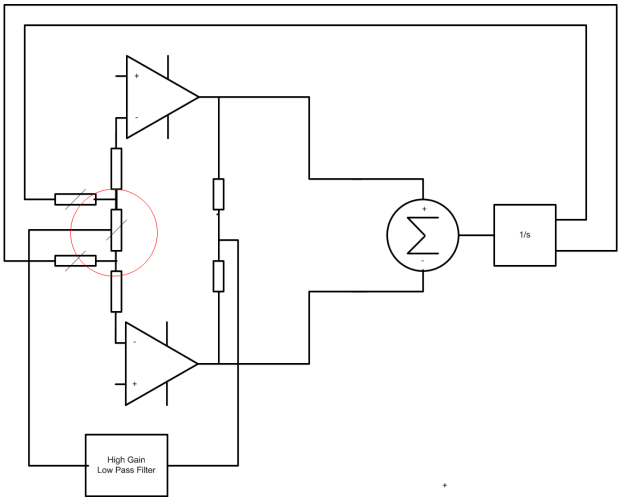


Figure 6. AIS339 Concept

Figure 6 above shows the AIS339 concept without the 3rd order filter or R2 feedback resistors. The input INA's can be seen with each of their outputs tied to a common divider. This divider will extract the common mode from the outputs of the amplifier and remove it from the input through a fast PI loop controlling a special voltage supply which sets the common mode between the two segments of the R1 resistor.

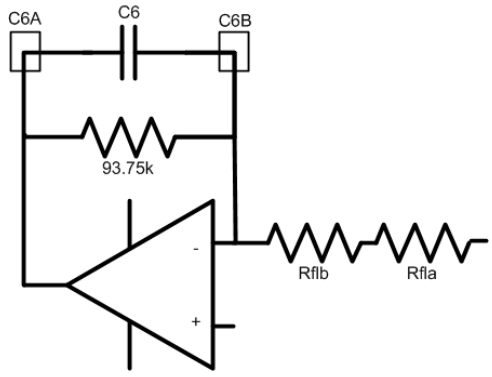


Figure 7. Fast CMRR Loop

Figure 7 shows the equivalent circuit for the fast CMRR rejection amplifier (labelled High Gain Low Pass Filter in Figure 7). The output divider is buffered and fed into Rfla and the output of the amplifier is used to set the midpoint of the 200Ω resistor with a fixed gain constant. The loop is programmable using the Fast Loop Register Bits C0-C7. Bits C0 to C3 set the Rfa resistor and C4 to C7 set the Refb resistor. Capacitor C6 should be connected between the pins C6A to C6B.

By placing this loop into the feedback it will invert in the transfer function (poles become zeros and vice versa), producing a common mode attenuation for higher gain settings (from the center of the 200ohm input PEAL resistors to the divider at the output of the input instrumentation amplifier stage) of:

$$\frac{vcmo}{Vcm} \approx \frac{1}{\frac{93.75k}{Rfla+Rflb} \cdot \frac{1}{1+s \cdot C_6 \cdot 93.75k}} \tag{4}$$

For lower gain settings we need to consider the INA gain resistances R1 and R2.

$$\frac{vcmo}{Vcm} = \frac{R_1 + 2 \cdot R_2}{R1 + 2 \cdot \frac{93.75k}{Rfla+Rflb} \cdot \frac{1}{1+s \cdot C_6 \cdot 93.75k} \cdot R2} \tag{5}$$

The corner frequency is at:

$$f_c = \frac{1}{93.75k * C_6 * 2 * \pi} \tag{6}$$

The combination of Raflb and Rfla can be set according to the following table:

Rflb				**Rfla**			
R7	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**
76k	51k	26k	1.5k	18.7k	12.5k	6.25k	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0

The resulting value for Rfla+Rflb is a combination of the MSB and LSB registers corresponding to Rflb and Rfla. For example a value of 00010001 would result in an overall Rfla+Rflb of 1.5k. A value of 10001000 would result in an overall Rfla+Rflb of 76k+18.7k=94.7k.

It is worth noting that the 200ohm differential resistor used to reject common mode can have its center point moved by a potential related to the voltage supply range as:

$$v_{dcrejectmax} = 2.1e-3 * V_{supply} \quad (7)$$

For example, with a 3.3V supply rail we can subtract off a DC input offset of 6.94mV from the common mode.

Differential Operation without Bessel Filter with RLD

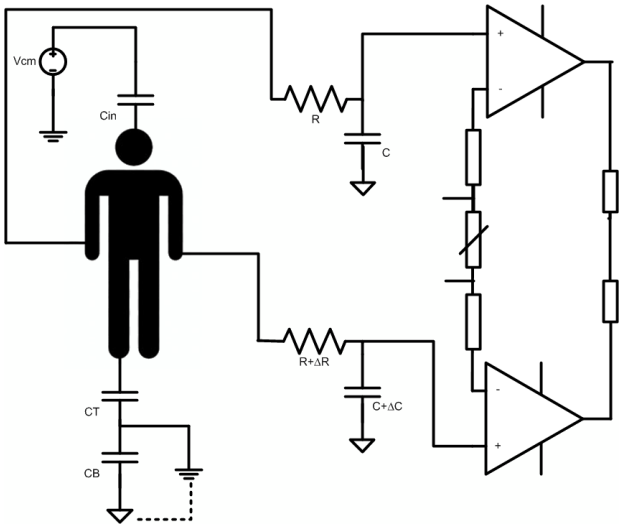


Figure 8. Simple RLD Setup

To understand common mode rejection Figure 8 illustrates the basic divider from the common mode voltage source through a capacitance (such as from building wiring and lighting through the air to the subject). This is the potential that appears on the subjects body for example.

Assuming for a moment that local ground and isolated ground are at the same potential we can find a simple formula for that potential, ignoring for the moment ΔC and ΔR:

$$v_{body} = \frac{\left(\frac{1}{s \cdot C_T}\right) \parallel \left(\frac{1+s \cdot C \cdot R}{2 \cdot s \cdot C}\right)}{\left(\frac{1}{s \cdot C_T}\right) \parallel \left(\frac{1+s \cdot C \cdot R}{2 \cdot s \cdot C}\right) + \frac{1}{s \cdot C_{in}}} \cdot v_{cm} \quad (8)$$

If the components are completely matched the common mode rejection is high, however, if there are mismatches the common mode turns into a differential mode signal and the common mode rejections degrades.

The common mode rejection can be approximated by:

$$CMR = 20 \cdot log\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right) + 20 \cdot log\left(\frac{f}{f_c}\right) \quad (9)$$

If the RC bandwidth is about 6Hz and we have 1% matching components then we only have about 73dB of CMR. In reality there are many components that will combine to create a mismatch of 20% or more and therefore degrade our CMR beyond acceptable levels. We need to find a better way.

A more realistic RLD scheme is shown in Figure 9. Here we have modelled the impedances related to the electrodes and cables, as well as finite input impedances of the input amplifiers. Accurate modelling of the mismatches in these components and ensuring the poles are cancelled by zeros in each of the cable and electrode paths is required to use the RLD to optimize the loop CMR.

3rd Order Differential MFB

The AIS includes a 3rd order MFB (multi-feedback filter). In this section the equations related to this filter are explored and an example set of component values presented. In the second section a special case of a Bessel filter is derived and component values calculated for an example case which may be extended to other types of filters in similar way based upon their characteristic polynomial.

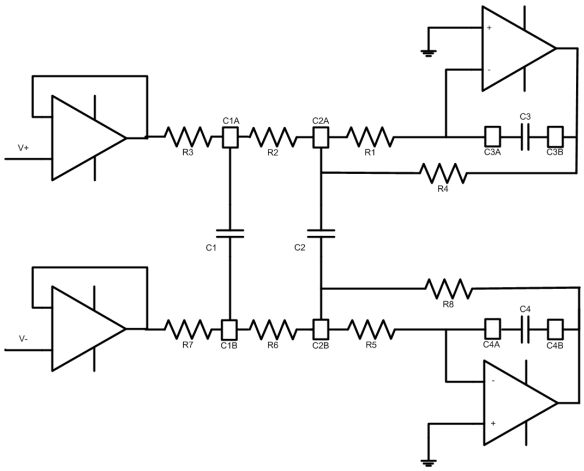


Figure 10. 3rd Order MFB Filter

The AIS339 includes an MFB filter. This filter can be configured by external capacitors C_1, C_2, C_3 and C_4 with integrated resistors internally provided and matched. Specifically, R_3=750, R_2=1.12k, R_3=25k.

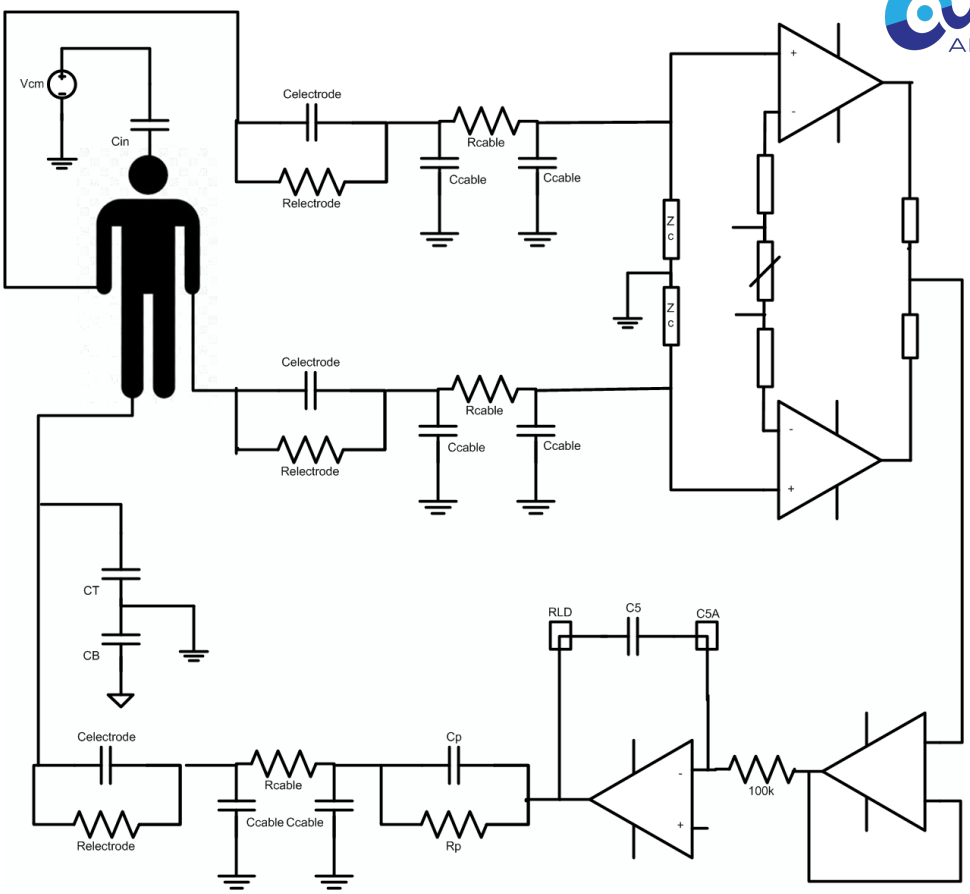


Figure 9. Complex RLD Setup

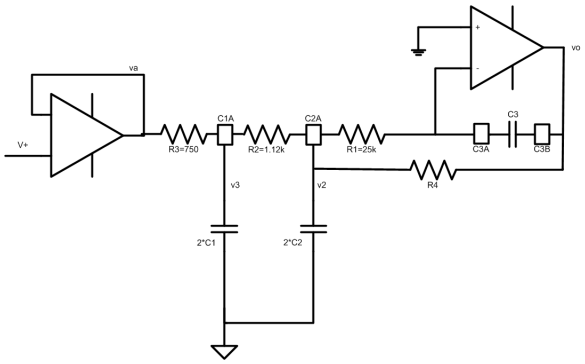


Figure 11. 3rd Order Differential Multi-Feedback (MFB) Filter

To analyze this circuit we look at the half circuit so that we can analyze it relative to ground. The half circuit requires that we double values of C1 and C2 to reach the same transfer function that we would if we analyzed the entire differential circuit.

By nodal analysis:

$$\frac{v_2}{R_1} = -v_o \cdot s \cdot C_1 \tag{10}$$

Therefore,

$$v_2 = -v_o \cdot s \cdot C_1 \cdot R_1 \tag{11}$$

Summing the current at node v_2:

$$\frac{v_3 - v_2}{R_2} = \frac{v_2}{R_1} + \frac{v_2 - v_o}{R_4} + v_2 \cdot s \cdot C_3 \tag{12}$$

Separating the voltages:

$$v_3 = v_2 \cdot \left(1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} + s \cdot C_3 \cdot R_2\right) - v_o \cdot \frac{R_2}{R_4} \tag{13}$$

Substituting v_2 we obtain:

$$v_3 = -v_o \cdot \left[s \cdot C_1 \cdot R_1 \cdot \left(1 + \tfrac{R_2}{R_1} + \tfrac{R_2}{R4}\right) + s^2 \cdot C_1 \cdot C_3 \cdot R_1 \cdot R_2 + \tfrac{R_2}{R_4}\right]$$

(14)

Now summing currents at node v_3:

$$\frac{v_a - v_3}{R_3} = \frac{v_3 - v_2}{R_2} + v_3 \cdot s \cdot C_4] \tag{15}$$

$$v_a = v_3 \cdot (1 + \frac{R_3}{R_2} + s \cdot C_4 \cdot R_3) + v_o \cdot s \cdot C_1 \cdot R_1 \cdot \frac{R_3}{R_2} \tag{16}$$

Solving we find the transfer function:

$$\frac{v_o}{v_s} = -\frac{1}{P \cdot s^3 + Q \cdot s^2 + R \cdot s + S} \tag{17}$$

where the coefficients P, Q, R, S are given by:

$$P = C_1 \cdot C_3 \cdot C_4 \cdot R_1 \cdot R_2 \cdot R_3 \tag{18}$$

$$Q = C_1 \cdot C_3 \cdot R_1 \cdot R_2 \cdot (1 + \frac{R_3}{R_2}) + C_1 \cdot C_4 \cdot R_1 \cdot R_3 \cdot (1 + \frac{R_2}{R_1} + \frac{R_2}{R_4}) \tag{19}$$

$$R = C_1 \cdot R_1 \cdot (1 + \frac{R_2}{R_1} + \frac{R_3}{R_1} + \frac{R_2}{R_4} + \frac{R_3}{R_4}) + C_4 \cdot R_3 \cdot \frac{R_2}{R_4} \tag{20}$$

$$S = \frac{R_2}{R_4} \cdot (1 + \frac{R_3}{R_2}) \tag{21}$$

Dividing through by P, we get:

$$\frac{\frac{1}{C_2 \cdot C_3 \cdot C_4 \cdot R_1 \cdot R_2 \cdot R_3}}{s^3 + K_2 \cdot s^2 + K_1 \cdot s + K_0} \tag{22}$$

Where,

$$K_2 = \frac{1}{C_4 \cdot R_3} \cdot (1 + \frac{R_3}{R_2}) + \frac{1}{C_3 \cdot R_2} \cdot (1 + \frac{R_2}{R_1} + \frac{R_2}{R_4}) \tag{23}$$

$$K_1 = \frac{1}{C_3 \cdot C_4 \cdot R_2 \cdot R_3} \cdot (1 + \frac{R_2}{R_1} + \frac{R_3}{R_1} + \frac{R_2}{R_4} + \frac{R_3}{R_4}) + \frac{1}{C_1 \cdot C_3 \cdot R_1 \cdot R_4}) \tag{24}$$

$$K_0 = \frac{1}{C_1 \cdot C_3 \cdot C_4 \cdot R_1 \cdot R_2 \cdot R_3} \cdot \frac{R_2}{R_4} \cdot (1 + \frac{R_3}{R_2}) \tag{25}$$

This can be simplified to:

$$\frac{v_o}{v_s} = -\frac{R_4}{R_2 + R_3} \cdot \frac{K_0}{s^3 + K_2 \cdot s^2 + K_1 \cdot s + K_0} \tag{26}$$

Therefore the DC gain is:

$$A_0 = -\frac{R_4}{R_2 + R_3} \tag{27}$$

The procedure to follow is:

1. Select a DC gain value, A_0 according to $\frac{R_4}{R_2+R_3}$. With external components such as a resistor across R4 we can reduce but not increase the gain, however, the matching coefficient will be poor due to the difference between on chip and off chip temperature coefficients. 1. Work out the type of filter one wants to use and obtain its characteristic equation coefficients. 2. Use the formulas below for the coefficients to solve the for the components values for an approximatly 1Hz bandwidth. 3. Scale the capacitor values to adjust the filter bandwidth to the desired 3db frequency or unity gain frequency. 4. Identify the capacitors common to the two halves of the differential circuit and halve the value of these components when used in the differential configuration. 5. Use a numerical solver, such as http://sim.okawa-denshi.jp/en/Multiple3tool.php. Enter the component values and confirm the filter response is as expected. Iterate the corner or unity gain frequency with this tool by scaling the capacitor values.

Utilizing the above procedure capacitor values of C_1=15nF, C_2=10nF, and C_3=C_4=2.2nF are obtained. To utilize these values in teh Okawa tool above we need to double the value of C_1 and C_2 and ensure that we are substituting components into the simulator according to Okawa's setup diagram and

not our own convention. Doing this we obtain the following bode plot:

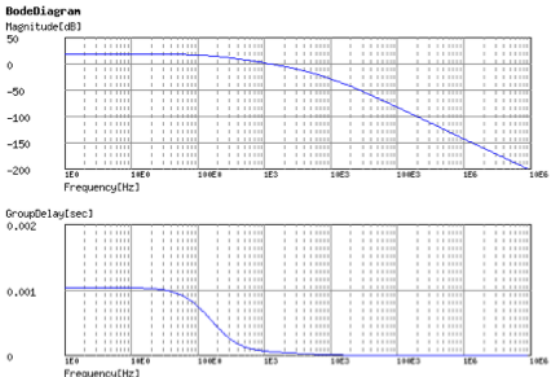


Figure 12. Bode Plot for C_1=15nF, C_2=10nF, and C_3=C_4=2.2nF

The 3db is at 161Hz and the gain is -7.75 (17.79db). The unity gain frequency is 1176Hz.

Bessel Filter

Most heart rate waveform extraction systems prefer a Bessel or all pass response. Figure 13 illustrates the difference between a Bessel filter and other types of filters.

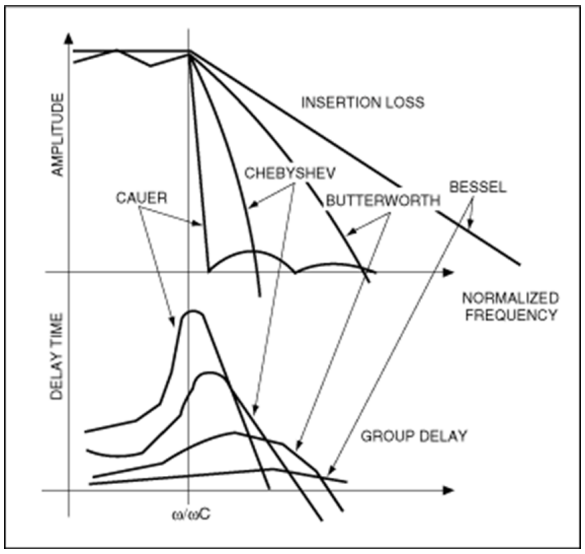


Figure 13. Comparison Between Filter Types

In general, it has been shown that a Bessel response will be achieved if the polynomical coefficient are calculated as follows:

$$c_i = \frac{(2\cdot n - i)!}{2^{n-1}\cdot i!\cdot (n-i)!} \tag{28}$$

For a 3rd order system of the form $c_3 s^3 + c_2 s^2 + c_1 s + c_0$ this means that:

c_0=15
c_1=15
c_2=6
c_3=1

We know that R3=750Ω, R3=1.12kΩ and R3=25kΩ.

$$6 = \frac{1}{C_4\cdot R_3}\cdot(1+\frac{R_3}{R_2})+\frac{1}{C_3\cdot R_2}\cdot(1+\frac{R_2}{R_1}+\frac{R_2}{R_4}) \tag{29}$$

$$15 = \frac{1}{C_3\cdot C_4\cdot R_2\cdot R_3}\cdot(1+\frac{R_2}{R_1}+\frac{R_3}{R_1}+\frac{R_2}{R_4}+\frac{R_3}{R_4})+\frac{1}{C_1\cdot C_3\cdot R_1\cdot R_4} \tag{30}$$

$$15 = \frac{1}{C_1\cdot C_3\cdot C_4\cdot R_1\cdot R_2\cdot R_3}\cdot\frac{R_2}{R_4}\cdot(1+\frac{R_3}{R_2}) \tag{31}$$

We know that the values of the built in resistors on the IC are R_4=14.5k, R_3=750, R_2=1.12k, R_1=25k. This means that the DC gain, A_0=$\frac{R_4}{R_2+R_3}$ = $\frac{14.5k}{1870}$ = $7.75 or 17.79 dB$.

Substituting resistor values:

$$6 = \frac{1}{C_4\cdot 750}\cdot(1+\frac{750}{1120})+\frac{1}{C_3\cdot 1120}\cdot(1+\frac{1120}{25000}+\frac{1120}{14500}) \tag{32}$$

which simplifies to:

$$6 = \frac{2.226e-3}{C_4}+\frac{1.002e-3}{C_3} \tag{33}$$

$$15 = \frac{1}{C_3\cdot C_4\cdot 1120\cdot 750}\cdot(1+\frac{1120}{25e3}+\frac{750}{25k}+\frac{1120}{14500}+\frac{750}{14500})+\frac{1}{C_1\cdot C_3\cdot 25k\cdot 145} \tag{34}$$

which simplifies to:

$$15 = \frac{1.433e-6}{C_3\cdot C_4}+\frac{2.759e-9}{C_1\cdot C_3} \tag{35}$$

$$15 = \frac{1}{C_1\cdot C_3\cdot C_4\cdot 750\cdot 1120\cdot 25000}\cdot\frac{1120}{1}4500\cdot(1+\frac{750}{1120}) \tag{36}$$

This simplifies to:

$$15 = \frac{6.1412e-12}{C_1\cdot C_3\cdot C_4} \tag{37}$$

Solving for C1 we get:

$$C_1 = \frac{4.094e-13}{C_3 \cdot C_4} \tag{38}$$

Substituting C_1 into 37 we get:

$$C_3 = \frac{1.433e-6}{(15-6739 \cdot C_4) \cdot C_4} \tag{39}$$

Note that the coefficients we used correspond to a maximally flat response, unfortunately Bessel systems do not have a simple formula to relate pole values to bandwidth.

The poles of a 3rd order Bessel system as given by the coefficients Equation 28 are:

r1 = -2.322 rad/s r2 = -1.8389 - j1.7544 rad/s r3 = -1.8389 + j1.7544 rad/s

Bessel poles lie on a family of ellipses becoming larger with increasing order, but all with their near focus at the complex plane origin and the other focus on the positive part of the real axis. We need to divide the roots r1,2,3 by a w_3n or 3db frequency to normalize to 1Hz bandwidth. For our application we then need to scale the bandwidth to our desired w3h (our 3db frequency) as desired, ie:

$$s1,2,3 = r1,2,3 \cdot \frac{w_H}{w_3N} \tag{40}$$

The easiest procedure to do this is to calculate our approximately 1Hz bandwidth and then iterate the pole locations by scaling per equation 40.

For example we choose C_4=1mF. This results in a C_3=0.173mF and C_1=2.366μF. Now we multiply by 0.5e-3 to scale the capacitors as follows: C_4=0.5μF, C_3=0.0685μF and C_1=1.183nF.

The w_H was set at $2\pi \cdot 513Hz$ to create an approximately flat all pass response up to $2\pi \cdot 250Hz$. The easiest way to iterate the w_H is to use the tool at http://sim.okawa-denshi.jp/en/Multiple3tool.php. Be sure to be mixed up by the labelling conventions used on this web site vs. those used in the analsis as they are not the same.

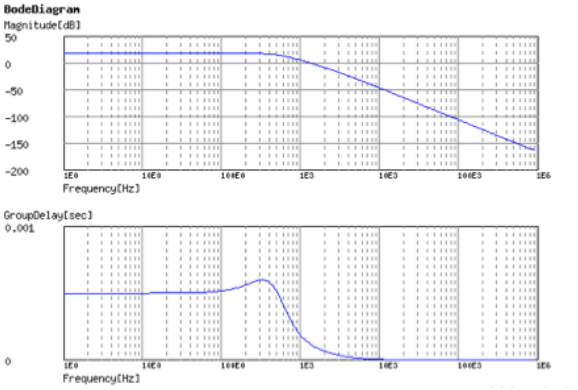


Figure 14. Bessel Response

Now that we have worked out the half circuit capacitor values we need to remember to half the values again for the differential case. Note that only C_3 and C_4 are connected between the two half circuits and therefore these are the only components whose values have to double.

Finally, we have the following values for the capacitors:

C_4=0.25nF (halved)
C_3=34nF (halved)
C_1=C_2=1.183nF (not halved)

The 3db frequency is 513Hz and the gain is -7.75 (17.79db). The unity gain frequency is 1327Hz. We then find that:

Transconductor Mode

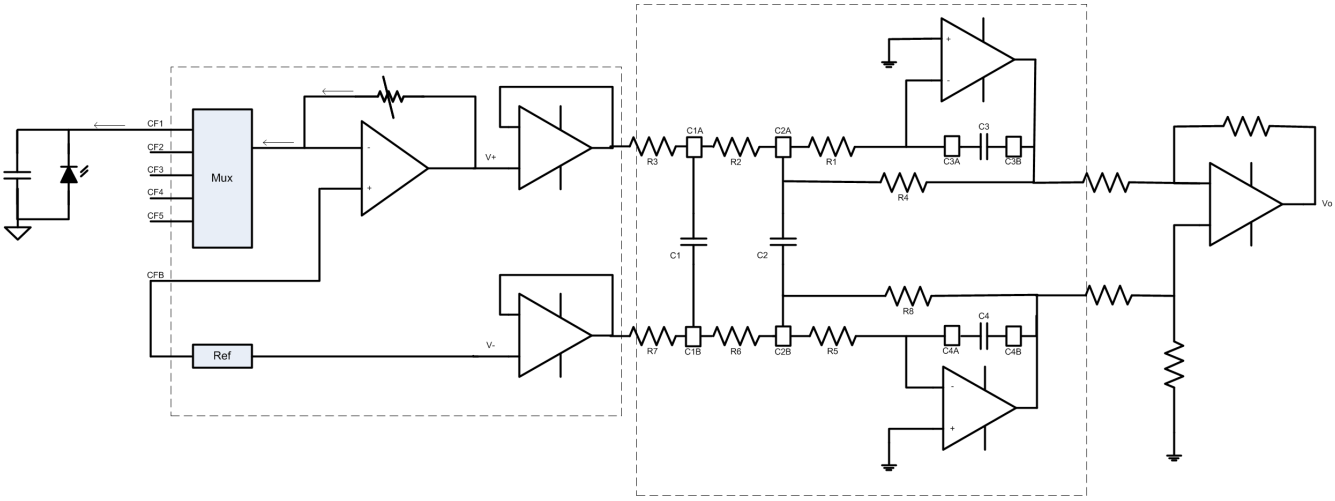


Figure 15. Transconductor Mode

Figure 15 above illustrates the AIS339 reconfigured into Transconductor Mode. In this mode the CFx pins may be connected to up to five different photodiodes while retaining the capture, filter and digitization abilities of the AIS339. The transconductor includes a variable resistor which can be used to control the current gain. The on board precision reference is buffered to VINN which is used as the connection point for the photodiodes and the transconductor inputs. The on board precision reference also represents one of the inputs to the 3rd order MFB filter. This filter is then coupled to a differential to single ended output stage and finally can be buffered to an analog output or can be digitized and read through the SPI registers.

Symbol	Gain	Units
Transconductor Resistor		
SET_TRANS_LOW_RANGE		
$0x8_{1010000000000001}$	1000	Ω
$0x8_{1010000000000010}$	2000	Ω
$0x8_{1010000000000100}$	4000	Ω
$0x8_{1010000000001000}$	8000	Ω
$0x8_{1010000000010000}$	16000	Ω
$0x8_{1010000000100000}$	32000	Ω
$0x8_{1010000001000000}$	64000	Ω
SET_TRANS_HIGH_RANGE		
$0x8_{1010000001000000}$	40000	Ω
$0x8_{1010000010000000}$	80000	Ω
$0x8_{1010000100000000}$	160000	Ω
$0x8_{1010001000000000}$	320000	Ω
$0x8_{1010010000000000}$	640000	Ω
$0x8_{1010100000000000}$	1280000	Ω
$0x8_{1011000000000000}$	2560000	Ω

Table 5. Flat-band Gain of 1st Gain Stage

To reduce the number of external components, high valued resistors are included on chip and may be programmed using register 0x8 according to the settings in Table 5.

Pinout

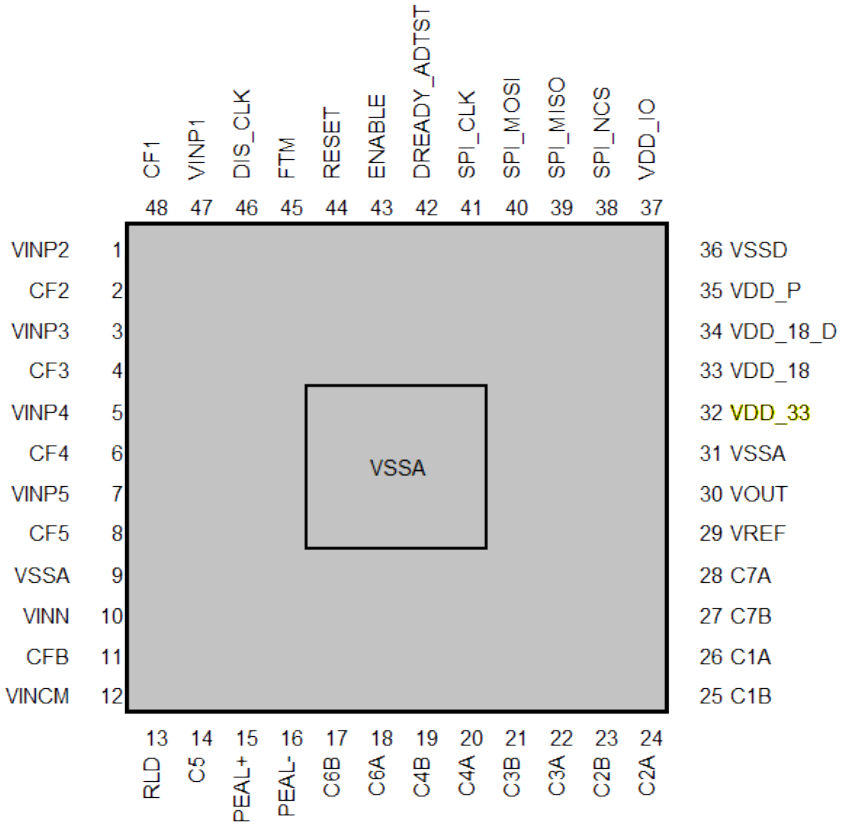


Figure 16. Pinout

Package Type	# Of Leads	Nominal Package Size	Package Outline Drawing Code	Pocket Tape		Pin 1 Orientation	Reel Size (mm)	Reel Size (inch)	Qty Per Reel
				Width	Pitch(P1)				
QFN	48	5x5x0.75mm	J1-10048-006	12mm	8mm	Top-Left	330mm	13"	TBD

Figure 17. Tape and Reel Details

Pin	Name	Voltage	Description
1	VINP2	3.3V	Positive input signal 2
2	CF2	3.3V	Capacitor to VINP2 - 1uF
3	VINP3	3.3V	Positive input signal 3
4	CF3	3.3V	Capacitor to VINP3 - 1uF
5	VINP4	3.3V	Positive input signal 4
6	CF4	3.3V	Capacitor to VINP4 - 1uF
7	VINP5	3.3V	Positive input signal 5
8	CF5	3.3V	Capacitor to VINP5 - 1uF
9	VSSA	0V	IC analog ground
10	VINN	3.3V	Negative input signal
11	CFB	3.3V	Capacitor to VINN - 1uF

Continued on next page

Table 6 – continued from previous page

Pin	Name	Voltage	Description
12	VINCM	3.3V	Common mode input
13	RLD	3.3V	Right Leg Drive, Common mode force, connected to VINCM
14	C5A	3.3V	Filter capacitor to VINCM - 100nF
15	PEAL+	3.3V	PEAL+ input
16	PEAL-	3.3V	PEAL- input
17	C6B	3.3V	Filter capacitor to C6A - 39nF
18	C6A	3.3V	Filter capacitor to C6B - 39nF
19	C4B	3.3V	Filter capacitor to C4A - 2.2nF
20	C4A	3.3V	Filter capacitor to C4B - 2.2nF
21	C3B	3.3V	Filter capacitor to C3A - 2.2nF
22	C3A	3.3V	Filter capacitor to C3B - 2.2nF
23	C2B	3.3V	Filter capacitor to C2A - 10nF
24	C2A	3.3V	Filter capacitor to C2B - 10nF
25	C1B	3.3V	Filter capacitor to C1A - 15nF
26	C1A	3.3V	Filter capacitor to C1B - 15nF
27	C7B	3.3V	Filter capacitor to C7A - 680nF
28	C7A	3.3V	Filter capacitor to C7B - 680nF
29	VREF	1.8V	Reference voltage output (programmable or to force externally)
30	VOUT	3.3V	INA output voltage
31	VSSA	0V	IC analog ground
32	VDD_33	3.3V	3.3V Input supply
33	VDD_18	1.8V	1.8V Regulator output for external capacitor (2.2uF)
34	VDD_18_D	1.8V	Digital part voltage suplly input
35	VDD_P	7.1V	OTP Programming voltage, 1.8V normal, 7.1V burning
36	VSSD	0V	IC digital ground
37	VDD_IO	1.8V-3.3V	IO voltage supply input
38	SPI_NCS	VDD_IO	SPI Chip select not
39	SPI_MISO	VDD_IO	SPI Miso
40	SPI_MOSI	VDD_IO	SPI Mosi
41	SPI_CLK	VDD_IO	SPI Clock
42	DREADY_ADTST	3.3V	Data ready output showing valid ADC data conversion, used in FTM for test signals
43	ENABLE	3.3V	Enable device (1.8V-3.3V logical high)
44	RESET	VDD_IO	Device reset
45	FTM	3.3V	Enable Factory Test Mode (1.8V-3.3V logical high)
46	DIS_CLK	VDD_IO	Disable internal Oscillator
47	VINP1	3.3V	Positive input signal 1
48	CF1	3.3V	Capacitor to VINP1 - 1uF

Table 6. Pinout