MP28254

High Efficiency 4A, 21V, 500kHz Synchronous Step down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP28254 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 4A continuous output current over a wide input supply range with excellent load and line regulation. The MP28254 has synchronous mode operation for higher efficiency over output current load range.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include OCP and thermal shut down.

The MP28254 requires a minimum number of readily available standard external components and is available in a space saving 3mm x 4mm 14-pin QFN package.

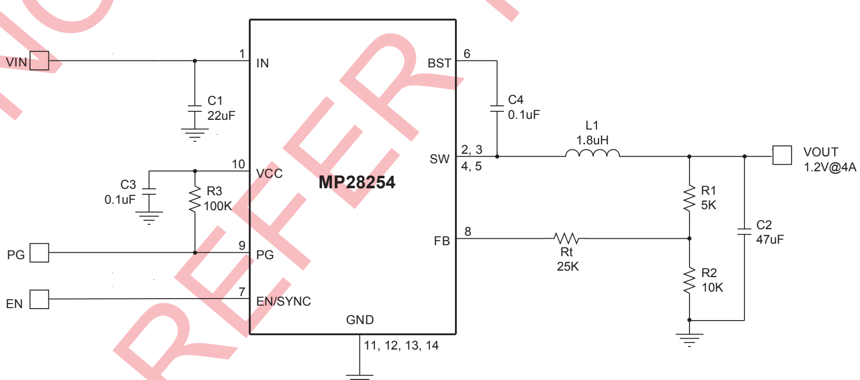
FEATURES

- Wide 4.5V to 21V Operating Input Range
- 4A Output Current
- Low Rds(on) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- High Efficiency Synchronous Mode Operation
- Fixed 500kHz Switching Frequency
- Sync from 300kHz to 2MHz External Clock
- Internal Compensation
- Integrated Bootstrap Diode
- OCP Protection and Thermal Shutdown
- Output Adjustable from 0.805V
- Available in a 3mm x 4mm 14-Pin QFN Package

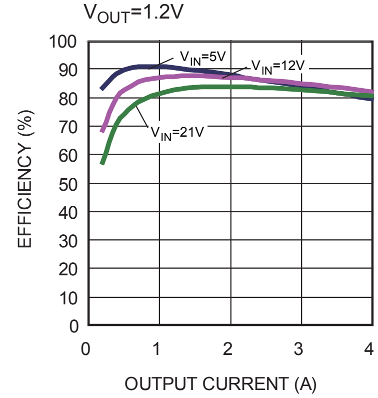
APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Digital Set Top Boxes
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



Efficiency
V_{OUT}=1.2V

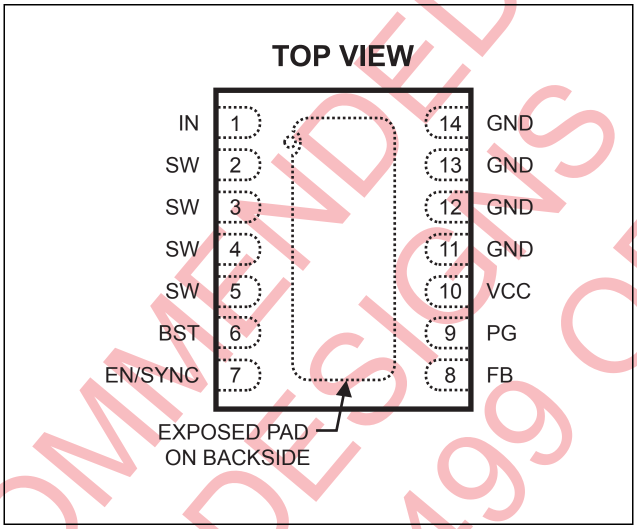


ORDERING INFORMATION

Part Number	Package	Top Marking
MP28254EL	3x4 QFN14	MP28254EL

For Tape & Reel, add suffix –Z (e.g. MP28254EL–Z);
For RoHS compliant packaging, add suffix –LF; (eg. MP28254EL–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 22V
V_{SW} ....-0.3V (-5V for < 10ns) to 23V
V_{BS} .... V_{SW} + 6V
All Other Pins...............................-0.3V to +6V
Operating Temperature..............-20°C to +85°C
Continuous Power Dissipation (T_A = +25°C) (2)
....2.6W
Junction Temperature.............................150°C
Lead Temperature ....260°C
Storage Temperature...............-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .... 4.5V to 21V
Operating Junct. Temp (T_J)......-20°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
3x4 QFN14	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			10	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.7		mA
HS Switch On Resistance	HS_{RDS-ON}			120		mΩ
LS Switch On Resistance	LS_{RDS-ON}			20		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	10	μA
Current Limit (5)	I_{LIMIT}		5			A
Oscillator Frequency	F_{SW}	V_{FB} = 0.75V	425	500	575	kHz
Fold-back Frequency	F_{FB}	V_{FB} = 300mV		0.25		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB} = 700mV	85	90		%
Minimum On Time (5)	t_{ON}			100		ns
Sync Frequency Range	F_{SYNC}		0.3		2	MHz
Feedback Voltage	V_{FB}		789	805	821	mV
Feedback Current	I_{FB}	V_{FB} = 800mV		10	50	nA
EN Rising Threshold	V_{EN_RISING}		1	1.3	1.6	V
EN Threshold Hysteresis	V_{EN_HYS}			0.4		V
EN Input Current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
EN Turn Off Delay	EN_{Td-Off}			5		μs
Power Good High Threshold	VTH_{PG}			0.9		V_{FB}
Power Good Low Threshold	VTL_{PG}			0.85		V_{FB}
Power Good Delay	PG_{Td}			20		μs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V			10	nA
V_{IN} Under Voltage Lockout Threshold Rising	$INUV_{VTH}$		3.8	4.0	4.2	V
V_{IN} Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			880		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		Icc=2mA		5		%
Soft-Start Period			2	4	6.5	ms
Thermal Shutdown	T_{SD}			150		°C

Note:
5) Guaranteed by design.

PIN FUNCTIONS

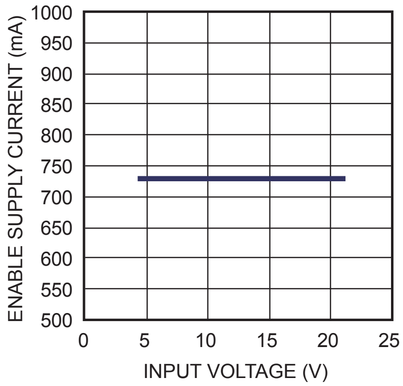
Pin #	Name	Description
1	IN	Supply Voltage. The MP28254 operates from a +4.5V to +21V input rail. C1 is needed to decouple the input rail. Use wide PCB trace to make the connection.
2,3,4,5	SW	Switch Output. Use wide PCB trace to make the connection.
6	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
7	EN/SYNC	EN=1 to enable the chip. External clock can be applied to EN pin for changing switching frequency. For automatic start-up, connect EN pin to VIN by proper EN resistor divider as Figure 2 shows.
8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 500mV.
9	PG	Power Good Output. The output of this pin is low if the output voltage is 15% less than the normal value; otherwise it is an open drain.
10	VCC	Bias Supply. Decouple with 0.1μF~0.22μF cap. And the capacitance should be no more than 0.22μF
11,12,13,14	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout. Suggested to be connected to GND with copper and vias.
	Exposed Pad	Exposed pad has no internal electrical connection, and make sure exposed pad is connected to GND through a large copper area in PCB layout.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1.8µH, T_A = +25ºC, unless otherwise noted.

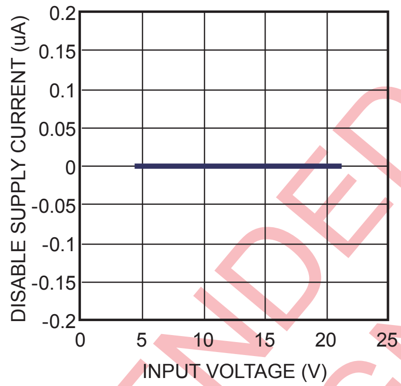
ENABLED SUPPLY CURRENT vs. INPUT VOLTAGE

V_{FB}=1V

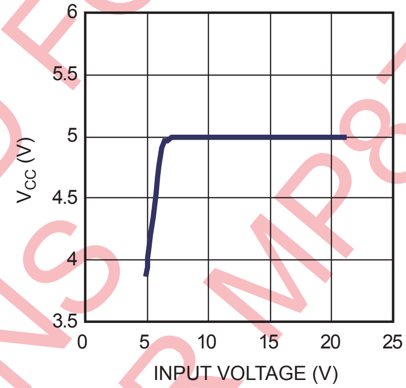


DISABLED SUPPLY CURRENT vs. INPUT VOLTAGE

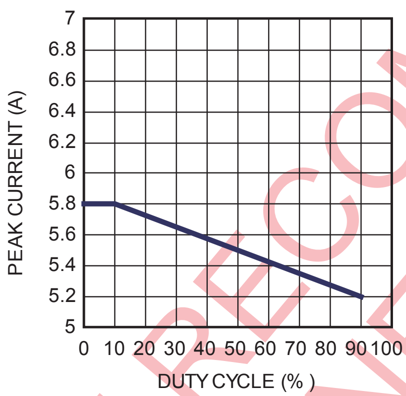
V_{EN}=0V



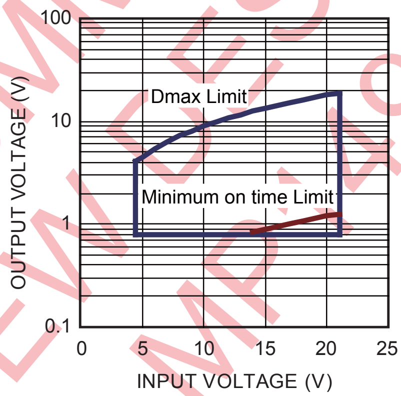
VCC Regulator Line Regulation



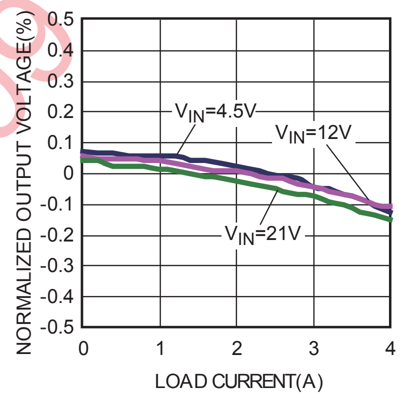
Peak Current vs. Duty Cycle



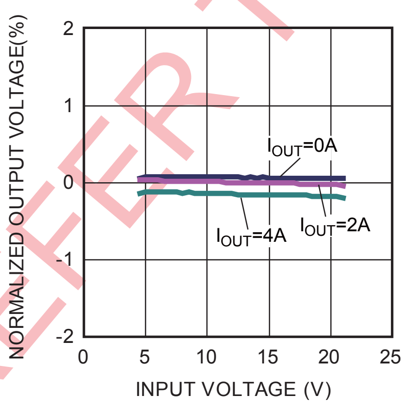
Operating Range



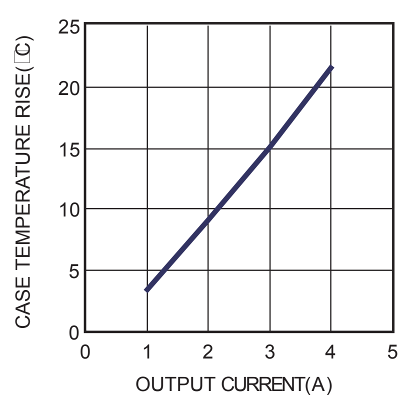
Load Regulation



Line Regulation



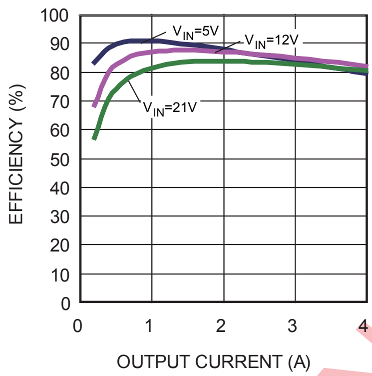
Case Temperature vs. Output Current



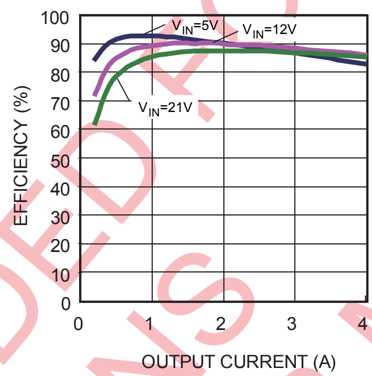
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1.8µH, T_A = +25ºC, unless otherwise noted.

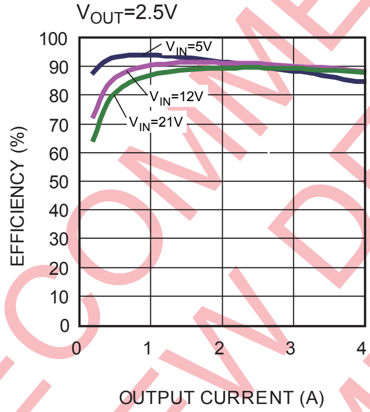
Efficiency
V_{OUT}=1.2V



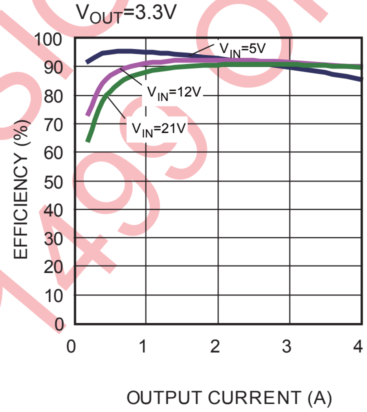
Efficiency
V_{OUT}=1.8V



Efficiency
V_{OUT}=2.5V



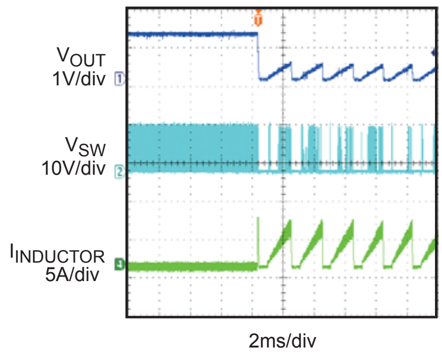
Efficiency
V_{OUT}=3.3V



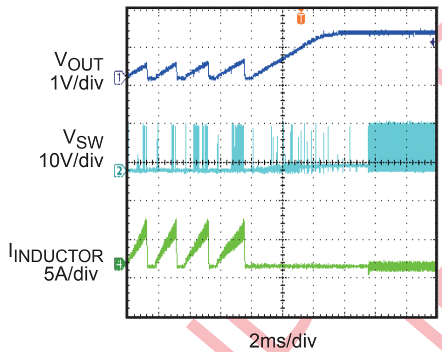
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1.8µH, T_A = +25ºC, unless otherwise noted.

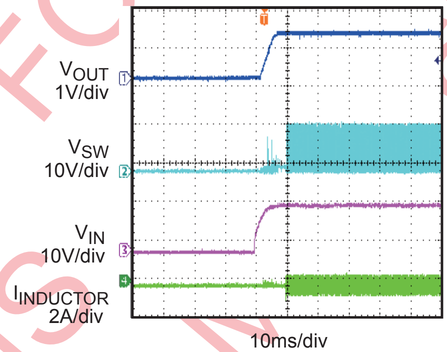
Short Entry



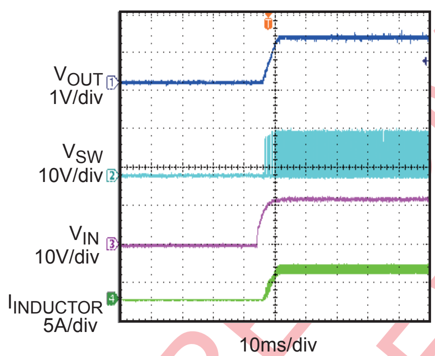
Short Recovery



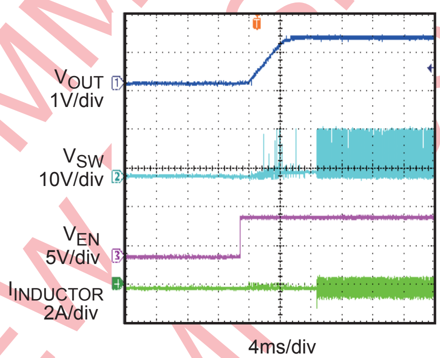
Power up without Load



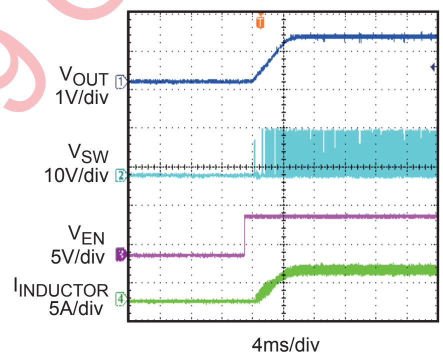
Power up with 4A Load



Enable Startup without Load

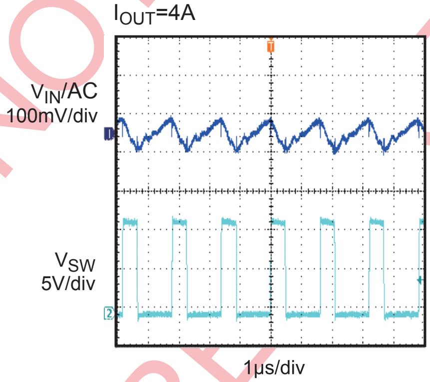


Enable Startup with 4A Load



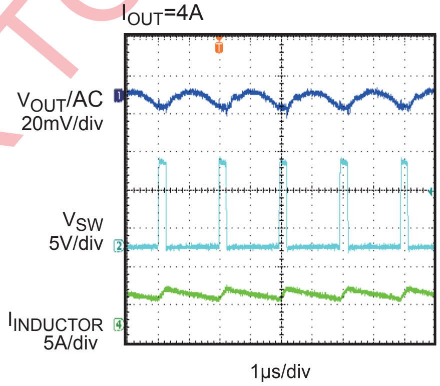
Input Ripple Voltage

I_{OUT}=4A



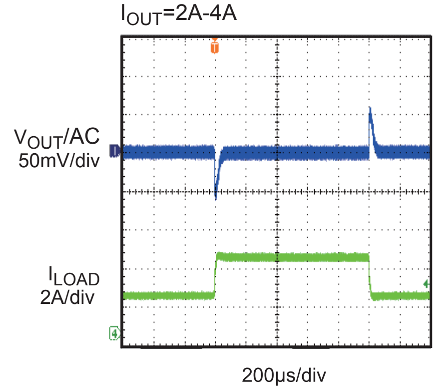
Output Ripple Voltage

I_{OUT}=4A



Load Transient Response

I_{OUT}=2A-4A



BLOCK DIAGRAM

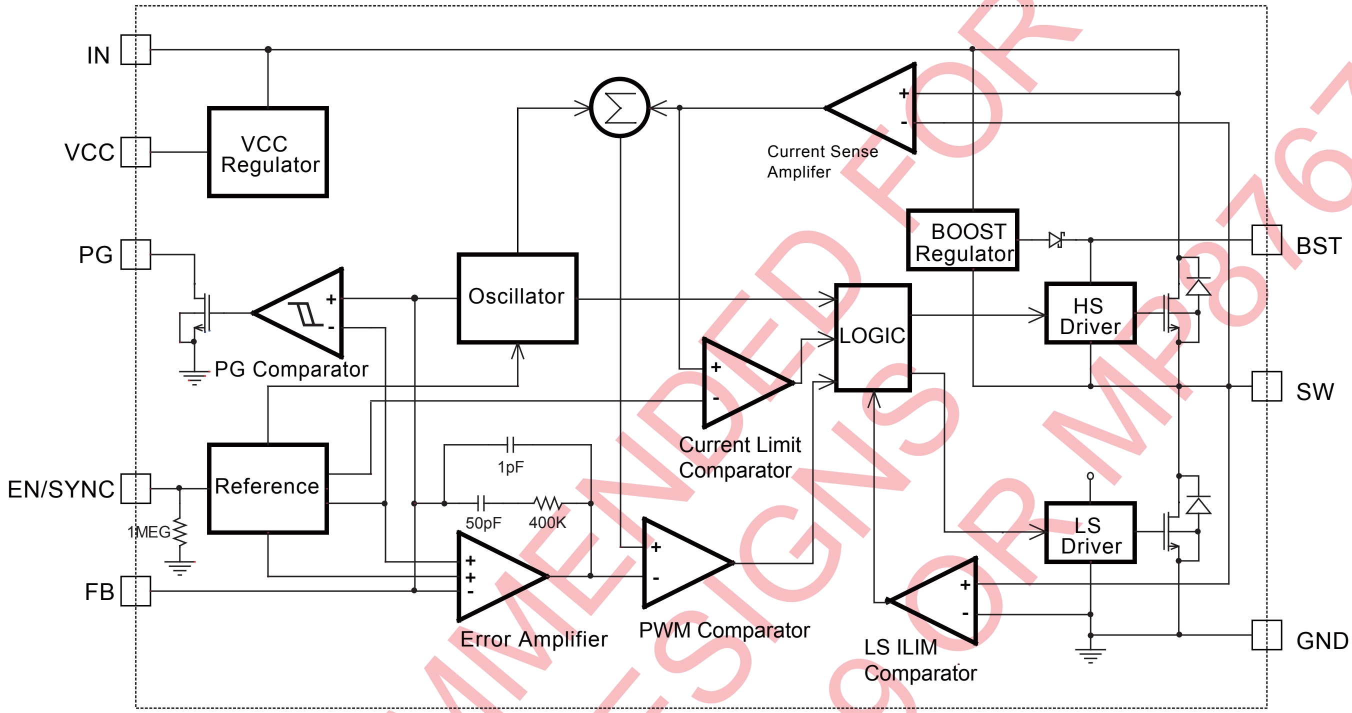


Figure 1—Function Block Diagram

OPERATION

The MP28254 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 4A continuous output current over a wide input supply range with excellent load and line regulation.

The MP28254 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off

Power Good Indicator

When the FB is below $0.85V_{FB}$, the PG pin will be internally pulled low. When the FB is above $0.9V_{FB}$, the PG becomes an open-drain output. If PG function is not used, it can be left open.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases. 0.1uF ceramic capacitor for decoupling purpose is required.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.805V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable/Sync Control

EN/Sync is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator, drive it low to turn it off. There is an internal 1MEG resistor from EN/Sync to GND thus EN/Sync can be floated to shut down the chip.

1) Enabled by external logic H/L signal

The chip starts up once the enable signal goes higher than EN/SYNC input high voltage (2V), and is shut down when the signal is lower than EN/SYNC input low voltage (0.4V). To disable the chip, EN must be pulled low for at least 5µs. The input is compatible with both CMOS and TTL.

2) Enabled by Vin through voltage divider.

Connect EN with VIN through a resistive voltage divider for automatic startup as the figure 2 shows.

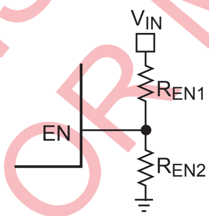


Figure 2—Enable Divider Circuit

Choose the value of the pull-up resistor R_{EN1} and pull-down resistor R_{EN2} to reset the automatic start-up voltage:

$$V_{IN\_START} = V_{EN\_RISING} \cdot \frac{(R_{EN1} + R_{EN2} \parallel 1M\Omega)}{R_{EN2} \parallel 1M\Omega}$$

$$V_{IN\_STOP} = V_{EN\text{-}FALLING} \cdot \frac{(R_{EN1} + R_{EN2} \parallel 1M\Omega)}{R_{EN2} \parallel 1M\Omega}$$

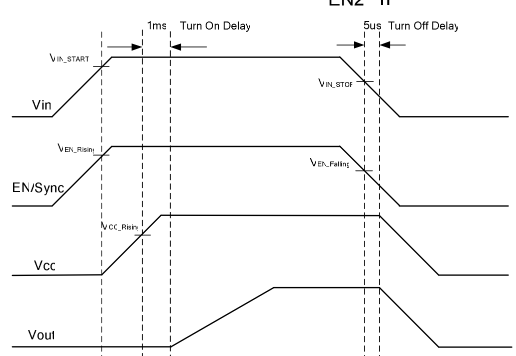


Figure 3—Startup Sequence Using EN Divider

3) Synchronized by External Sync Clock Signal

The chip can be synchronized to external clock range from 300kHz up to 2MHz through this pin 2ms right after output voltage is set, with the internal clock rising edge synchronized to the external clock rising edge.

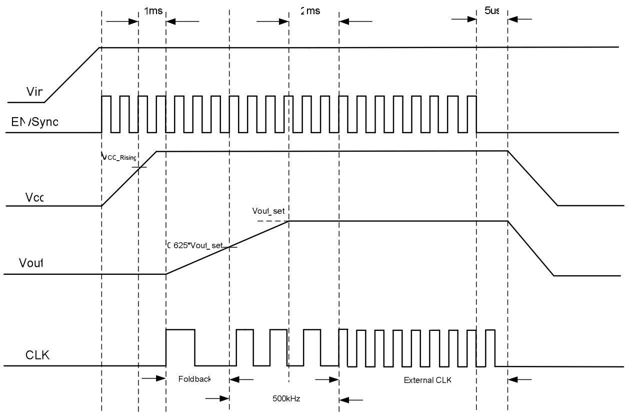


Figure 4—Startup Sequence Using External Sync Clock Signal

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP28254 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 4ms.

Over-Current-Protection and Hiccup

The MP28254 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the MP28254 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MP28254 exits the hiccup mode once the over current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M3, C4, L1 and C2 (Figure 5). If (VIN-VSW) is more than 5V, U2 will regulate M3 to maintain a 5V BST voltage across C4.

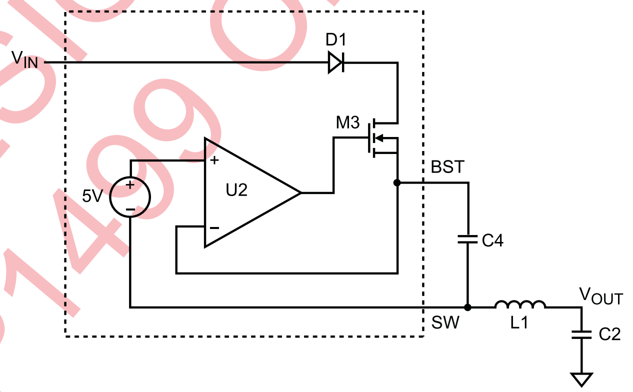


Figure 5—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

The T-type network is highly recommended when Vo is low, as Figure 6 shows.

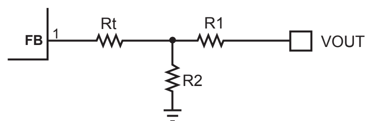


Figure 6— T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	L (uH)	C_{OUT} (uF, Ceramic)
1.05	4.99	16.5	24.9	1-4.7	47
1.2	4.99	10.2	24.9	1-4.7	47
1.5	4.99	5.76	24.9	1-4.7	47
1.8	4.99	4.02	24.9	1-4.7	47
2.5	40.2	19.1	0	1-4.7	47
3.3	40.2	13	0	1-4.7	47
5	40.2	7.68	0	1-4.7	47

Note:
The above feedback resistor table applies to a specific load capacitor condition as shown in the table 1. Other capacitive loading conditions will require different values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor ripple current to be approximately 30% if the maximum load current, 4A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP28254 can be optimized for a wide range of capacitance and ESR values.

PCB Layout

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure 7 for references.

1) Keep the connection of input ground and GND pin as short and wide as possible.

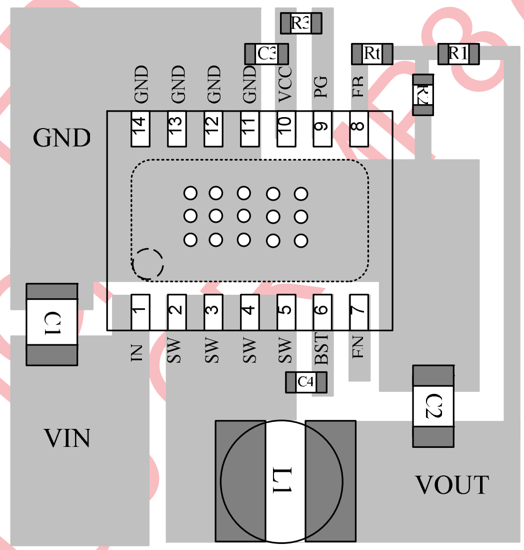
2) Keep the connection of input capacitor and IN pin as short and wide as possible.

3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

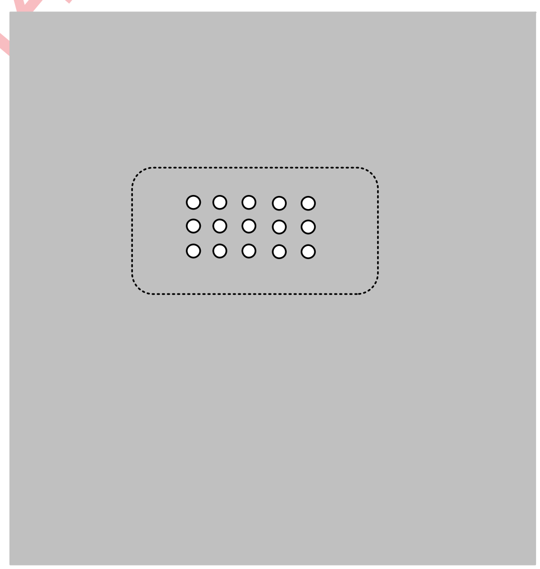
4) Route SW away from sensitive analog areas such as FB.

5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

6) Adding RC snubber circuit from IN pin to SW pin can reduce SW spikes.



Top Layer



Bottom Layer

Figure 7—PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode is:

- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In this case, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 8

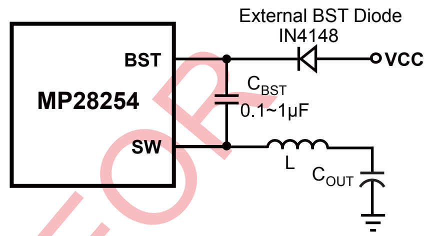
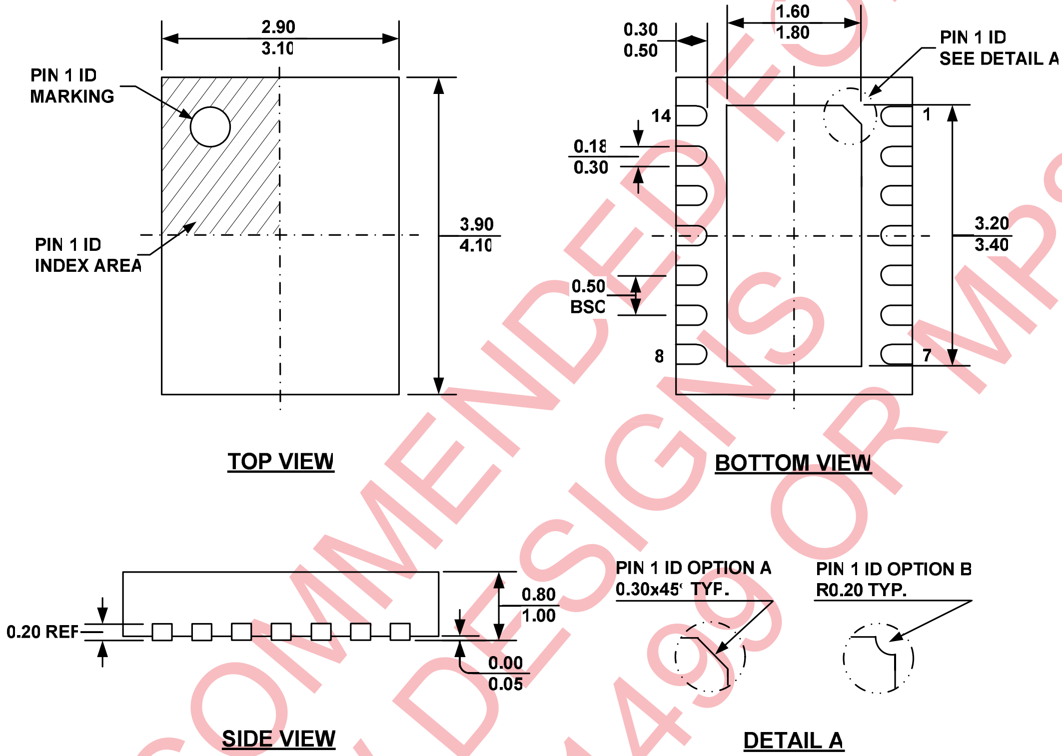


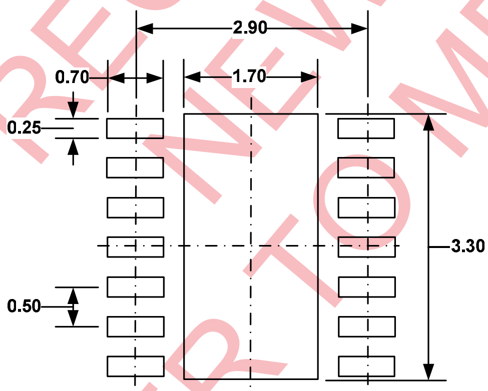
Figure 8—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

PACKAGE INFORMATION

3mm x 4mm QFN14





RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION VGED-3.
5) DRAWING IS NOT TO SCALE.