

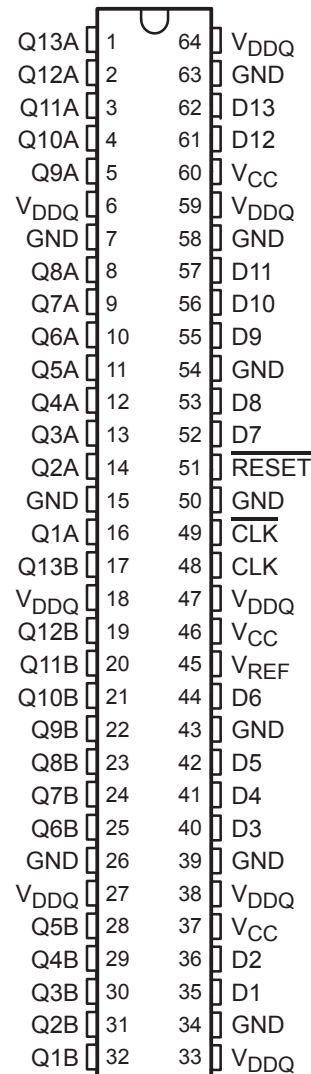
SN74SSTVF16859

13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL_2 INPUTS AND OUTPUTS

SCES429B – MARCH 2003 – REVISED FEBRUARY 2004

- Member of the Texas Instruments Widebus™ Family
- Operates at 2.3 V to 2.7 V for PC1600, PC2100, and PC2700
- Operates at 2.5 V to 2.7 V for PC3200 (QFN Package)
- Pinout and Functionality Compatible With JEDEC Standard SSTV16859
- 600 ps Faster (Simultaneous Switching) Than the JEDEC Standard SSTV16859 in PC2700 DIMM Applications
- 1-to-2 Outputs to Support Stacked DDR DIMMs
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Outputs Meet SSTL_2 Class I Specifications
- Supports SSTL_2 Data Inputs
- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Pinout Optimizes DIMM PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

**DGG PACKAGE
(TOP VIEW)**



description/ordering information

This 13-bit to 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN – RGQ (Tin-Pb Finish)	Tape and reel	SN74SSTVF16859SR	SSF859
	QFN – RGQ (Matte-Tin Finish)		SN74SSTVF16859S8	
	TSSOP – DGG	Tape and reel	SN74SSTVF16859GR	SSTVF16859

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

SN74SSTVF16859

13-BIT TO 26-BIT REGISTERED BUFFER

WITH SSTL_2 INPUTS AND OUTPUTS

SCES429B – MARCH 2003 – REVISED FEBRUARY 2004

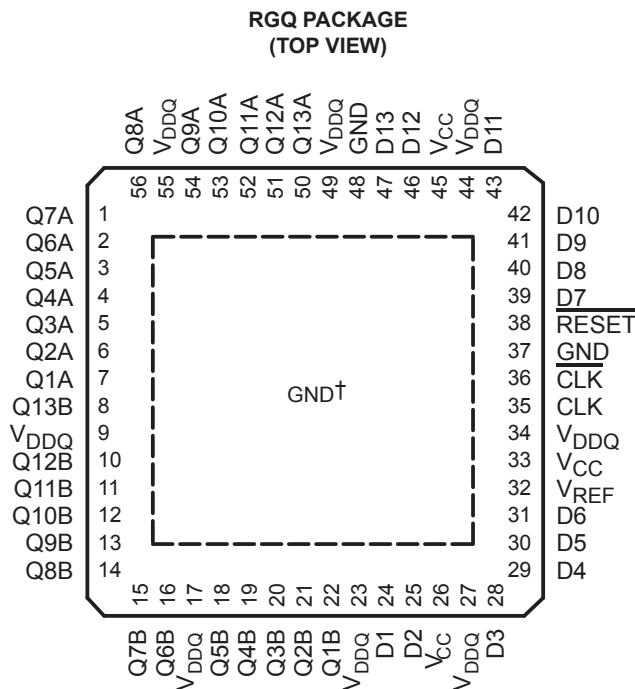
description/ordering information (continued)

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are edge-controlled LVCMOS circuits optimized for unterminated DIMM loads.

The SN74SSTVF16859 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

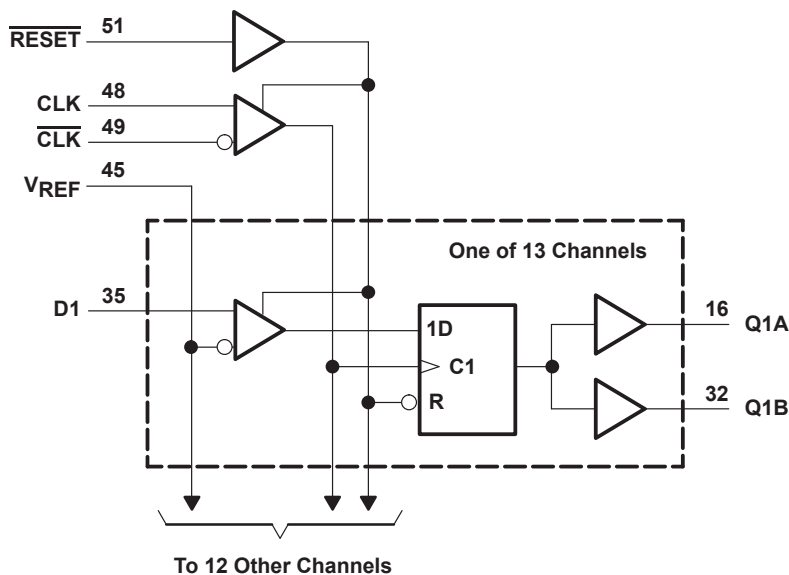


† The center die pad must be connected to GND.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

logic diagram (positive logic)



Pin numbers shown are for the DGG package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ}	-0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	± 50 mA
Continuous current through each V_{CC} , V_{DDQ} , or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	55°C/W
(see Note 4): RGQ package	22°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN74SSTVF16859

13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL 2 INPUTS AND OUTPUTS

SCES429B – MARCH 2003 – REVISED FEBRUARY 2004

recommended operating conditions (see Note 5)

		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	V _{DDQ}		2.7	V	
V _{DDQ}	Output supply voltage	PC1600, PC2100, PC2700		2.7	V	
		PC3200		2.7		
V _{REF}	Reference voltage (V _{REF} = V _{DDQ} /2)	PC1600, PC2100, PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.3	1.35	
V _I	Input voltage	0		V _{CC}	V	
V _{IH}	AC high-level input voltage	Data inputs	V _{REF} +310mV		V	
V _{IL}	AC low-level input voltage	Data inputs		V _{REF} -310mV	V	
V _{IH}	DC high-level input voltage	Data inputs	V _{REF} +150mV		V	
V _{IL}	DC low-level input voltage	Data inputs		V _{REF} -150mV	V	
V _{IH}	High-level input voltage	RESET	1.7		V	
V _{IL}	Low-level input voltage	RESET		0.7	V	
V _{ICR}	Common-mode input voltage range	CLK, CLK	0.97	1.53	V	
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK	360		mV	
I _{OH}	High-level output current			-16	mA	
I _{OL}	Low-level output current			16		
T _A	Operating free-air temperature		0	70	°C	

NOTE 5: The RESET input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless RESET is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics for PC1600, PC2100, and PC2700 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} †	MIN	TYP‡	MAX	UNIT
V _{IK}		I _I = -18 mA	2.3 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	2.3 V to 2.7 V	V _{DDQ} -0.2			V
		I _{OH} = -8 mA	2.3 V	1.95			
V _{OL}		I _{OL} = 100 μA	2.3 V to 2.7 V			0.2	V
		I _{OL} = 8 mA	2.3 V			0.35	
I _I	All inputs	V _I = V _{CC} or GND	2.7 V			±5	μA
I _{CC}	Static standby	RESET = GND	2.7 V			10	μA
	Static operating	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC)				25	
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle	2.5 V			19	μA/ MHz
	Dynamic operating – per each data input	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				7	
C _i §	Data inputs	V _I = V _{REF} ± 310 mV	2.5 V	2.5	3	3.5	pF
	CLK, CLK	V _{ICR} = 1.25 V, V _{I(PP)} = 360mV		2.5	3	3.5	
	RESET	V _I = V _{CC} or GND		2.3	3	3.5	

† For this test condition, V_{DDQ} always is equal to V_{CC}.

‡ All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

§ Measured at 50-MHz input frequency



SN74SSTVF16859
13-BIT TO 26-BIT REGISTERED BUFFER
WITH SSTL 2 INPUTS AND OUTPUTS

SCES429B – MARCH 2003 – REVISED FEBRUARY 2004

electrical characteristics for PC3200 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{IK}		I _I = -18 mA	2.5 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	2.5 V to 2.7 V	V _{DDQ} -0.2			V
		I _{OH} = -8 mA	2.5 V	1.95			
V _{OL}		I _{OL} = 100 μA	2.5 V to 2.7 V			0.2	V
		I _{OL} = 8 mA	2.5 V			0.35	
I _I	All inputs	V _I = V _{CC} or GND	2.7 V			±5	μA
I _{CC}	Static standby	RESET = GND	2.7 V			10	μA
	Static operating	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC)					
I _{CCD}	Dynamic operating - clock only	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle	2.6 V			19	μA/MHz
	Dynamic operating - per each data input	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				7	μA/clock MHz/D input
C _i [§]	Data inputs	V _I = V _{REF} ± 310 mV	2.6 V	2.5	3	3.5	pF
	CLK, CLK	V _{ICR} = 1.25 V, V _I (PP) = 360mV		2.5	3	3.5	
	RESET	V _I = V _{CC} or GND		2.3	3	3.5	

[†] For this test condition, V_{DDQ} always is equal to V_{CC}.

[‡] All typical values are at V_{CC} = 2.6 V, T_A = 25°C.

[§] Measured at 50-MHz input frequency

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 2.5 V ± 0.2 V [†]		V _{CC} = 2.6 V ± 0.1 V [†]		UNIT	
		MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	500		500		MHz	
t _w	Pulse duration, CLK, CLK high or low	1		1		ns	
t _{act}	Differential inputs active time (see Note 6)	22		22		ns	
t _{inact}	Differential inputs inactive time (see Note 7)	22		22		ns	
t _{su}	Setup time	Fast slew rate (see Notes 8 and 10)	Data before CLK↑, CLK↓		0.65	0.65	ns
		Slow slew rate (see Notes 9 and 10)			0.75	0.75	
t _h	Hold time	Fast slew rate (see Notes 8 and 10)	Data after CLK↑, CLK↓		0.65	0.65	ns
		Slow slew rate (see Notes 9 and 10)			0.8	0.8	

[†] For this test condition, V_{DDQ} always is equal to V_{CC}.

NOTES: 6. V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after RESET is taken high.

7. V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after RESET is taken low.

8. For data signal input slew rate ≥ 1 V/ns.

9. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.

10. CLK, CLK signals input slew rates are ≥ 1 V/ns.



SN74SSTVF16859
13-BIT TO 26-BIT REGISTERED BUFFER
WITH SSTL 2 INPUTS AND OUTPUTS

SCES429B – MARCH 2003 – REVISED FEBRUARY 2004

switching characteristics for TSSOP over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V†		UNIT
			MIN	MAX	
f _{max}			500		MHz
t _{pd} ‡	CLK and $\overline{\text{CLK}}$	Q	1.1	2.5	ns
t _{PHL}	$\overline{\text{RESET}}$	Q		5	ns

† For this test condition, V_{DDQ} always is equal to V_{CC}.

‡ Single-bit switching

switching characteristics for QFN over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V†		V _{CC} = 2.6 V ± 0.1 V†		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			500		500		MHz
t _{pd} ‡	CLK and $\overline{\text{CLK}}$	Q	1.1	2.5	1.1	2.2	ns
t _{PHL}	$\overline{\text{RESET}}$	Q		5		5	ns

† For this test condition, V_{DDQ} always is equal to V_{CC}.

‡ Single-bit switching

output slew rates over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V _{CC} = 2.5 V ± 0.2 V†		V _{CC} = 2.6 V ± 0.1 V†		UNIT
			MIN	MAX	MIN	MAX	
dV/dt _r	20%	80%	1	4	1	4	V/ns
dV/dt _f	80%	20%	1	4	1	4	V/ns
dV/dt _Δ §	20% or 80%	80% or 20%		1		1	V/ns

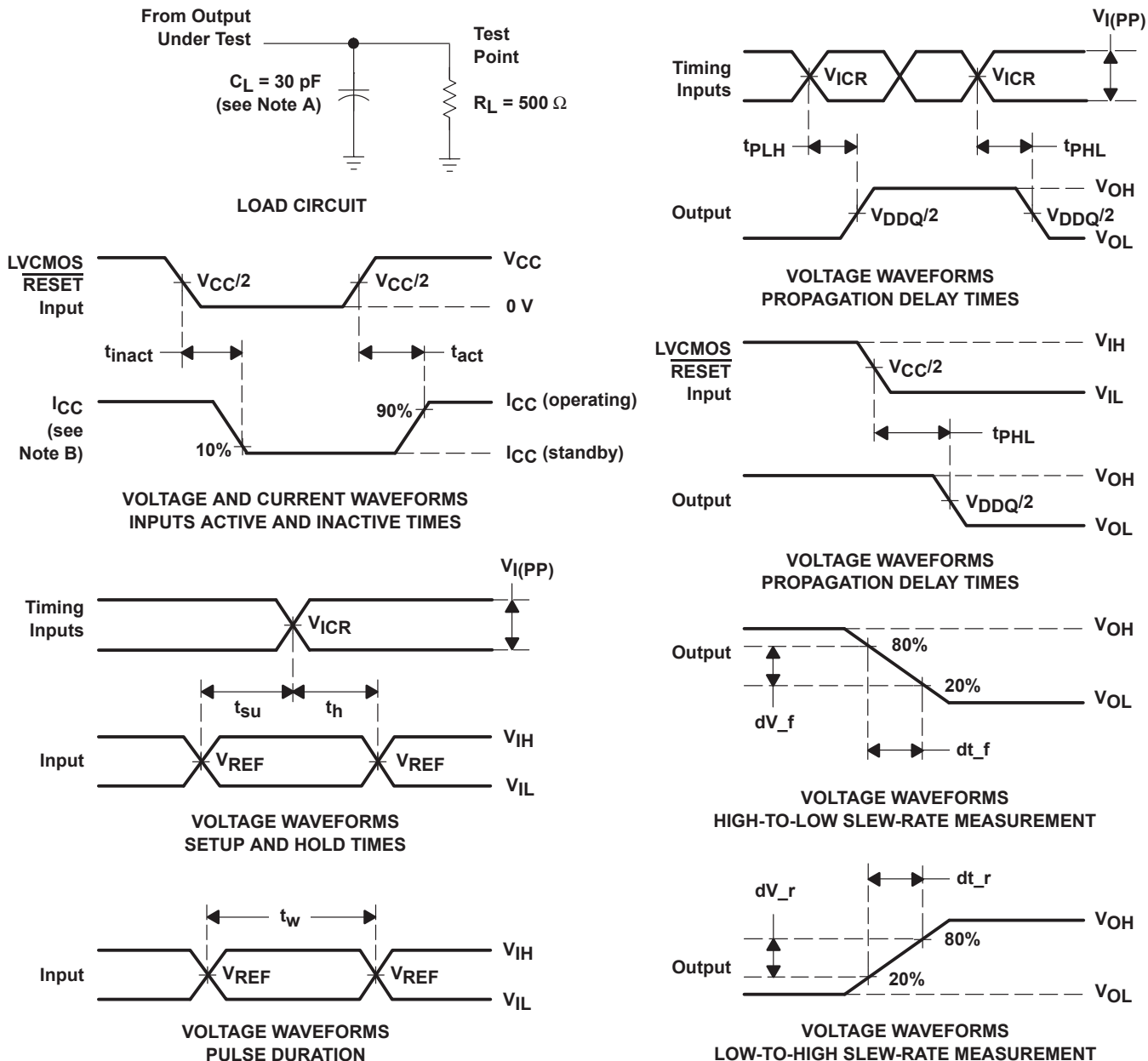
† For this test condition, V_{DDQ} always is equal to V_{CC}.

§ Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).



PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$ AND $V_{CC} = 2.6 V \pm 0.1 V$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and $I_O = 0$ mA.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, input slew rate = 1 V/ns $\pm 20\%$ (unless otherwise noted).
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. $V_{TT} = V_{REF} = V_{DDQ}/2$
 - F. $V_{IH} = V_{REF} + 310$ mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVC MOS input.
 - G. $V_{IL} = V_{REF} - 310$ mV (ac voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS input.
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74SSTVF16859G4RG4	ACTIVE	VQFN	RGQ	56	2000	Green (RoHS & no Sb/Br)	CU	Level-3-260C-168 HR	0 to 70	SSF859	Samples
HPA0002558	ACTIVE	VQFN	RGQ	56	2000	Green (RoHS & no Sb/Br)	CU	Level-3-260C-168 HR	0 to 70	SSF859	Samples
SN74SSTVF16859G4R	ACTIVE	VQFN	RGQ	56	2000	Green (RoHS & no Sb/Br)	CU	Level-3-260C-168 HR	0 to 70	SSF859	Samples
SN74SSTVF16859GR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTVF16859	Samples
SN74SSTVF16859GRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTVF16859	Samples
SN74SSTVF16859S8	ACTIVE	VQFN	RGQ	56	2000	Green (RoHS & no Sb/Br)	CU	Level-3-260C-168 HR	0 to 70	SSF859	Samples
SN74SSTVF16859S8G3	ACTIVE	VQFN	RGQ	56	2000	Green (RoHS & no Sb/Br)	CU	Level-3-260C-168 HR	0 to 70	SSF859	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



www.ti.com

PACKAGE OPTION ADDENDUM

15-Apr-2017

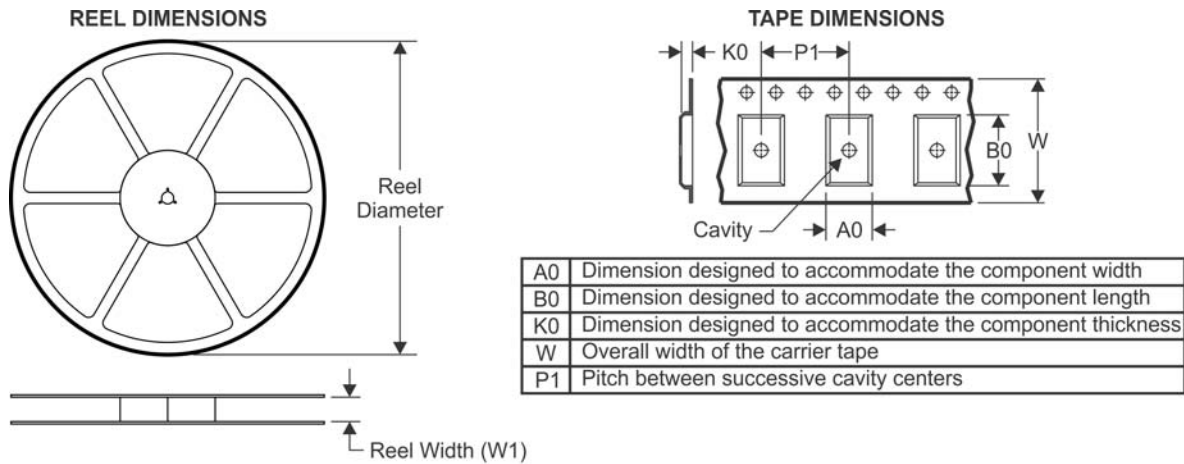
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

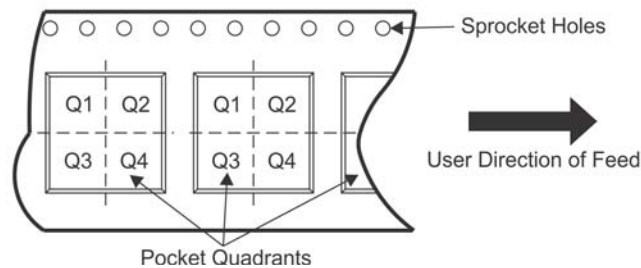
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



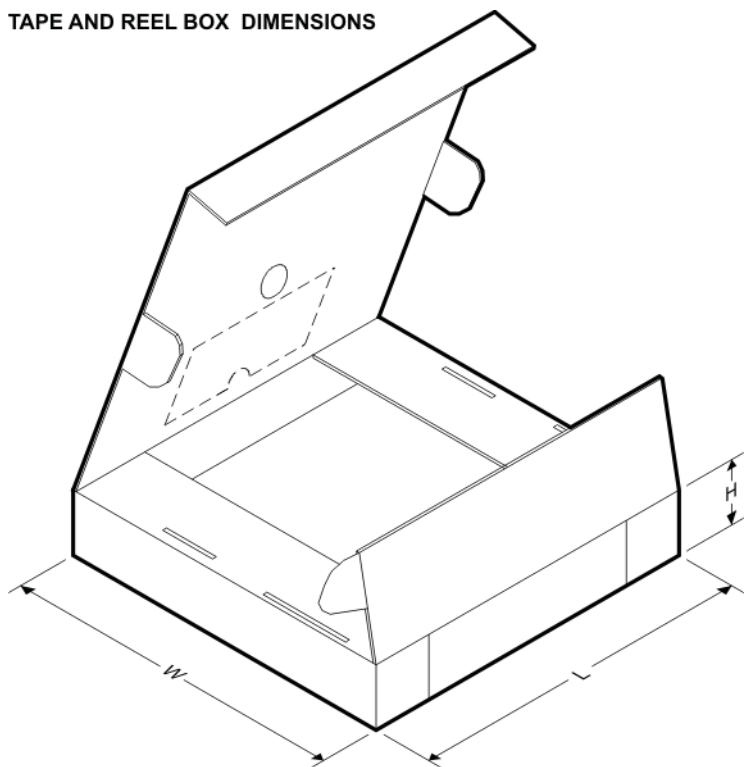
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTVF16859GR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

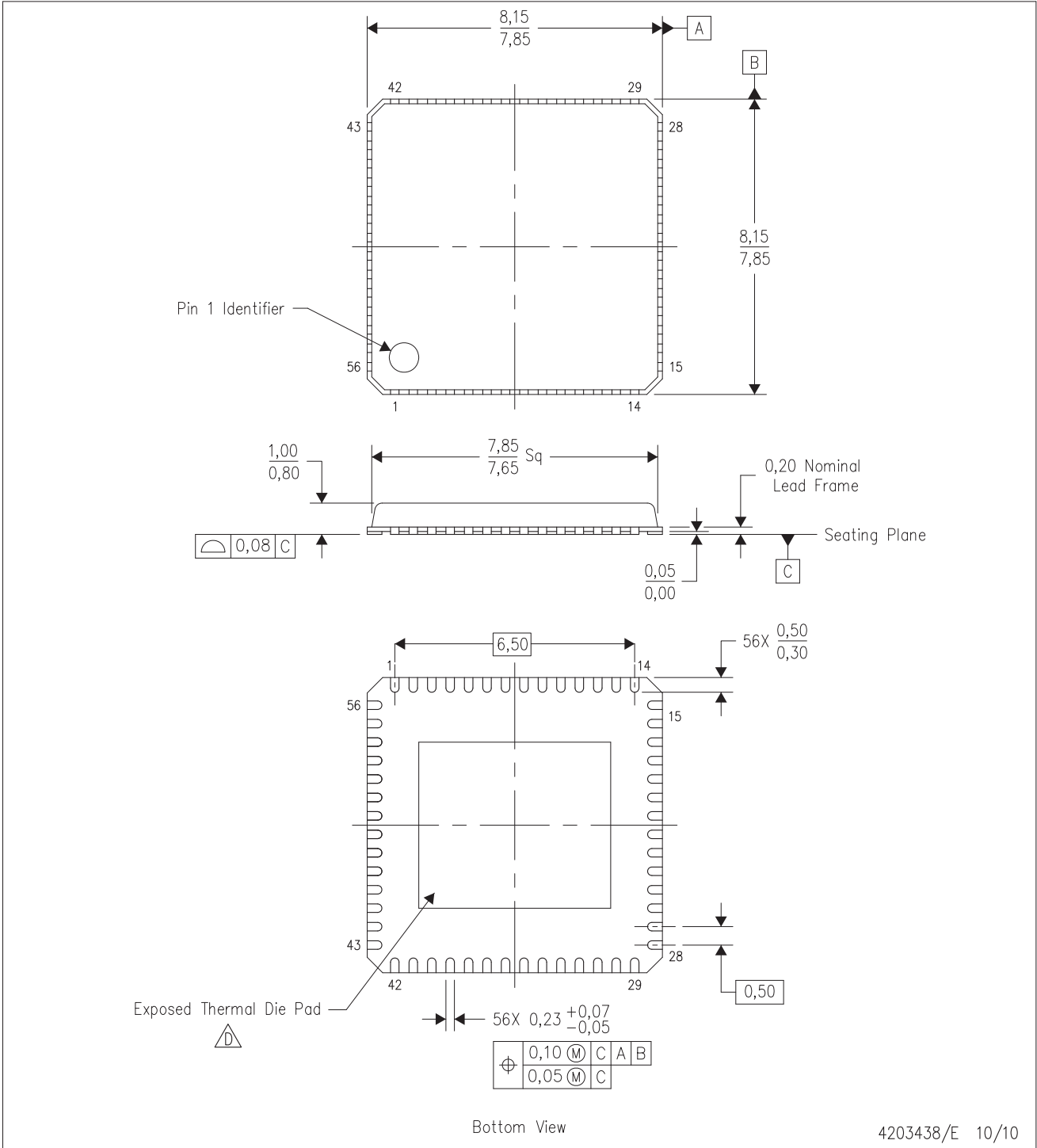


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTVF16859GR	TSSOP	DGG	64	2000	367.0	367.0	45.0


RGQ (S-PVQFN-N56)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203438/E 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-220 variation VLLD-2.

THERMAL PAD MECHANICAL DATA

RGQ (S-PVQFN-N56)

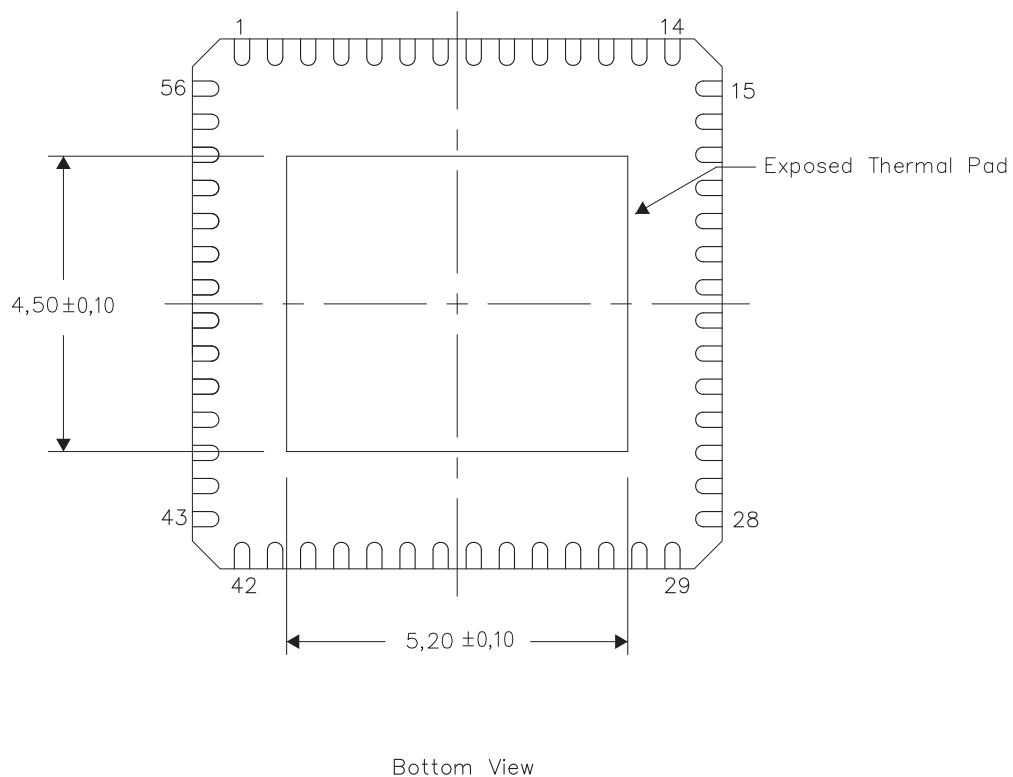
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



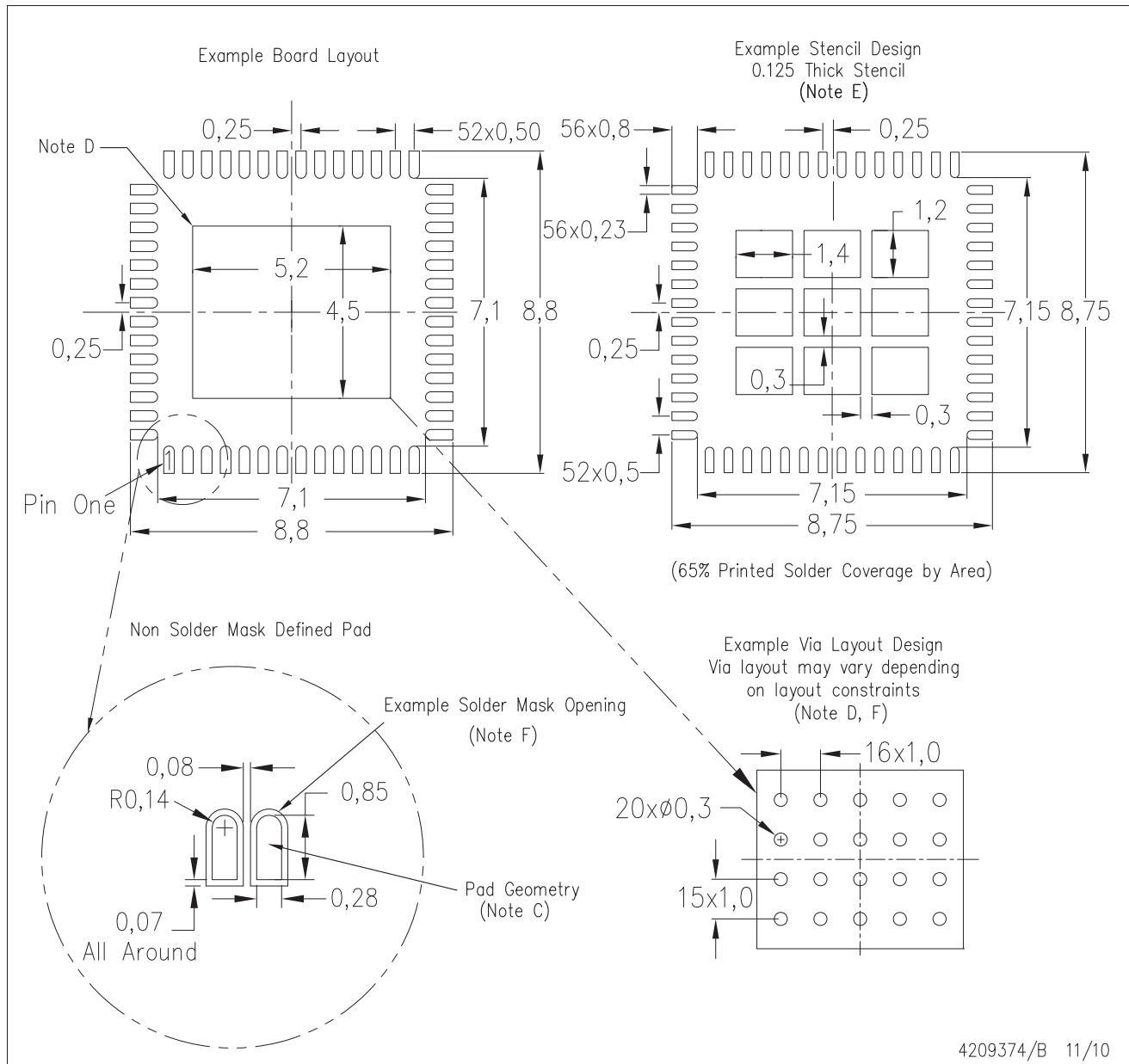
Exposed Thermal Pad Dimensions

4206347/D 12/10

NOTE: A. All linear dimensions are in millimeters

RGQ (S-PVQFN-N56)

PLASTIC QUAD FLATPACK NO-LEAD



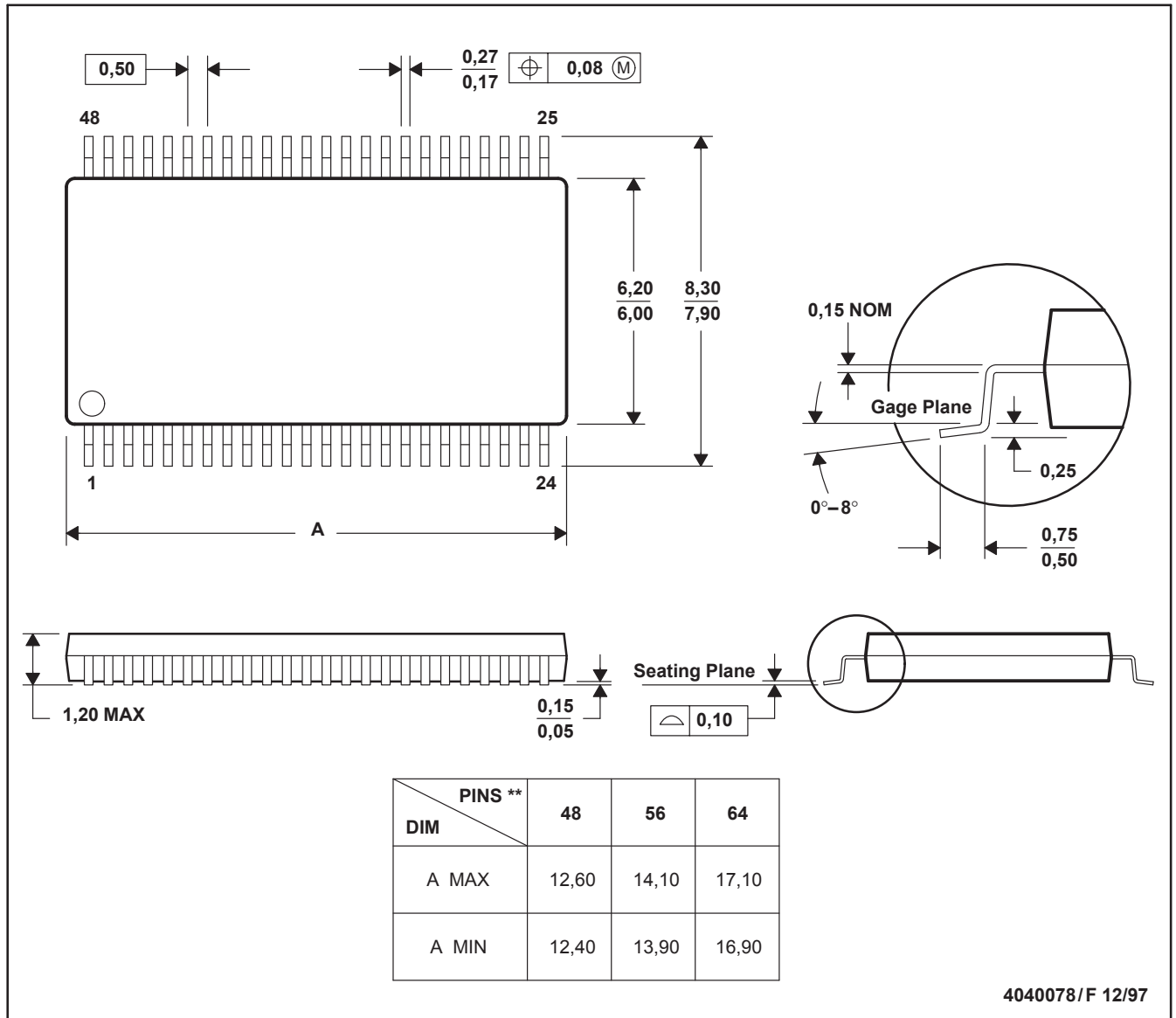
4209374/B 11/10

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153