# Special Function Logic Gate

# NLSF457

### Description

The NLSF457 is a single special function gate in tiny footprint package.

### Features

- Designed for 1.65 V to 5.5 V $V_{CC}$ Operation
- 2.7 ns $t_{PD}$ at 5 V (typ)
- Inputs/Outputs Over−Voltage Tolerant up to 5.5 V
- $I_{OFF}$ Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in 1.45 mm x 1.0 mm UDFN8 Package
- Chip Complexity < 100 FETs
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

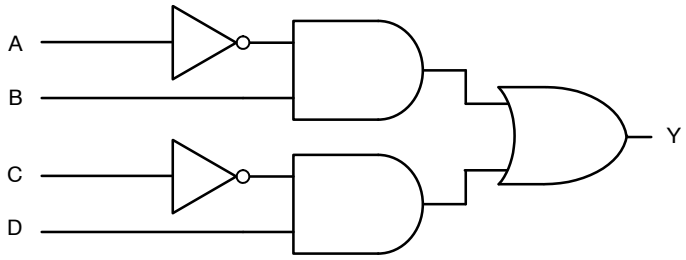


**Figure 1. Logic Diagram**

**ON Semiconductor®**

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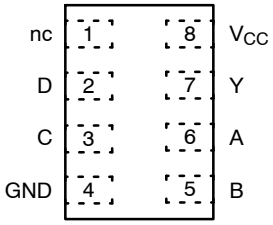
**UDFN8, 1.45x1, 0.35P**
**CASE 517EB**

### MARKING DIAGRAM


XX = Specific Device Code
M = Assembly Operation Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Assembly Operation Code orientation and/or may vary depending upon manufacturing location.

### PIN ASSIGNMENT




| Pin | Name | Description |
|---|---|---|
| 1 | nc | No Connect |
| 2 | D | Input |
| 3 | C | Input |
| 4 | GND | Ground |
| 5 | B | Input |
| 6 | A | Input |
| 7 | Y | Output |
| 8 | $V_{CC}$ | Power Supply |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

**Table 1. FUNCTION TABLE**

| Input | | | | Output |
|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

## MAXIMUM RATINGS

| Symbol | Parameter | | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +6.5 | V |
| $V_{OUT}$ | DC Output Voltage | Active−Mode (High or Low State) | −0.5 to $V_{CC}$+0.5 | V |
| | | Tri−State Mode (Note 1) | −0.5 to +6.5 | |
| | | Power−Down Mode ($V_{CC}$ = 0 V) | −0.5 to +6.5 | |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < GND | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND | −50 | mA |
| $I_{OUT}$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ or $I_{GND}$ | DC Supply Current Per Supply Pin or Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | UDFN8 | 231 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 125°C | UDFN8 | 541 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3) | Charged Device Model | > 2000 | V |
| | | Human Body Model | > 1000 | |
| $I_{LATCHUP}$ | Latchup Performance (Note 4) | | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm − by − 1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | 1.65 | 5.5 | V |
| $V_{IN}$ | Digital Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage | Active Mode (High or Low State) | 0 | $V_{CC}$ | V |
| | | Tri−State Mode (Note 1) | 0 | 5.5 | |
| | | Power Down Mode ($V_{CC}$ = 0 V) | 0 | 5.5 | |
| $T_A$ | Operating Free−Air Temperature | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Transition Rise or Fall Rate | $V_{CC}$ = 1.65 V to 1.95 V | 0 | 20 | nS/V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 20 | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0 | 10 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0 | 5 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High−Level Input Voltage | | 1.65 to 1.95 | 0.65 x $V_{CC}$ | − | − | 0.65 x $V_{CC}$ | − | V |
| | | | 2.3 to 5.5 | 0.70 x $V_{CC}$ | − | − | 0.70 x $V_{CC}$ | − | |
| $V_{IL}$ | Low−Level Input Voltage | | 1.65 to 1.95 | − | − | 0.35 x $V_{CC}$ | − | 0.35 x $V_{CC}$ | V |
| | | | 2.3 to 5.5 | − | − | 0.30 x $V_{CC}$ | − | 0.30 x $V_{CC}$ | |
| $V_{OH}$ | High−Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −100 μA<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA<br>$I_{OH}$ = −12 mA<br>$I_{OH}$ = −16 mA<br>$I_{OH}$ = −24 mA<br>$I_{OH}$ = −32 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | <br>$V_{CC}$ − 0.1<br>1.29<br>1.9<br>2.2<br>2.4<br>2.3<br>3.8 | <br>$V_{CC}$<br>1.4<br>2.1<br>2.4<br>2.7<br>2.5<br>4.0 | − | <br>$V_{CC}$ − 0.1<br>1.29<br>1.9<br>2.2<br>2.4<br>2.3<br>3.8 | − | V |
| $V_{OL}$ | Low−Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 100 μA<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA<br>$I_{OL}$ = 12 mA<br>$I_{OL}$ = 16 mA<br>$I_{OL}$ = 24 mA<br>$I_{OL}$ = 32 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | − | <br><br>0.08<br>0.2<br>0.22<br>0.28<br>0.38<br>0.42 | <br>0.1<br>0.24<br>0.3<br>0.4<br>0.4<br>0.55<br>0.55 | − | <br>0.1<br>0.24<br>0.3<br>0.4<br>0.4<br>0.55<br>0.55 | V |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 1.65 to 5.5 | − | − | ±0.1 | − | ±1.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{IN}$ = 5.5 V or $V_{OUT}$ = 5.5 V | 0 | − | − | 1.0 | − | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND | 5.5 | − | − | 1.0 | − | 10 | μA |

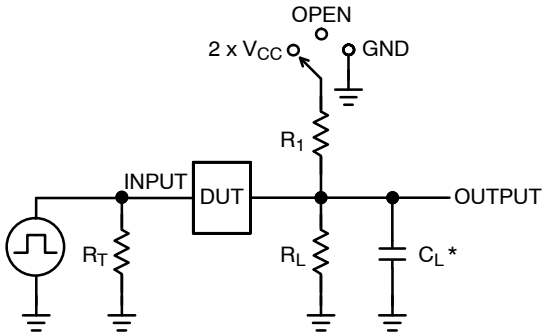
## AC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, (A or B or C or D) to Y (Figures 3 and 4) | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 1.65 to 1.95 | − | 7.7 | 10 | − | 10.5 | ns |
| | | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 2.3 to 2.7 | − | 4.2 | 7.5 | − | 8.0 | |
| | | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 3.0 to 3.6 | − | 3.0 | 5.2 | − | 5.5 | |
| | | $R_L$ = 500 Ω, $C_L$ = 50 pF | | − | 3.5 | 5.7 | − | 6.0 | |
| | | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 4.5 to 5.5 | − | 2.3 | 4.5 | − | 4.8 | |
| | | $R_L$ = 500 Ω, $C_L$ = 50 pF | | − | 2.6 | 5.0 | − | 5.3 | |

## CAPACITAVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | Typical ($T_A$ = 25 °C) | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$ | 2.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$ | 2.5 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | 10 MHz, $V_{CC}$ = 3.3 V, $V_{IN}$ = 0 V or $V_{CC}$ | 9 | pF |
| | | 10 MHz, $V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$ | 11 | |

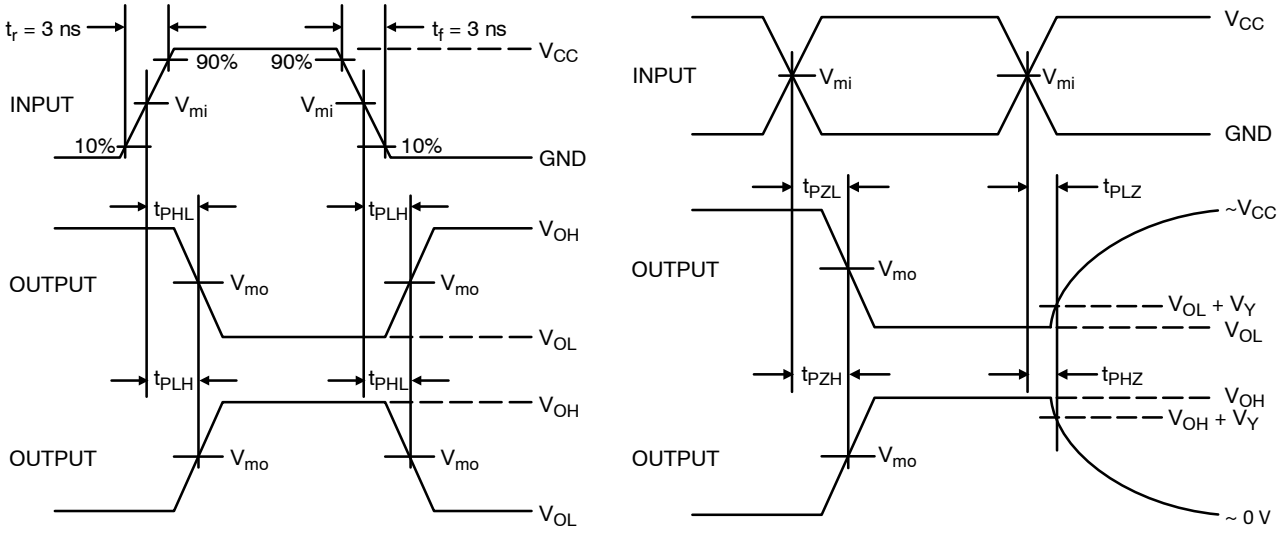
5. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)}$ = $C_{PD}$ • $V_{CC}$ • $f_{in}$ + $I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption: $P_D$ = $C_{PD}$ • $V_{CC}^2$ • $f_{in}$ + $I_{CC}$ • $V_{CC}$.




$C_L$ includes probe and jig capacitance
$R_T$ is $Z_{OUT}$ of pulse generator (typicaly 50 Ω)
f = 1 MHz

| Test | Switch Position | $C_L$, pF | $R_L$, Ω | $R_1$, Ω |
|---|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | See AC Characteristics Table | | |
| $t_{PLZ}$ / $t_{PZL}$ | 2 x $V_{CC}$ | 50 | 500 | 500 |
| $t_{PHZ}$ / $t_{PZH}$ | GND | 50 | 500 | 500 |

**Figure 2. Test Circuit**




| $V_{CC}$, V | $V_{mi}$, V | $V_{mo}$, V | | $V_Y$, V |
|---|---|---|---|---|
| | | $t_{PLH}$, $t_{PHL}$ | $t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$ | |
| 1.65 to 1.95 | $V_{CC}$/2 | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 2.3 to 2.7 | $V_{CC}$/2 | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 3.0 to 3.6 | $V_{CC}$/2 | $V_{CC}$/2 | $V_{CC}$/2 | 0.3 |
| 4.5 to 5.5 | $V_{CC}$/2 | $V_{CC}$/2 | $V_{CC}$/2 | 0.3 |

**Figure 3. Switching Waveforms**

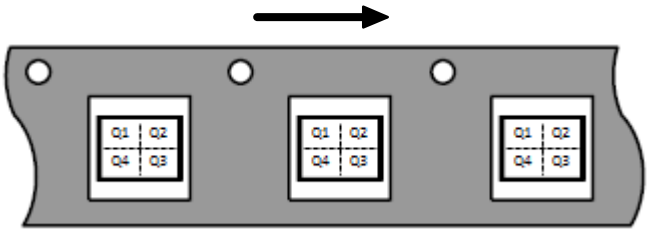
## ORDERING INFORMATION

| Device | Package | Marking | Pin 1 Orientation (see bellow) | Shipping† |
|---|---|---|---|---|
| NLSF457MU3TCG | UDFN8, 1.45 x 1.0, 0.35P | AA | Q4 | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC – Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel
Direction of Feed

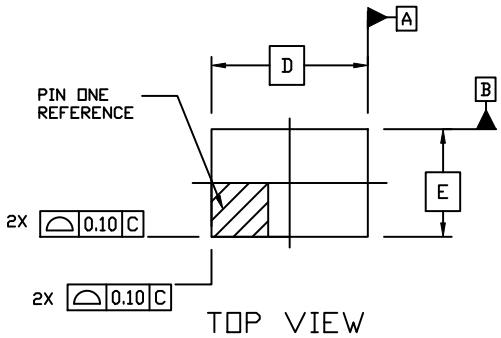


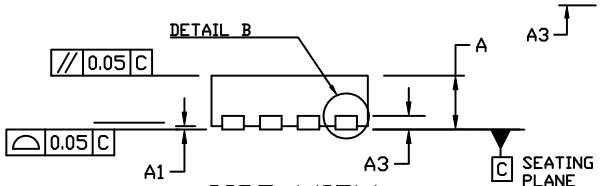
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

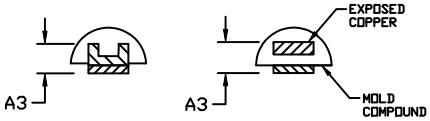
ON Semiconductor®

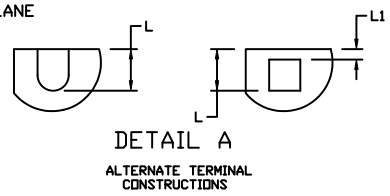
**UDFN8, 1.45x1.0, 0.35P**
CASE 517EB
ISSUE O

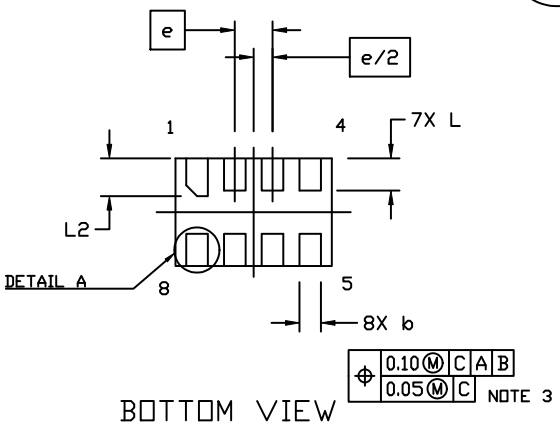
DATE 27 AUG 2018



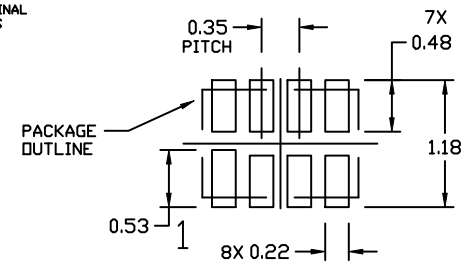




NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. PACKAGE DIMENSIONS EXCUSIVE OF BURRS AND MOLD FLASH.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 0.45 | 0.50 | 0.55 |
| A1 | --- | --- | 0.05 |
| A3 | 0.13 REF | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 1.35 | 1.45 | 1.55 |
| E | 0.90 | 1.00 | 1.10 |
| e | 0.35 BSC | | |
| L | 0.25 | 0.30 | 0.35 |
| L1 | 0.05 | 0.10 | 0.15 |
| L2 | 0.30 | 0.35 | 0.40 |




For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***


XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON97212G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **UDFN8, 1.45x1.0, 0.35P** | **PAGE 1 OF 1** |

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