# SN74LV2T74-Q1 Automotive Dual D-Type Flip-Flop With Integrated Translation

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in wettable flank QFN (WBQA) package
- Wide operating range of 1.8 V to 5.5 V
- Single-supply voltage translator (refer to *LVxT Enhanced Input Voltage*):
  - Up translation:
    - 1.2 V to 1.8 V
    - 1.5 V to 2.5 V
    - 1.8 V to 3.3 V
    - 3.3 V to 5.0 V
  - Down translation:
    - 5.0 V, 3.3 V, 2.5 V to 1.8 V
    - 5.0 V, 3.3 V to 2.5 V
    - 5.0 V to 3.3 V
- 5.5-V tolerant input pins
- Supports standard pinouts
- Up to 150 Mbps with 5-V or 3.3-V $V_{CC}$
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- Convert a momentary switch to a toggle switch
- Hold a signal during controller reset
- Input slow edge-rate signals
- Operate in noisy environments
- Divide a clock signal by two

## 3 Description

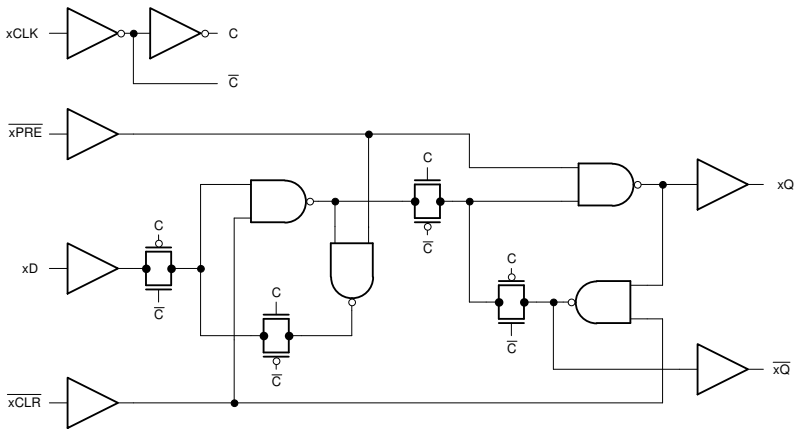
The SN74LV2T74-Q1 contains two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) input sets the output high. A low level at the clear ($\overline{CLR}$) input resets the output low. Preset and clear functions are asynchronous and not dependent on the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs (Q, $\overline{Q}$) on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the input clock (CLK) signal. Following the hold-time interval, data at the data (D) input can be changed without affecting the levels at the outputs (Q, $\overline{Q}$). The output level is referenced to the supply voltage ($V_{CC}$) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs (for example, 1.2 V input to 1.8 V output or 1.8 V input to 3.3 V output). In addition, the 5-V tolerant input pins enable down translation (for example, 3.3 V to 2.5 V output).

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE (NOM)(3) |
|---|---|---|---|
| SN74LV2T74-Q1 | BQA (WQFN, 14) | 3 mm × 2.5 mm | 3 mm × 2.5 mm |
| | PW (TSSOP, 14) | 5 mm × 6.4 mm | 5 mm × 4.4 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Simplified Logic Diagram (Positive Logic)**

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## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| May 2023 | * | Initial Release |

## 5 Pin Configuration and Functions

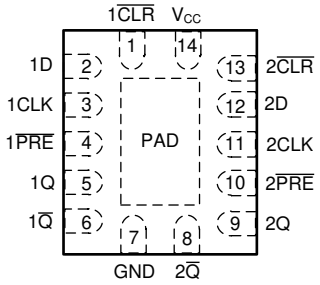



**Figure 5-1. BQA Package, 14-Pin WQFN (Top View)**

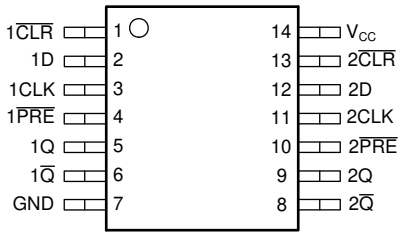



**Figure 5-2. PW Package, 14-Pin TSSOP (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1$\overline{CLR}$ | 1 | Input | Clear for channel 1, active low |
| 1D | 2 | Input | Data for channel 1 |
| 1CLK | 3 | Input | Clock for channel 1, rising edge triggered |
| 1$\overline{PRE}$ | 4 | Input | Preset for channel 1, active low |
| 1Q | 5 | Output | Output for channel 1 |
| 1$\overline{Q}$ | 6 | Output | Inverted output for channel 1 |
| GND | 7 | — | Ground |
| 2$\overline{Q}$ | 8 | Output | Inverted output for channel 2 |
| 2Q | 9 | Output | Output for channel 2 |
| 2$\overline{PRE}$ | 10 | Input | Preset for channel 2, active low |
| 2CLK | 11 | Input | Clock for channel 2, rising edge triggered |
| 2D | 12 | Input | Data for channel 2 |
| 2$\overline{CLR}$ | 13 | Input | Clear for channel 2, active low |
| $V_{CC}$ | 14 | — | Positive supply |
| Thermal Pad(1) | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply |

(1) BQA package only.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < -0.5 V | | -20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < -0.5 V or $V_O$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous output current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B | ±1000 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.6 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 2 V | 1.1 | | V |
| | | $V_{CC}$ = 2.25 V to 2.75 V | 1.28 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 1.45 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | |
| $V_{IL}$ | Low-Level input voltage | $V_{CC}$ = 1.65 V to 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.25 V to 2.75 V | | 0.65 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.75 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.85 | |
| $I_O$ | Output current | $V_{CC}$ = 1.6 V to 2 V | | ±3 | mA |
| | | $V_{CC}$ = 2.25 V to 2.75 V | | ±7 | |
| | | $V_{CC}$ = 3.3 V to 5.0 V | | ±15 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.6 V to 5.0 V | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV2T74-Q1 | | UNIT |
|---|---|---|---|---|
| | | WBQA (WQFN) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 88.3 | 151.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 90.9 | 80.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.8 | 94.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 9.9 | 28.0 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 56.7 | 93.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 33.4 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = -50 µA | 1.65 V to 5.5 V | $V_{CC}$-0.1 | | | $V_{CC}$-0.1 | | | V |
| | $I_{OH}$ = -2 mA | 1.65 V to 2 V | 1.28 | 1.7 (1) | | 1.21 | | | |
| | $I_{OH}$ = -3 mA | 2.25 V to 2.75 V | 2 | 2.4(1) | | 1.93 | | | |
| | $I_{OH}$ = -5.5 mA | 3 V to 3.6 V | 2.6 | 3.08(1) | | 2.49 | | | |
| | $I_{OH}$ = -8 mA | 4.5 V to 5.5 V | 4.1 | 4.65(1) | | 3.95 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 1.65 V to 2 V | | 0.1(1) | 0.2 | | | 0.25 | |
| | $I_{OL}$ = 3 mA | 2.25 V to 2.75 V | | 0.1(1) | 0.15 | | | 0.2 | |
| | $I_{OL}$ = 5.5 mA | 3 V to 3.6 V | | 0.2(1) | 0.2 | | | 0.25 | |
| | $I_{OL}$ = 8 mA | 4.5 V to 5.5 V | | 0.3(1) | 0.3 | | | 0.35 | |
| $I_I$ | $V_I$ = 0 V or $V_{CC}$ | 0 V to 5.5 V | | | ±0.1 | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = 0 V or $V_{CC}$, $I_O$ = 0; open on loading | 1.65 V to 5.5 V | | | 2 | | | 20 | µA |
| $\Delta I_{CC}$ | One input at 0.3 V or 3.4 V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 5.5 V | | | 1.35 | | | 1.5 | mA |
| | One input at 0.3 V or 1.1 V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 1.8 V | | | 10 | | | 20 | µA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | 10 | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 3 | | | | | pF |
| $C_{PD}$ (2) (3) | No load, F = 1 MHz | 5 V | | 14 | | | | | pF |

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)
(2) $C_{PD}$ is used to determine the dynamic power consumption, per channel.
(3) $P_D = V_{CC}^2 \times F_I \times (C_{PD} + C_L)$ where $F_I$= input frequency, $C_L$= output load capacitance, $V_{CC}$= supply voltage.

## 6.6 Timing Characteristics 1.8-V $V_{CC}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | $T_A$ = 25°C | | -40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_W$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ LOW | 8 | | 9 | | nS |
| $t_W$ | Pulse duration | CLK | 8 | | 9 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | Data | 8 | | 9 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | $\overline{PRE}$ or $\overline{CLR}$ Inactive | 7 | | 7 | | nS |
| $t_H$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | nS |

## 6.7 Timing Characteristics 2.5-V $V_{CC}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | $T_A$ = 25°C | | -40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_W$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ LOW | 7 | | 8 | | nS |
| $t_W$ | Pulse duration | CLK | 7 | | 8 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | Data | 7 | | 8 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | $\overline{PRE}$ or $\overline{CLR}$ Inactive | 6 | | 6 | | nS |
| $t_H$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | nS |

## 6.8 Timing Characteristics 3.3-V $V_{CC}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | $T_A$ = 25°C | | -40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_W$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ LOW | 6 | | 7 | | nS |
| $t_W$ | Pulse duration | CLK | 6 | | 7 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | Data | 6 | | 7 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | $\overline{PRE}$ or $\overline{CLR}$ Inactive | 5 | | 5 | | nS |
| $t_H$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | nS |

## 6.9 Timing Characteristics 5-V $V_{CC}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | $T_A$ = 25°C | | -40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_W$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ LOW | 5 | | 5 | | nS |
| $t_W$ | Pulse duration | CLK | 5 | | 5 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | Data | 5 | | 5 | | nS |
| $t_{SU}$ | Setup time before CLK↑ | $\overline{PRE}$ or $\overline{CLR}$ Inactive | 3 | | 3 | | nS |
| $t_H$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | nS |

## 6.10 Switching Characteristics 1.8-V $V_{CC}$

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $F_{MAX}$ | | | $C_L$ = 15 pF | 34 | 53 | | 30 | | | MHz |
| | | | $C_L$ = 50 pF | 21 | 32 | | 19 | | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 14.8 | 24.0 | 1 | | 28.3 | nS |
| $t_{PHL}$ | | | | | 14.8 | 24.0 | 1 | | 28.3 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 13.1 | 23.2 | 1 | | 27.3 | nS |
| $t_{PHL}$ | | | | | 13.1 | 23.2 | 1 | | 27.3 | nS |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 19.7 | 30.8 | 1 | | 35.1 | nS |
| $t_{PHL}$ | | | | | 19.7 | 30.8 | 1 | | 35.1 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 17.9 | 30.0 | 1 | | 34.1 | nS |
| $t_{PHL}$ | | | | | 17.9 | 30.0 | 1 | | 34.1 | nS |

## 6.11 Switching Characteristics 2.5-V $V_{CC}$

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $F_{MAX}$ | | | $C_L$ = 15 pF | 52 | 81 | | 46 | | | MHz |
| | | | $C_L$ = 50 pF | 33 | 49 | | 29 | | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 9.9 | 16.0 | 1 | | 18.9 | nS |
| $t_{PHL}$ | | | | | 9.9 | 16.0 | 1 | | 18.9 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 8.7 | 15.5 | 1 | | 18.2 | nS |
| $t_{PHL}$ | | | | | 8.7 | 15.5 | 1 | | 18.2 | nS |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 13.1 | 20.5 | 1 | | 23.4 | nS |
| $t_{PHL}$ | | | | | 13.1 | 20.5 | 1 | | 23.4 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 12.0 | 20.0 | 1 | | 22.8 | nS |
| $t_{PHL}$ | | | | | 12.0 | 20.0 | 1 | | 22.8 | nS |

## 6.12 Switching Characteristics 3.3-V $V_{CC}$

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $F_{MAX}$ | | | $C_L$ = 15 pF | 80 | 125 | | 70 | | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.6 | 12.3 | 1 | | 14.5 | nS |
| $t_{PHL}$ | | | | | 7.6 | 12.3 | 1 | | 14.5 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 6.7 | 11.9 | 1 | | 14 | nS |
| $t_{PHL}$ | | | | | 6.7 | 11.9 | 1 | | 14 | nS |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 10.1 | 15.8 | 1 | | 18 | nS |
| $t_{PHL}$ | | | | | 10.1 | 15.8 | 1 | | 18 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 9.2 | 15.4 | 1 | | 17.5 | nS |
| $t_{PHL}$ | | | | | 9.2 | 15.4 | 1 | | 17.5 | nS |

## 6.13 Switching Characteristics 5-V $V_{CC}$

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $F_{MAX}$ | | | $C_L$ = 15 pF | 130 | 170 | | 110 | | | MHz |
| | | | $C_L$ = 50 pF | 90 | 140 | | 75 | | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 4.8 | 7.7 | 1 | | 9 | nS |
| $t_{PHL}$ | | | | | 4.8 | 7.7 | 1 | | 9 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 4.6 | 7.3 | 1 | | 8.5 | nS |
| $t_{PHL}$ | | | | | 4.6 | 7.3 | 1 | | 8.5 | nS |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 6.3 | 9.7 | 1 | | 11 | nS |
| $t_{PHL}$ | | | | | 6.3 | 9.7 | 1 | | 11 | nS |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 6.1 | 9.3 | 1 | | 10 | nS |
| $t_{PHL}$ | | | | | 6.1 | 9.3 | 1 | | 10 | nS |

## 6.14 Noise Characteristics

VCC = 5 V, CL = 50 pF, TA = 25°C

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.9 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | -0.8 | -0.3 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | 5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.1 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.5 | V |

## 6.15 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

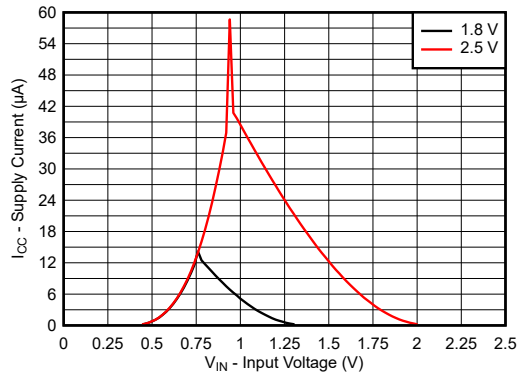



**Figure 6-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply**

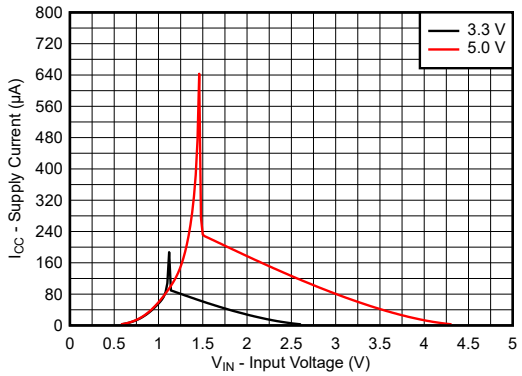



**Figure 6-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply**

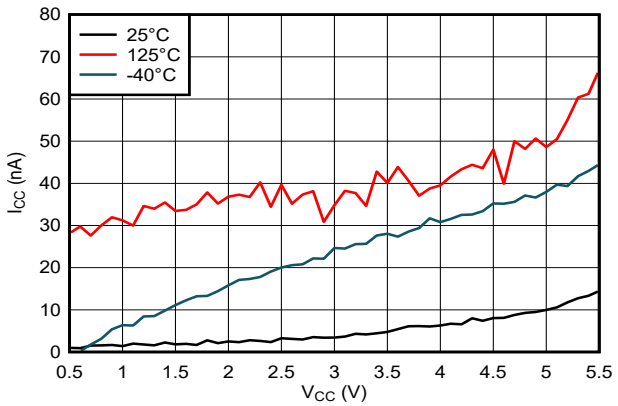



**Figure 6-3. Supply Current Across Supply Voltage**

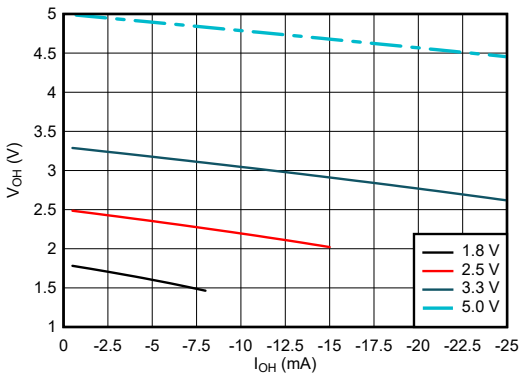



**Figure 6-4. Output Voltage vs Current in HIGH State**

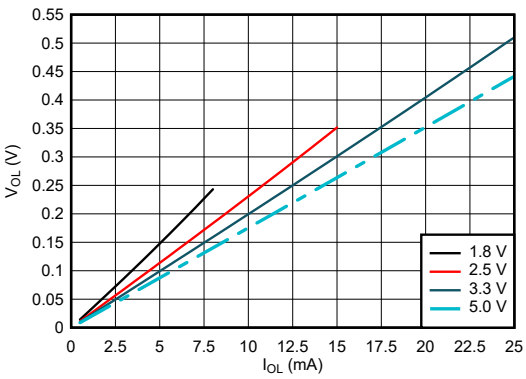



**Figure 6-5. Output Voltage vs Current in LOW State**

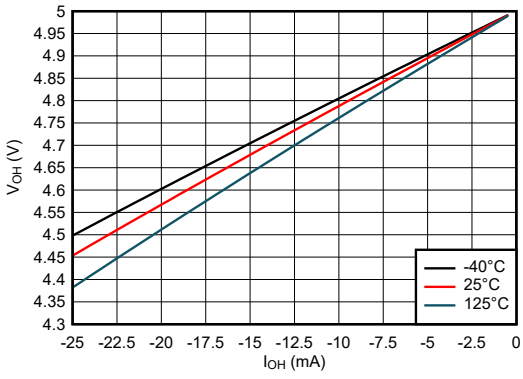



**Figure 6-6. Output Voltage vs Current in HIGH State; 5-V Supply**

## 6.15 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

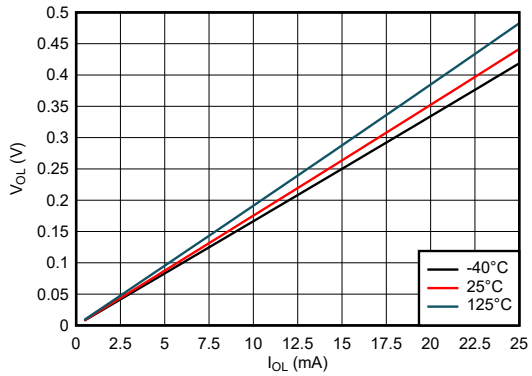



**Figure 6-7. Output Voltage vs Current in LOW State; 5-V Supply**

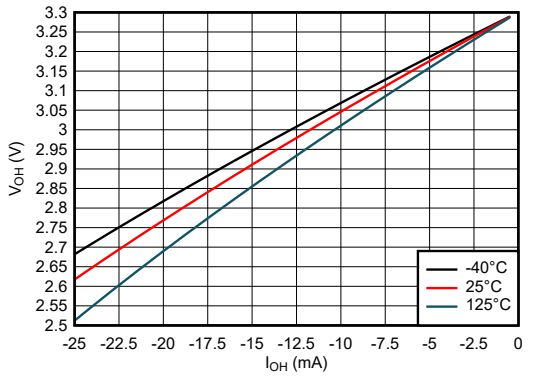



**Figure 6-8. Output Voltage vs Current in HIGH State; 3.3-V Supply**

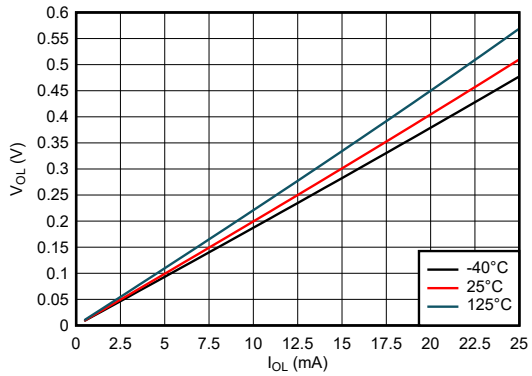



**Figure 6-9. Output Voltage vs Current in LOW State; 3.3-V Supply**

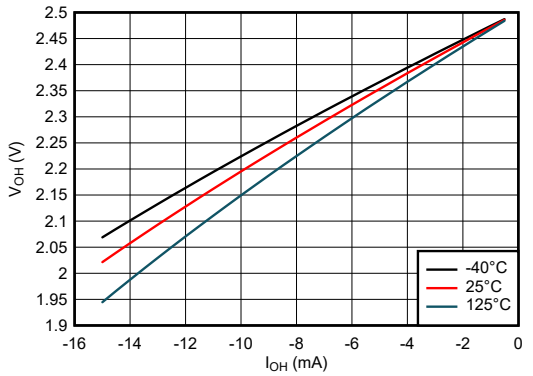



**Figure 6-10. Output Voltage vs Current in HIGH State; 2.5-V Supply**

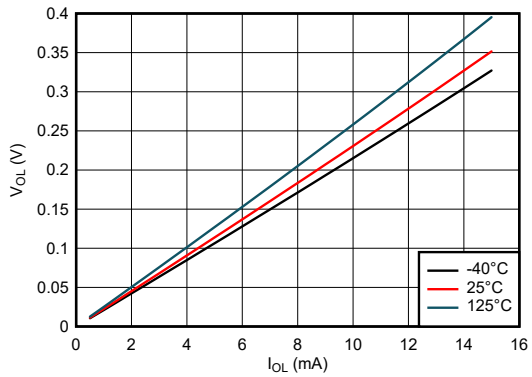



**Figure 6-11. Output Voltage vs Current in LOW State; 2.5-V Supply**

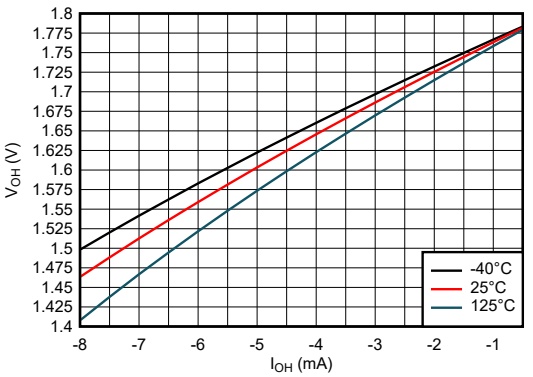



**Figure 6-12. Output Voltage vs Current in HIGH State; 1.8-V Supply**

## 6.15 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

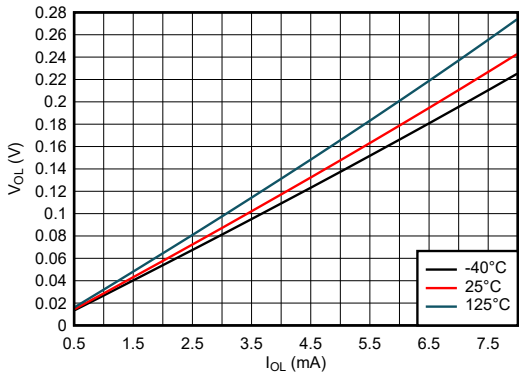


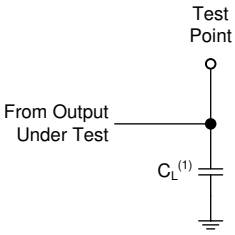

**Figure 6-13. Output Voltage vs Current in LOW State; 1.8-V Supply**

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω.

For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.




(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 7-1. Load Circuit for Push-Pull Outputs**

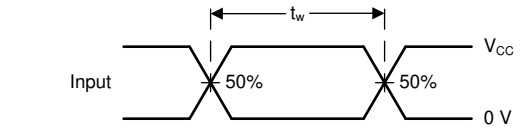



**Figure 7-2. Voltage Waveforms, Pulse Duration**

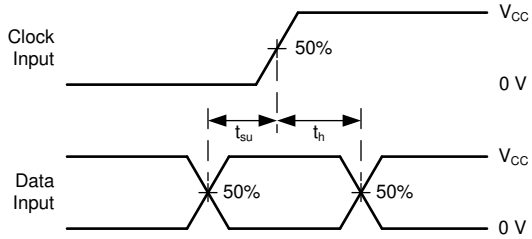
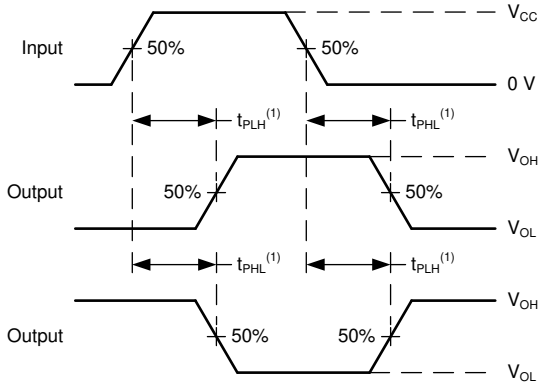
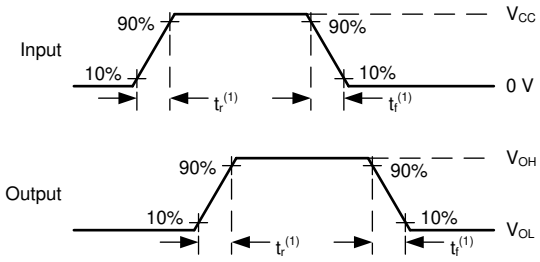



**Figure 7-3. Voltage Waveforms, Setup and Hold Times**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**Figure 7-4. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**Figure 7-5. Voltage Waveforms, Input and Output Transition Times**

# 8 Detailed Description

## 8.1 Overview

Figure 8-1 shows the SN74LV2T74-Q1. As the SN74LV2T74-Q1 is a dual D-Type positive-edge-triggered flip-flop with clear and preset, the following diagram describes one of the two device flip-flops.

## 8.2 Functional Block Diagram

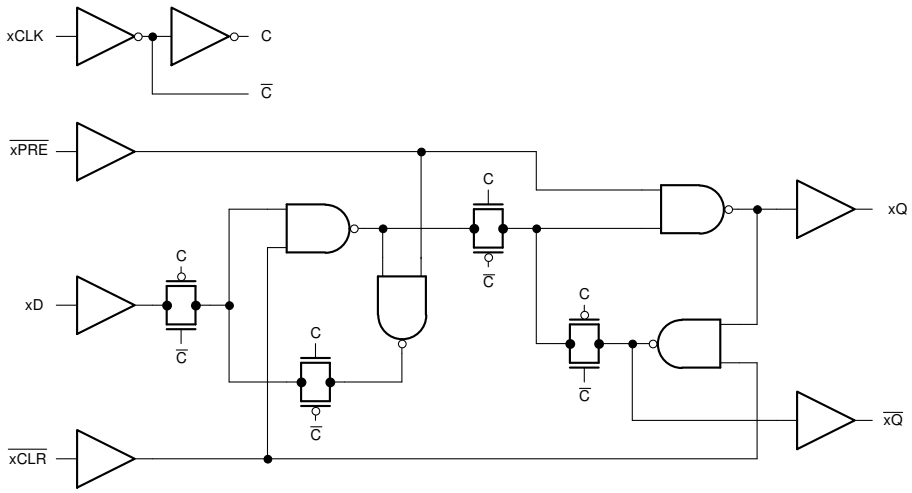



**Figure 8-1. Logic Diagram (Positive Logic) for One Channel of SN74LV2T74-Q1**

## 8.3 Feature Description

### 8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 8.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in Figure 8-2.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

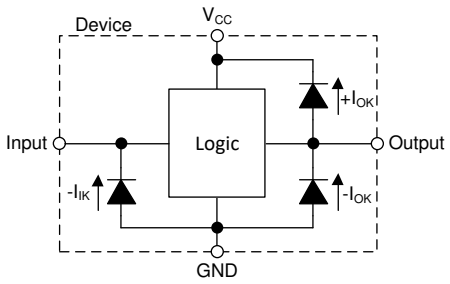



**Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.3 LVxT Enhanced Input Voltage

The SN74LV2T74-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage ($V_{CC}$), as described in the *Electrical Characteristics* table. To ensure proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 8-3 shows the typical $V_{IH}$ and $V_{IL}$ levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

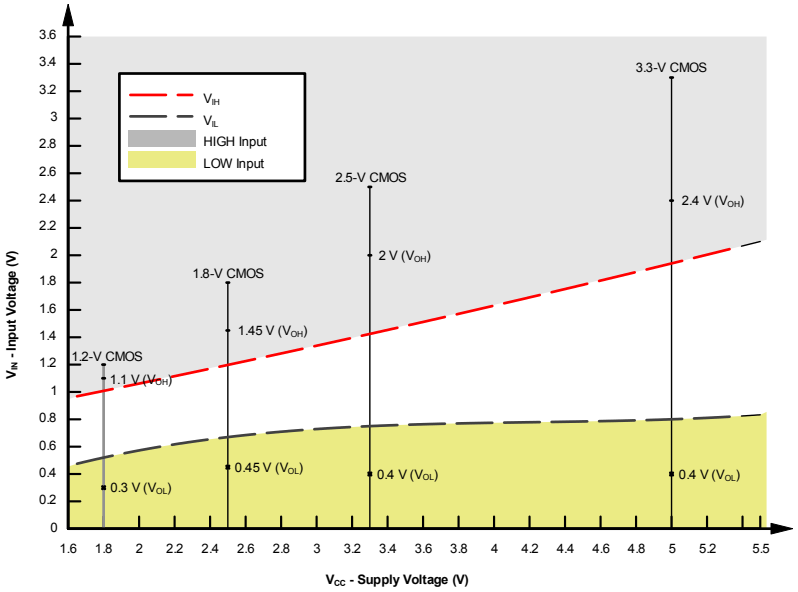



**Figure 8-3. LVxT Input Voltage Levels**

#### 8.3.3.1 Down Translation

Signals can be translated down using the SN74LV2T74-Q1. The voltage applied at the $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state. As shown in Figure 8-3, ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.

As shown in Figure 8-4 for example, the standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V $V_{CC}$.

*Down Translation Combinations* are as follows:

- 1.8-V $V_{CC}$ – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V $V_{CC}$ – Inputs from 3.3 V and 5.0 V
- 3.3-V $V_{CC}$ – Inputs from 5.0 V

#### 8.3.3.2 Up Translation

Input signals can be up translated using the SN74LV2T74-Q1. The voltage applied at $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV2T74-Q1, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in Figure 8-4, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

*Up Translation Combinations* are as follows:

- 1.8-V $V_{CC}$ – Inputs from 1.2 V
- 2.5-V $V_{CC}$ – Inputs from 1.8 V
- 3.3-V $V_{CC}$ – Inputs from 1.8 V and 2.5 V
- 5.0-V $V_{CC}$ – Inputs from 2.5 V and 3.3 V

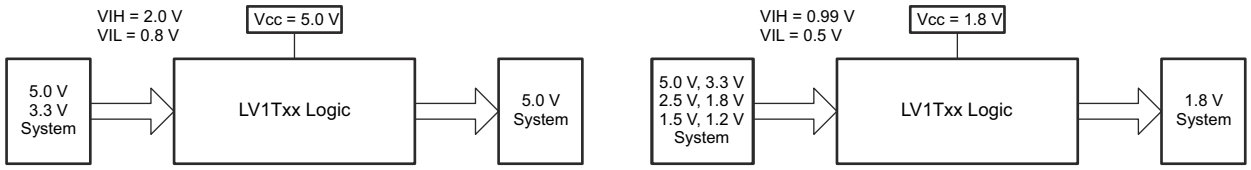



**Figure 8-4. LVxT Up and Down Translation Example**

### 8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

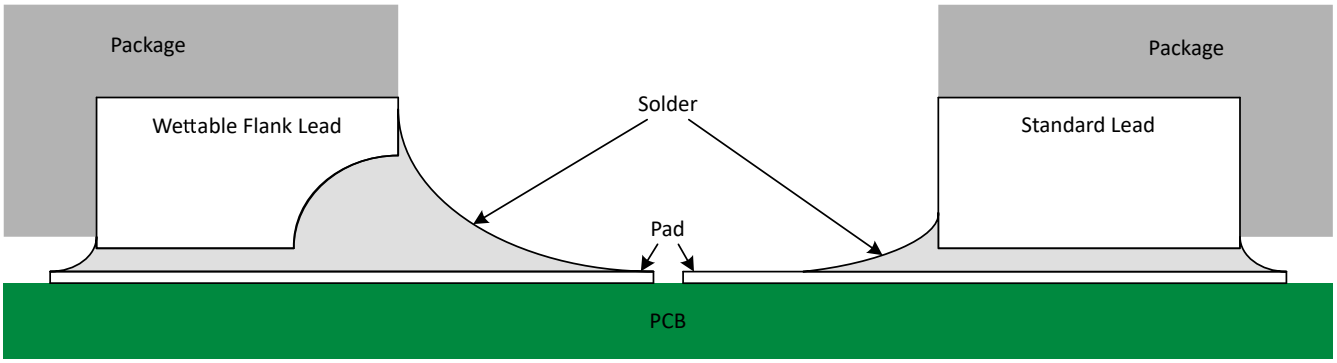



**Figure 8-5. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 8-5, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

## 8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74LV2T74-Q1.

**Table 8-1. Function Table**

| INPUTS | | | | OUTPUTS(1) | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H(1) | H(1) |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. External Schmitt-trigger buffers are used to remove noisy inputs into the (CLK) and (D) inputs.

If the data input (D) of the SN74LV2T74-Q1 is tied to the inverted output ($\overline{Q}$), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and directly connected to the clock input (CLK) to toggle the output.

## 9.2 Typical Application

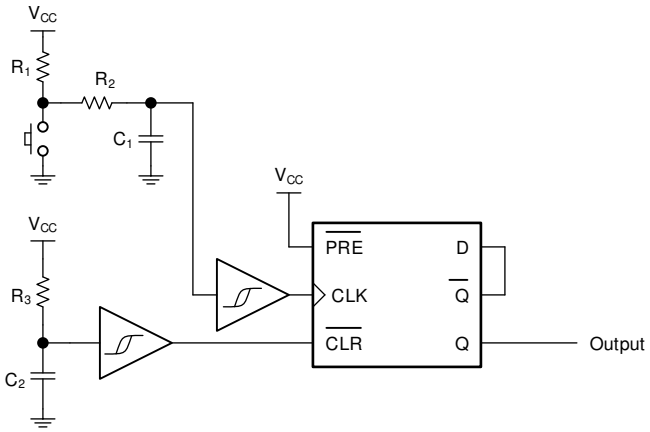



**Figure 9-1. Typical Application Block Diagram**

### 9.2.1 Design Requirements

#### *9.2.1.1 Input Considerations*

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV2T74-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV2T74-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### 9.2.1.2 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV2T74-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 9.2.3 Application Curves

Figure 9-2 shows an example of a single button press bouncing and causing the output to toggle multiple times. This will cause issues in the desired application. Figure 9-3 shows 4 button presses with an added debounce circuit, fixing the unwanted toggling and allowing for proper toggle switch operation.

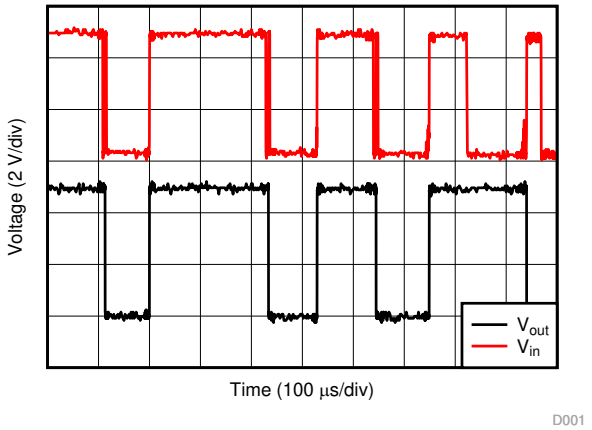



**Figure 9-2. Circuit Response Without RC Debounce**
**$V_{in}$: = CLK Input, $V_{out}$ := Q Output**

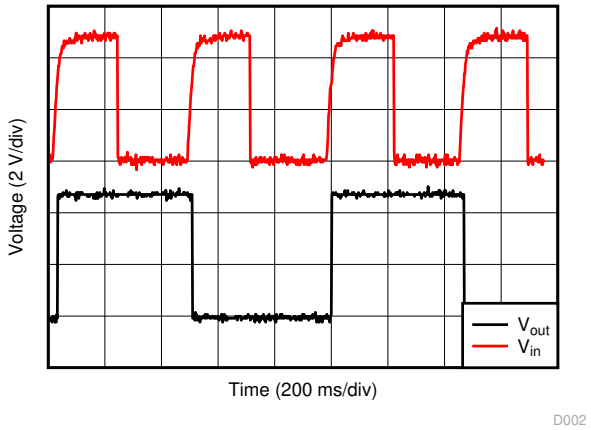



**Figure 9-3. Circuit Response with RC Debounce**
**$V_{in}$: = CLK Input, $V_{out}$ := Q Output**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

# 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV2T74QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVT74Q | Samples |
| SN74LV2T74QWBQARQ1 | ACTIVE | WQFN | BQA | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVT74Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN74LV2T74-Q1 :**

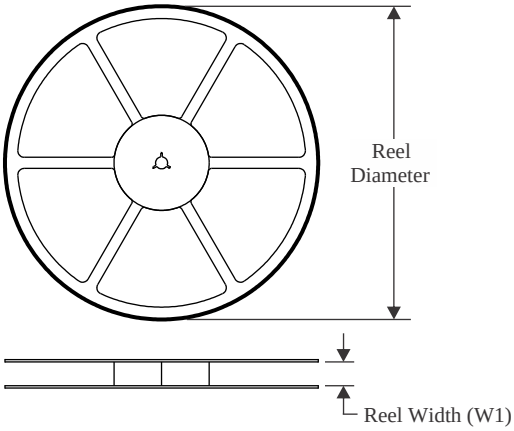
- Catalog : SN74LV2T74

NOTE: Qualified Version Definitions:

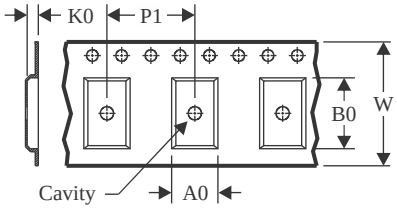
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

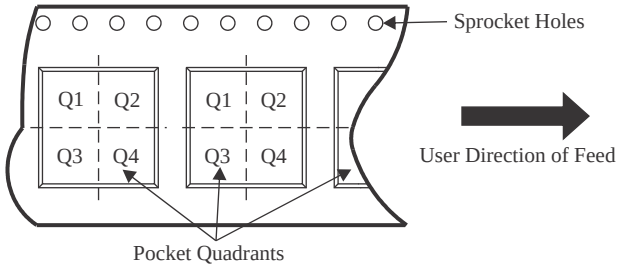



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

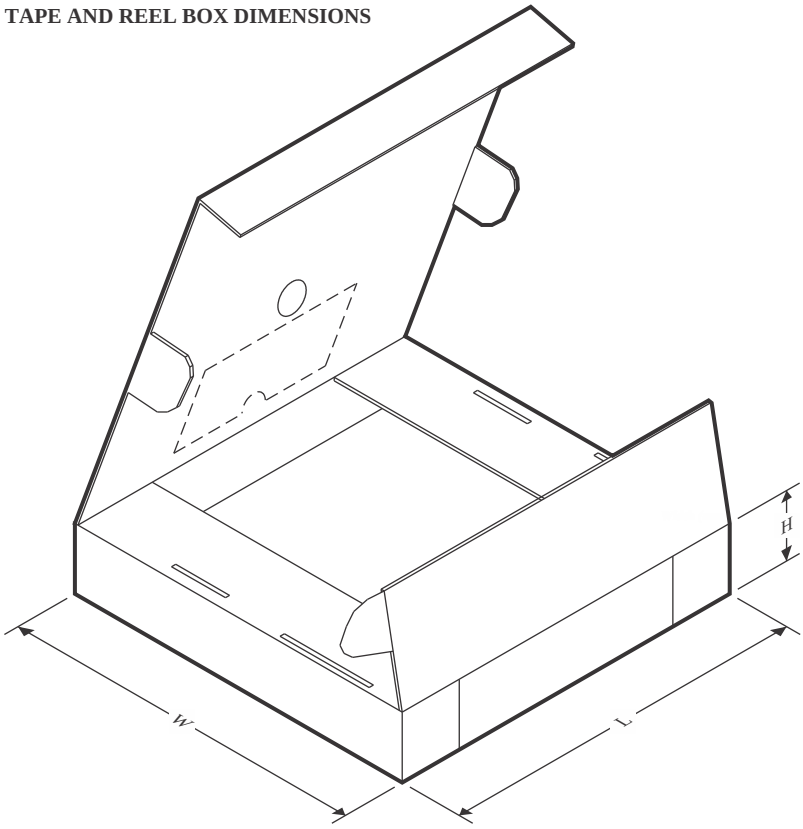
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV2T74QPWRQ1 | TSSOP | PW | 14 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV2T74QWBQARQ1 | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV2T74QPWRQ1 | TSSOP | PW | 14 | 3000 | 356.0 | 356.0 | 35.0 |
| SN74LV2T74QWBQARQ1 | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

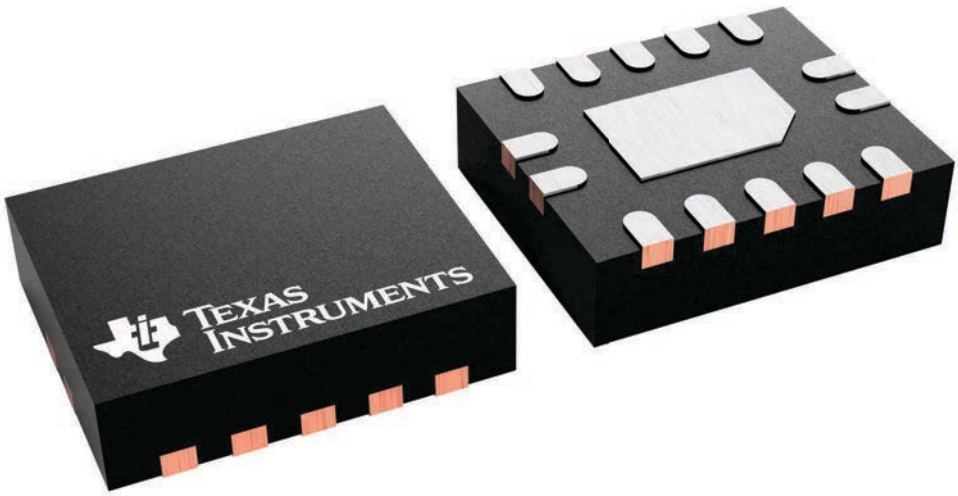
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

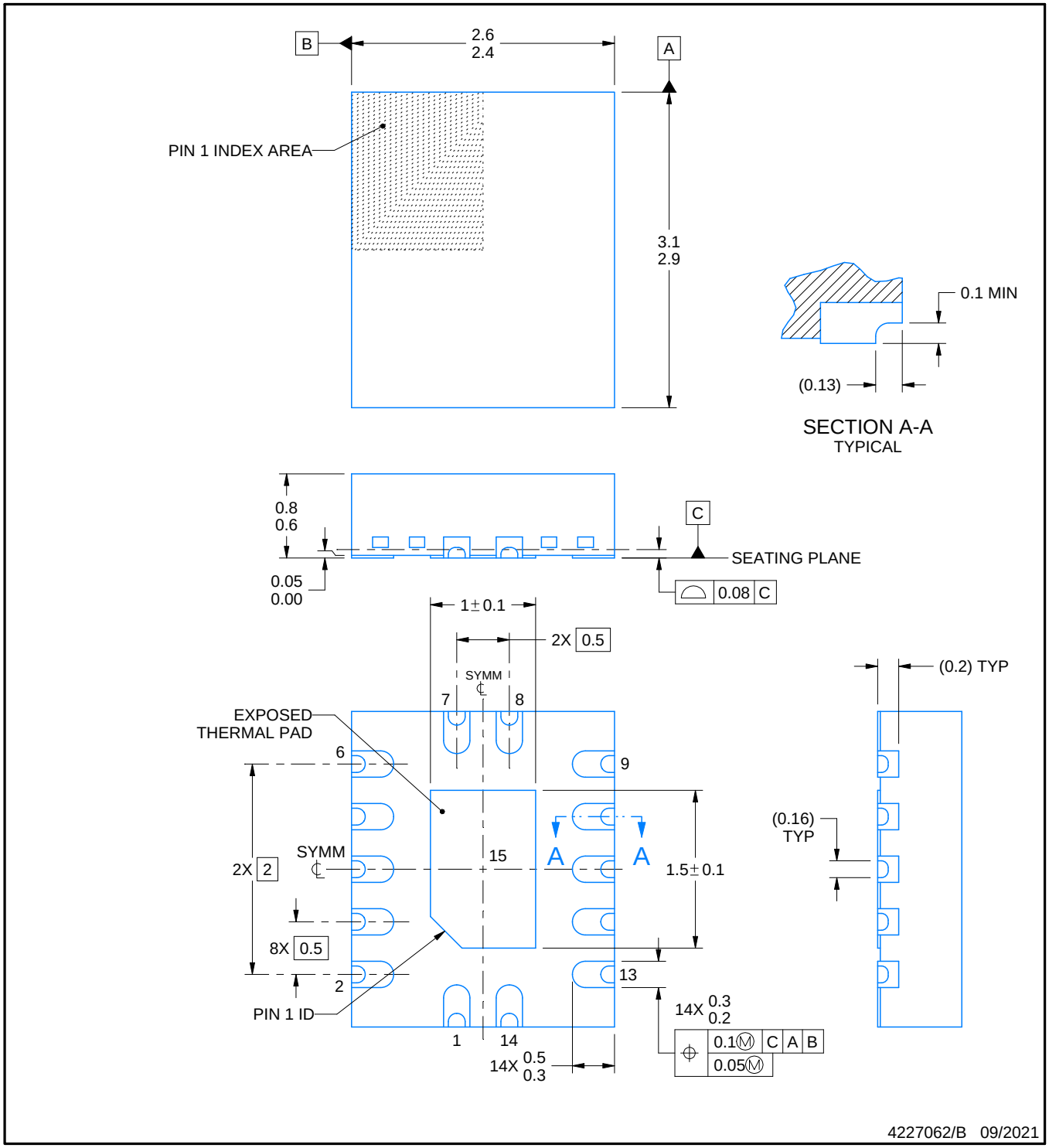


# BQA0014B

# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

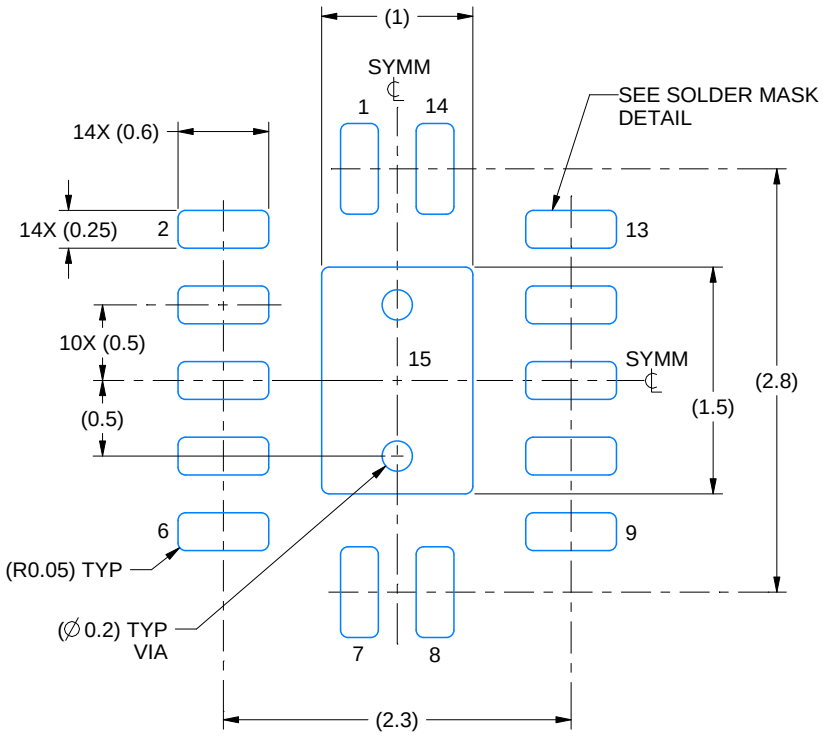
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

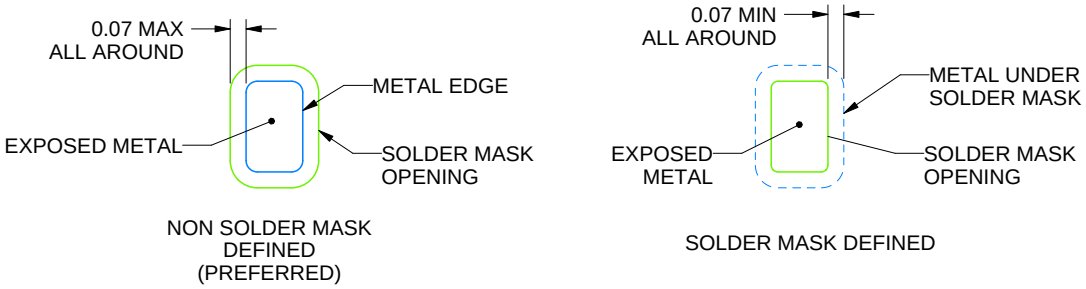
## BQA0014B

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




SOLDER MASK DETAILS

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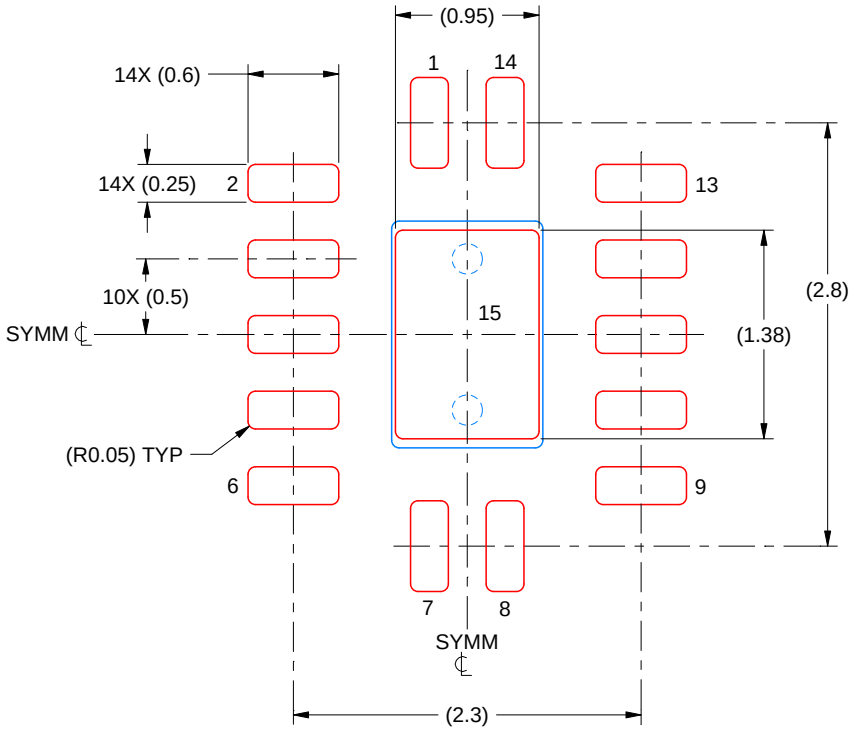
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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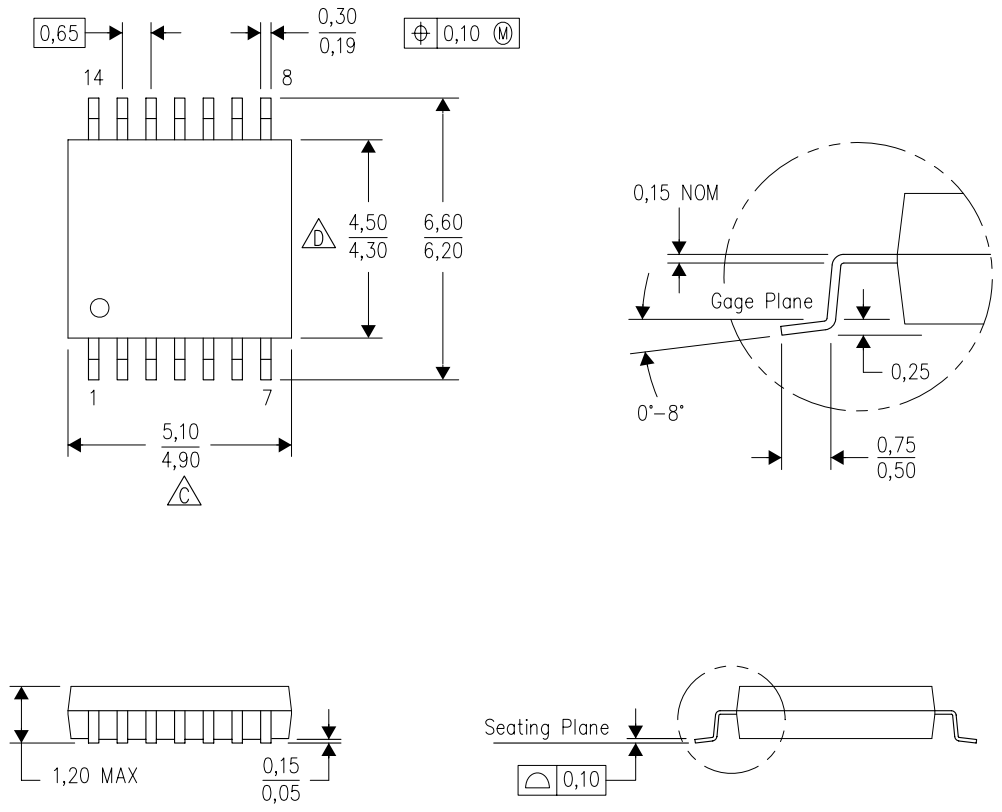
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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