

# NLSF308

## Quad 2-Input AND Gate

The NLSF308 is an advanced high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed:  $t_{PD} = 4.3 \text{ ns}$  (Typ) at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2.0 \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8 \text{ V}$  (Max)
- Function Compatible with Other Standard Logic Families
- QFN-16 Package
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V;  
Machine Model; > 200 V
- Chip Complexity: 24 FETs or 6 Equivalent Gates
- Pb-Free Package is Available\*

**FUNCTION TABLE**

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H



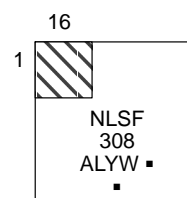
**ON Semiconductor®**

<http://onsemi.com>



**QFN-16  
MN SUFFIX  
CASE 485G**

### MARKING DIAGRAM



NLSF308 = Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NLSF308MNR2	QFN-16	3000 / Tape & Reel
NLSF308MNR2G	QFN-16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLSF308

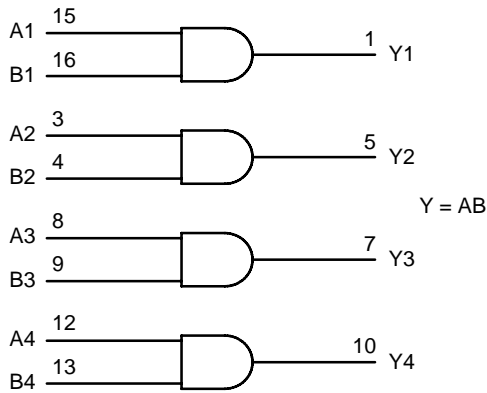


Figure 1. LOGIC DIAGRAM

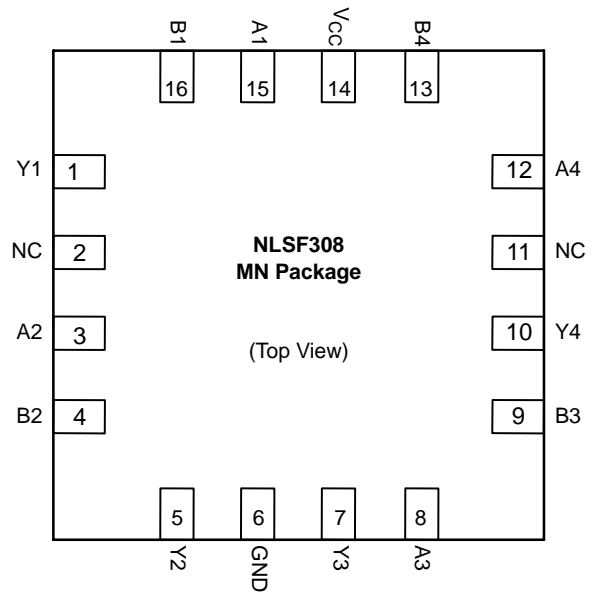


Figure 2. PIN ASSIGNMENT (QFN-16)

## MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	$V_{CC}$	-0.5 to + 7.0	V
DC Input Voltage	$V_{in}$	-0.5 to + 7.0	V
DC Output Voltage	$V_{out}$	-0.5 to $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current, per Pin	$I_{out}$	$\pm 25$	mA
DC Supply Current, $V_{CC}$ and GND Pins	$I_{CC}$	$\pm 50$	mA
Power Dissipation in Still Air	$P_D$	450	mW
Storage Temperature	$T_{stg}$	-65 to + 150	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	$V_{CC}$	2.0	5.5	V
DC Input Voltage	$V_{in}$	0	5.5	V
DC Output Voltage	$V_{out}$	0	$V_{CC}$	V
Operating Temperature	$T_A$	-40	+ 85	$^{\circ}C$
Input Rise and Fall Time	$t_r, t_f$	0	100	ns/V
		0	20	

# NLSF308

## DC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Symbol	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
Minimum High-Level Input Voltage		V <sub>IH</sub>	2.0 3.0 to 5.5	1.50 V <sub>CC</sub> x 0.7			1.50 V <sub>CC</sub> x 0.7		V
Maximum Low-Level Input Voltage		V <sub>IL</sub>	2.0 3.0 to 5.5			0.50 V <sub>CC</sub> x 0.3		0.50 V <sub>CC</sub> x 0.3	V
Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA	V <sub>OH</sub>	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -4 mA, I <sub>OH</sub> = -8 mA		3.0 4.5	2.58 3.94			2.48 3.80		
Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	V <sub>OL</sub>	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA		3.0 4.5			0.36 0.36		0.44 0.44	
Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND		0 to 5.5			± 0.1		± 1.0	μA
Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND		5.5			2.0		20.0	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns)

Parameter	Test Conditions	Symbol	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
Maximum Propagation Delay, A or B to Y	V <sub>CC</sub> = 3.3 ± 0.3 V, C <sub>L</sub> = 15 pF, C <sub>L</sub> = 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>		6.2 8.7	8.8 12.3	1.0 1.0	10.5 14.0	ns
	V <sub>CC</sub> = 5.0 ± 0.5 V, C <sub>L</sub> = 15 pF, C <sub>L</sub> = 50 pF			4.3 5.8	5.9 7.9	1.0 1.0	7.0 9.0	
Maximum Input Capacitance		C <sub>in</sub>		4	10		10	pF
Power Dissipation Capacitance (Note 1)		C <sub>PD</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V					pF
			18					

1. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per gate). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns, C<sub>L</sub> = 50 pF, V<sub>CC</sub> = 5.0 V)

Characteristic	Symbol	T <sub>A</sub> = 25°C		Unit
		Typ	Max	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	0.3	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>		3.5	V
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>		1.5	V

# NLSF308

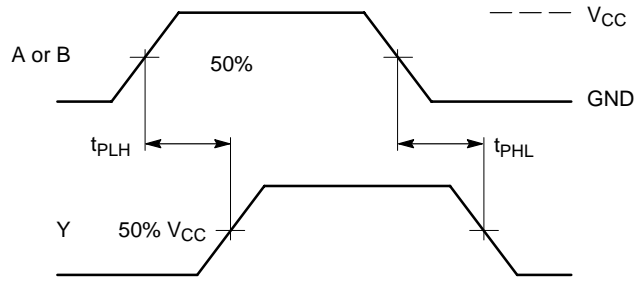
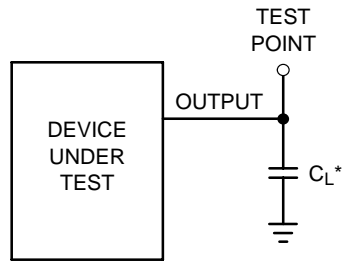


Figure 3. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 4. Test Circuit

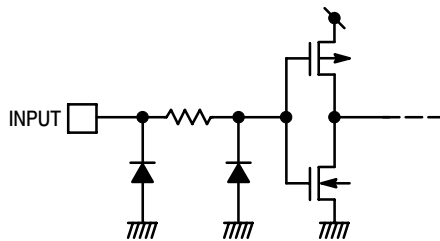


Figure 5. Input Equivalent Circuit

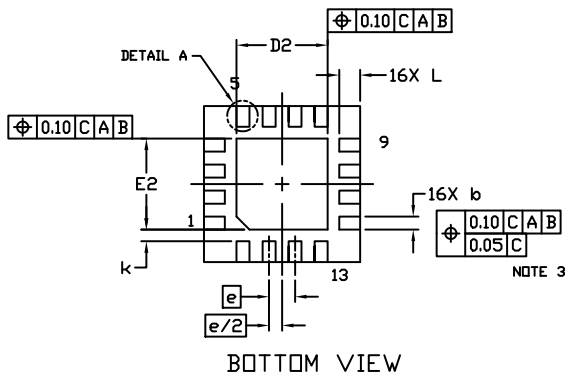
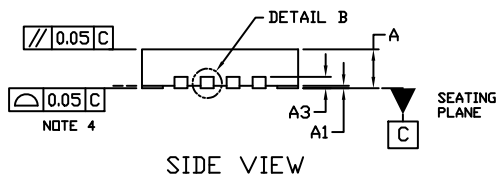
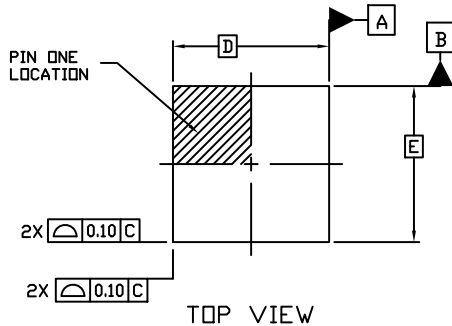
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

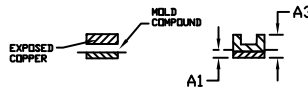
**QFN16 3x3, 0.5P**  
CASE 485G  
ISSUE G

DATE 08 OCT 2021

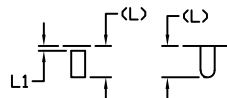


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



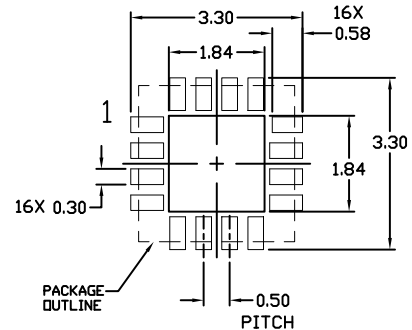
DETAIL B  
ALTERNATE  
CONSTRUCTIONS



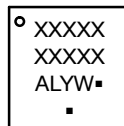
DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
<i>b</i>	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
<i>e</i>	0.50 BSC		
<i>k</i>	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

**MOUNTING FOOTPRINT**



**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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