

FEATURES

- ESD Protection for RS-232 Bus Pins
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC61000-4-2, Contact Discharge
 - ± 15 -kV IEC61000-4-2, Air-Gap Discharge
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 500 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s) for TRSF3223E

APPLICATIONS

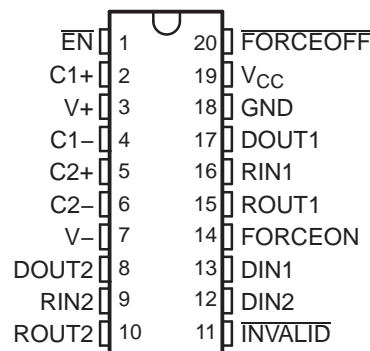
- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

DESCRIPTION/ ORDERING INFORMATION

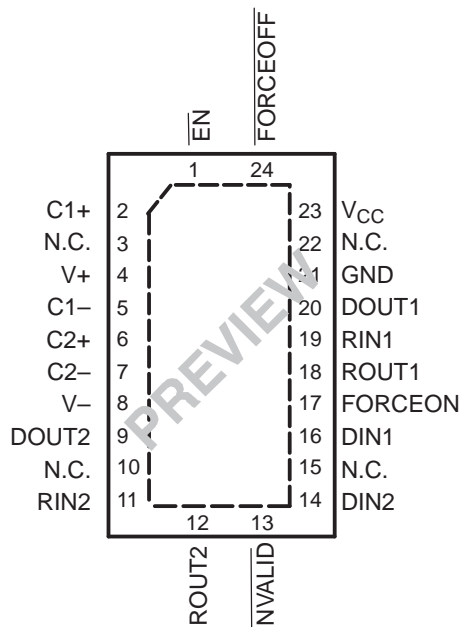
The TRS3223E consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at typical data signaling rates up to 500 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when $\overline{\text{FORCEON}}$ is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low and EN is high, both drivers and receivers are shut off, and the supply current is reduced to 1 mA. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 4 for receiver input levels.

DB, DW, OR PW PACKAGE
(TOP VIEW)



RHL PACKAGE
(TOP VIEW)



N.C. – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TRS3223E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ±15-kV ESD PROTECTION

SLLS794–JUNE 2007

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN – RHL	Reel of 2000	TRS3223ECRHLR	PREVIEW
	SOIC – DW	Tube of 25	TRS3223ECDW	TRS3223EC
		Reel of 2000	TRS3223ECDWR	
	SSOP – DB	Tube of 70	TRS3223ECDB	RS23EC
		Reel of 2000	TRS3223ECDBR	
	TSSOP – PW	Tube of 70	TRS3223ECPW	RS23EC
		Reel of 2000	TRS3223ECPWR	
	–40°C to 85°C	QFN – RHL	Reel of 2000	TRS3223EIRHLR
SOIC – DW		Tube of 25	TRS3223EIDW	TRS3223EI
		Reel of 2000	TRS3223EIDWR	
SSOP – DB		Tube of 70	TRS3223EIDB	RS23EI
		Reel of 2000	TRS3223EIDBR	
TSSOP – PW		Tube of 70	TRS3223EIPW	RS23EI
		Reel of 2000	TRS3223EIPWR	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

EACH DRIVER⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

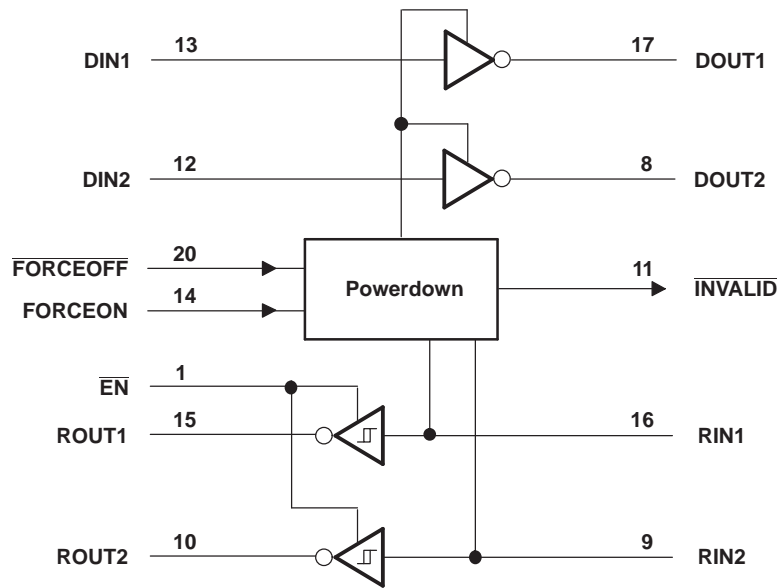
- (1) H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER⁽¹⁾

INPUTS			OUTPUT DOUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

- (1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers are for the DB, DW, and PW packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.3	6	V
V+	Positive-output supply voltage range ⁽²⁾	-0.3	7	V
V-	Negative-output supply voltage range ⁽²⁾	0.3	-7	V
V+ - V-	Supply voltage difference ⁽²⁾		13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)		V
		Receiver		
V _O	Output voltage range	Driver		V
		Receiver (INVALID)		
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DB package		°C/W
		DW package		
		PW package		
		RHL package		
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

TRS3223E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ±15-kV ESD PROTECTION

SLLS794–JUNE 2007

Recommended Operating Conditions⁽¹⁾

See [Figure 6](#)

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, \overline{EN} , $\overline{FORCEOFF}$, FORCEON	$V_{CC} = 3.3\text{ V}$	2		V
			$V_{CC} = 5\text{ V}$	2.4		
V_{IL}	Driver and control low-level input voltage	DIN, \overline{EN} , $\overline{FORCEOFF}$, FORCEON			0.8	V
V_I	Driver and control input voltage	DIN, \overline{EN} , $\overline{FORCEOFF}$, FORCEON	0	5.5		V
	Receiver input voltage		-25	25		V
T_A	Operating free-air temperature	TRS3223EC	0	70		°C
		TRS3223EI	-40	85		

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
I_I	Input leakage current	\overline{EN} , $\overline{FORCEOFF}$, FORCEON		±0.01	±1	μA	
I_{CC}	Supply current	Auto-powerdown disabled	$V_{CC} = 3.3\text{ V}$ or 5 V , $T_A = 25^\circ\text{C}$, No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	μA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10	

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOOUT at R _L = 3 k Ω to GND	5	5.4		V
V _{OL}	Low-level output voltage	DOOUT at R _L = 3 k Ω to GND	–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}		± 0.01	± 1	μ A
I _{IL}	Low-level input current	V _I at GND		± 0.01	± 1	μ A
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V		± 35	± 60	mA
		V _{CC} = 5.5 V, V _O = 0 V				
r _o	Output resistance	V _{CC} , V ₊ , and V _– = 0 V, V _O = ± 2 V	300	10M		Ω
I _{OZ}	Output leakage current	FORCEOFF = GND, V _{CC} = 3 V to 3.6 V, V _O = ± 12 V			± 25	μ A
		FORCEOFF = GND, V _{CC} = 4.5 V to 5.5 V, V _O = ± 12 V			± 25	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	C _L = 1000 pF, One DOOUT switching,	R _L = 3 k Ω , See Figure 1	250	500		kbit/s
t _{sk(p)}	Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, See Figure 2	R _L = 3 k Ω to 7 k Ω ,		100		ns
SR(tr)	Slew rate, transition region (See Figure 1)	R _L = 3 k Ω to 7 k Ω , V _{CC} = 3.3 V	C _L = 150 pF to 1000 pF	6		30	V/ μ s
			C _L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

TRS3223E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
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SLLS794–JUNE 2007

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.6	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{OZ}	Output leakage current	$\overline{EN} = V_{CC}$		± 0.05		μ A
r _i	Input resistance	V _I = ± 3 V to ± 25 V	3	5		k Ω

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	150	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 3	150	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4	200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4	200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{T+}(\text{valid})$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND,	$\overline{\text{FORCEOFF}} = V_{CC}$		2.7	V
$V_{T(\text{valid})}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND,	$\overline{\text{FORCEOFF}} = V_{CC}$	-2.7		V
$V_{T(\text{invalid})}$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND,	$\overline{\text{FORCEOFF}} = V_{CC}$	-0.3	0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	$I_{OH} = 1 \text{ mA}$, $\overline{\text{FORCEOFF}} = V_{CC}$	FORCEON = GND,	$V_{CC} - 0.6$		V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	$I_{OL} = 1.6 \text{ mA}$, $\overline{\text{FORCEOFF}} = V_{CC}$	FORCEON = GND,		0.4	V

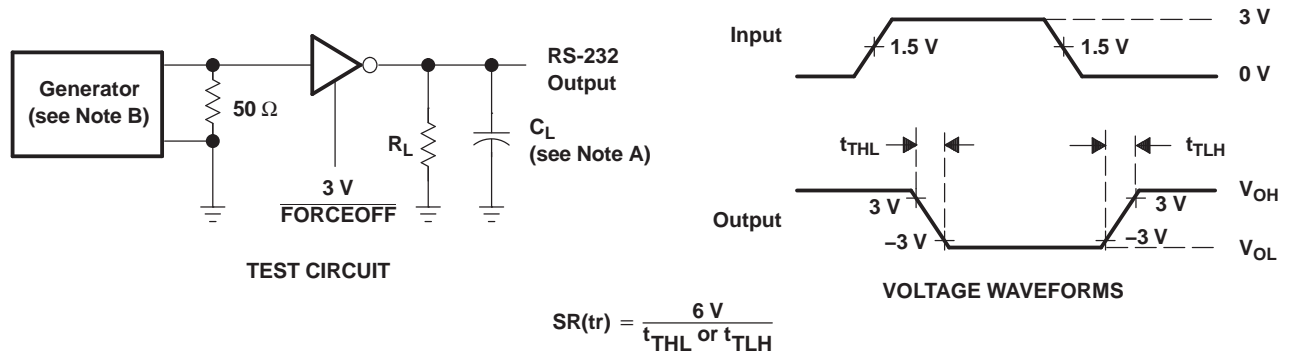
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
t_{invalid}	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

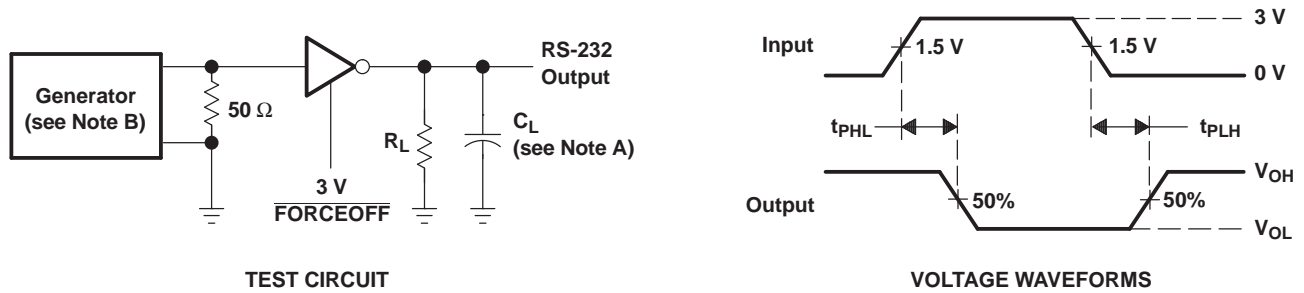
(1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



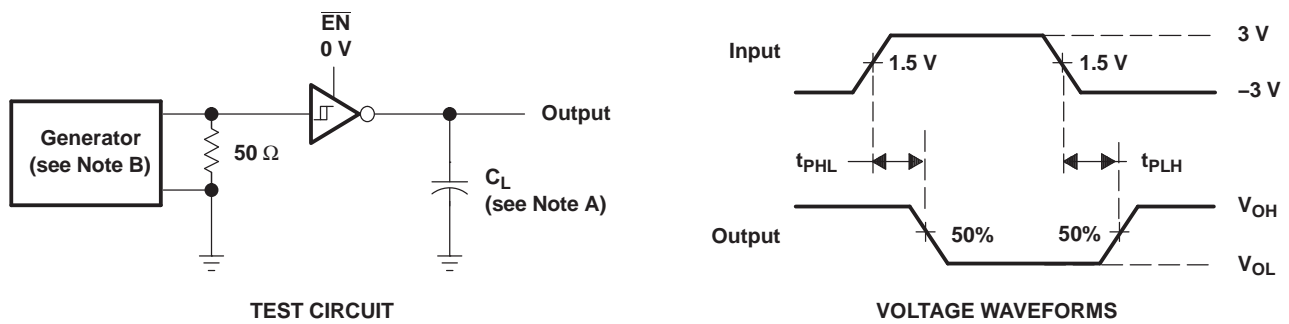
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

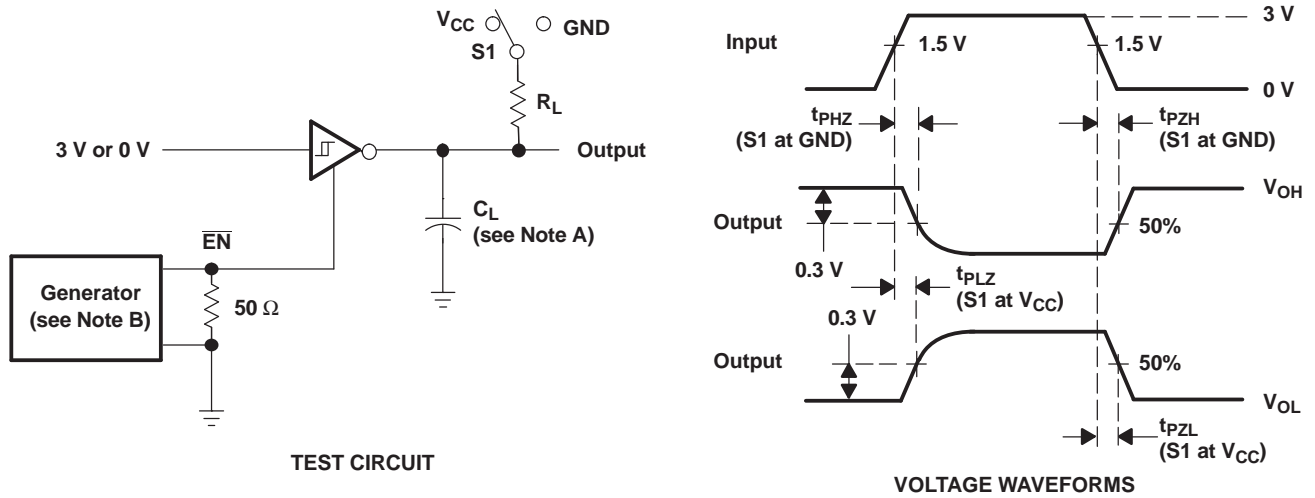
Figure 2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

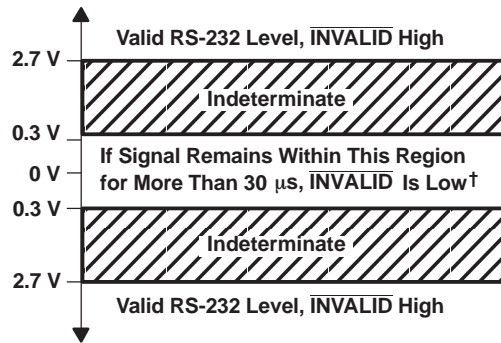
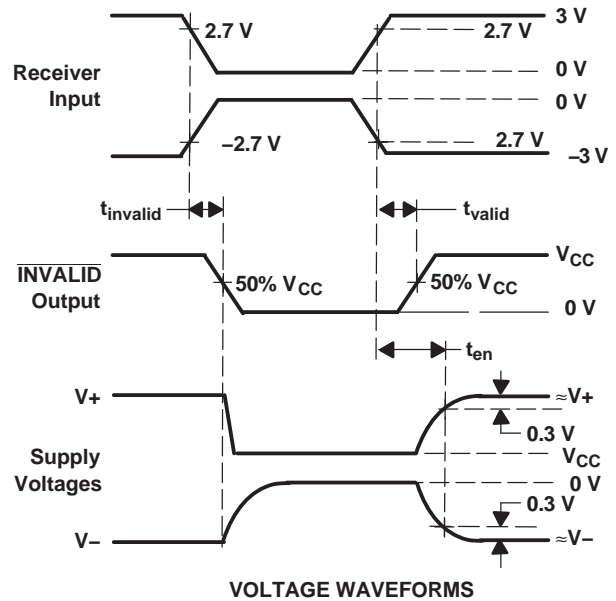
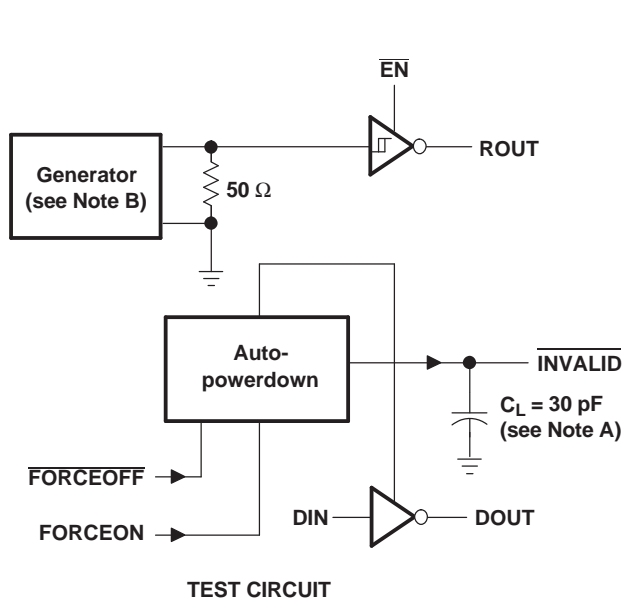
PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION (continued)

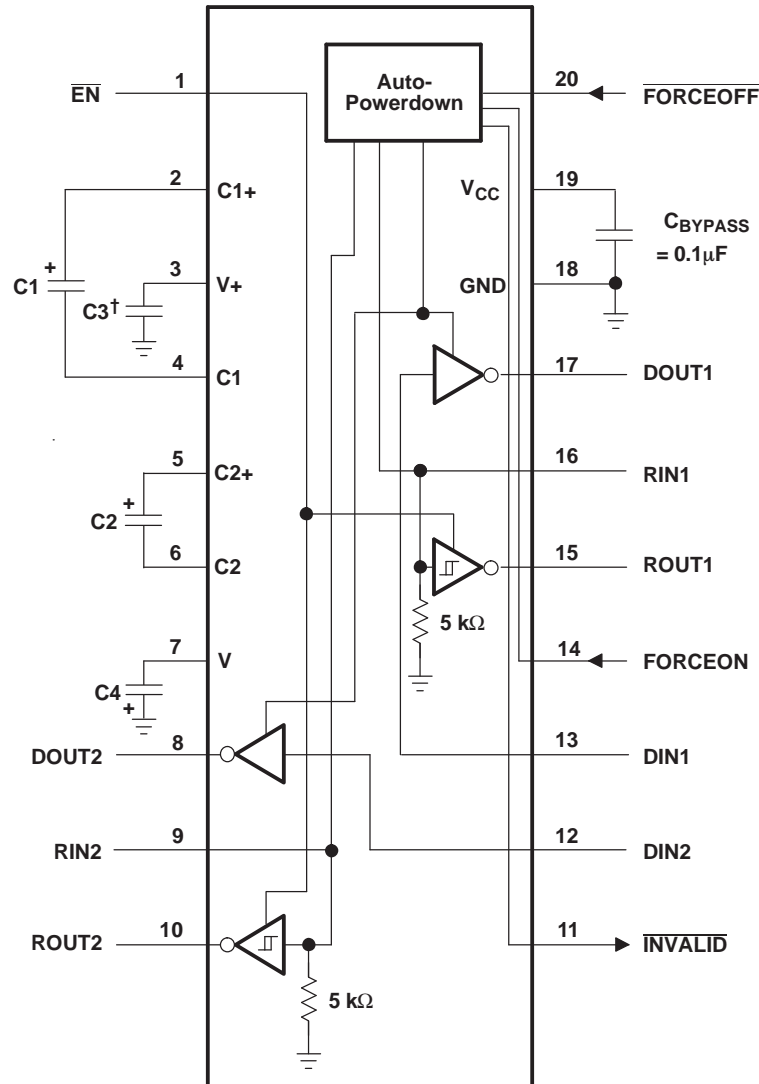


† Auto-powerdown disables drivers and reduces supply current to 1 μ A

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3223ECDBR	LIFEBUY	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS23EC	
TRS3223ECDWR	LIFEBUY	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3223EC	
TRS3223ECPW	LIFEBUY	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS23EC	
TRS3223ECPWR	LIFEBUY	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS23EC	
TRS3223EIDB	LIFEBUY	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS23EI	
TRS3223EIDBR	LIFEBUY	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS23EI	
TRS3223EIPW	LIFEBUY	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS23EI	
TRS3223EIPWR	LIFEBUY	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS23EI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3223ECDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRS3223ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRS3223ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TRS3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRS3223EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3223ECDBR	SSOP	DB	20	2000	356.0	356.0	35.0
TRS3223ECDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TRS3223ECPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
TRS3223EIDBR	SSOP	DB	20	2000	356.0	356.0	35.0
TRS3223EIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TRS3223ECPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TRS3223EIDB	DB	SSOP	20	70	530	10.5	4000	4.1
TRS3223EIPW	PW	TSSOP	20	70	530	10.2	3600	3.5

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

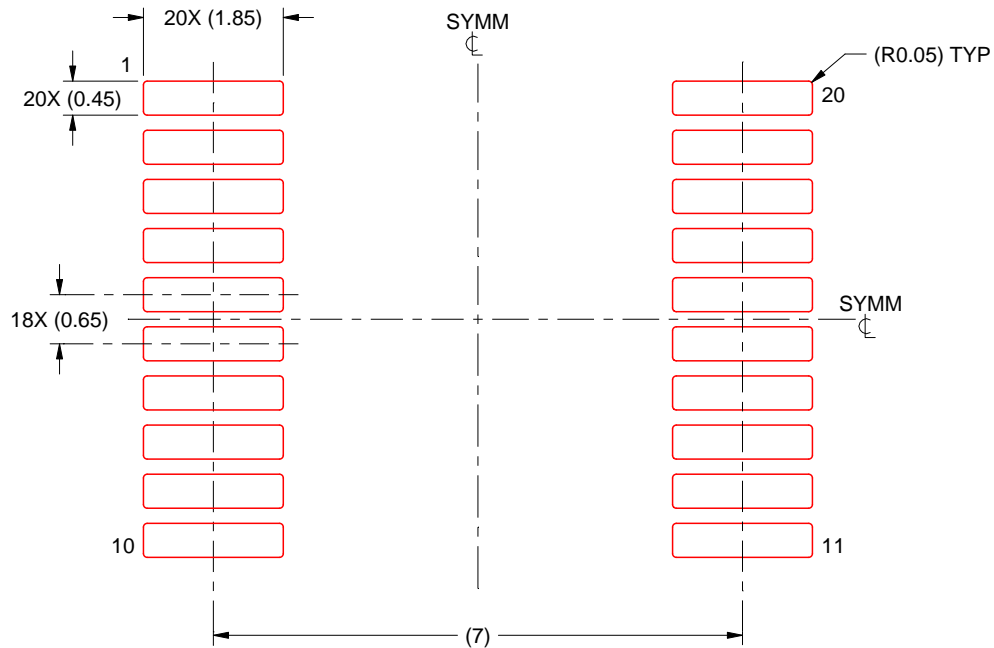
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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