CS5351

108 dB, 192 kHz, Multi-bit Audio A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-bit Conversion
- 108 dB Dynamic Range
- -98 dB THD+N
- System Sampling Rates up to 192 kHz
- 135 mW Power Consumption
- High-Pass Filter and DC Offset Calibration
- Supports Logic Levels Between 5 and 2.5 V
- Single-Ended Analog Inputs
- Overflow Detection
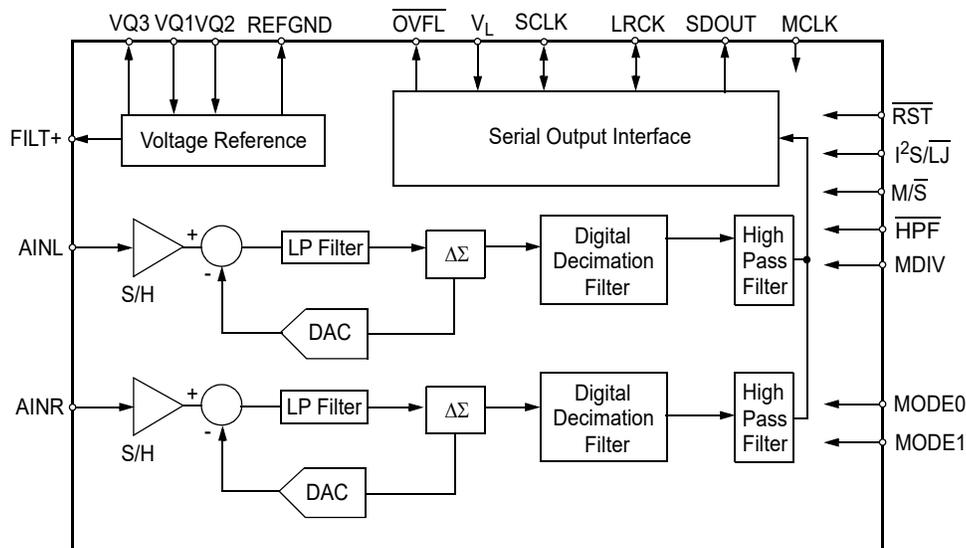- Pin Compatible with the CS5361

General Description

The CS5351 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, and anti-alias filtering. The device generates 24-bit values for both left and right inputs in serial form at sample rates up to 192 kHz per channel.

The CS5351 uses a 5th-order, multi-bit, delta-sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5351 is ideal for audio systems requiring wide dynamic range, negligible distortion, and low noise. Such applications include A/V receivers, DVD-R, CD-R, digital mixing consoles, and effects processors.

ORDERING INFORMATION

CS5351K-KZZ, Lead Free   -10° to 70°C   24-pin TSSOP
CS5351K-KZZR, Lead Free -10° to 70°C   24-pin TSSOP
CS5351K-DZZ, Lead Free   -40° to 85°C   24-pin TSSOP
CS5351K-DZZR, Lead Free -40° to 85°C   24-pin TSSOP
CDB5351   Evaluation Board

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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies: Positive Analog		VA	4.75	5.0	5.25	V
Positive Digital		VD	3.1	3.3	5.25	V
Positive Logic		VL	2.37	3.3	5.25	V
Ambient Operating Temperature Commercial (-KSZ/-KZZ)		T_{AC}	-10	-	70	°C
Automotive (-DZZ)		T_{AI}	-40	-	85	°C

ABSOLUTE MAXIMUM RATINGS (GND = 0 V, All voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Max	Units
DC Power Supplies: Analog		VA	-0.3	+6.0	V
Logic		VL	-0.3	+6.0	V
Digital		VD	-0.3	+6.0	V
Input Current	(Note 2)	I_{in}	-10	+10	mA
Analog Input Voltage	(Note 3)	V_{IN}	GND - 0.7	VA + 0.7	V
Digital Input Voltage	(Note 3)	V_{IND}	-0.7	VL + 0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

3. The maximum over/under voltage is limited by the input current.

ANALOG CHARACTERISTICS (CS5351-KSZ/KZZ) (Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.)

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode	**Fs = 48 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
Total Harmonic Distortion + Noise	(Note 4)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-84	-	dB
	-60 dB		-	-44	-	dB
Double-Speed Mode	**Fs = 96 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
40 kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 4)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-84	-	dB
	-60 dB		-	-44	-	dB
40 kHz bandwidth	-1 dB		-	-95	-	dB
Quad-Speed Mode	**Fs = 192 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
40 kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 4)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-84	-	dB
	-60 dB		-	-44	-	dB
40 kHz bandwidth	-1 dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	95	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-2	-	2	%
Gain Drift			-100	-	100	ppm/°C
Offset Error	HPF enabled		-	-	0	LSB
	HPF disabled		-	-	100	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.55*VA	0.56*VA	.57*VA	Vpp
Input Impedance			7.5	-	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

Notes: 4. Referred to the typical full-scale input voltage.

ANALOG CHARACTERISTICS (CS5351-DZZ) (Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.)

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode	**Fs = 48 kHz**					
Dynamic Range	A-weighted		100	108	-	dB
	unweighted		97	105	-	dB
Total Harmonic Distortion + Noise	(Note 4)	THD+N				
	-1 dB		-	-98	-90	dB
	-20 dB		-	-84	-	dB
	-60 dB		-	-44	-	dB
Double-Speed Mode	**Fs = 96 kHz**					
Dynamic Range	A-weighted		100	108	-	dB
	unweighted		97	105	-	dB
	40 kHz bandwidth unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 4)	THD+N				
	-1 dB		-	-98	-90	dB
	-20 dB		-	-84	-	dB
	-60 dB		-	-44	-	dB
40 kHz bandwidth	-1 dB		-	-95	-	dB
Quad-Speed Mode	**Fs = 192 kHz**					
Dynamic Range	A-weighted		100	108	-	dB
	unweighted		97	105	-	dB
	40 kHz bandwidth unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 4)	THD+N				
	-1 dB		-	-98	-90	dB
	-20 dB		-	-84	-	dB
	-60 dB		-	-44	-	dB
40 kHz bandwidth	-1 dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	95	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	5	%
Gain Drift			-100	-	100	ppm/°C
Offset Error	HPF enabled		-	-	0	LSB
	HPF disabled		-	-	100	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.53*VA	0.56*VA	0.59*VA	Vpp
Input Impedance			7.5	-	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

DIGITAL FILTER CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode (2 kHz to 51 kHz sample rates)						
Passband (-0.1 dB) (Note 5)			0	-	0.47	Fs
Passband Ripple			-0.1	-	0.035	dB
Stopband (Note 5)			0.58	-	-	Fs
Stopband Attenuation			-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		t_{gd}	-	12/Fs	-	s
Interchannel Phase Deviation			-	0.0001	-	Deg
Double-Speed Mode (50 kHz to 102 kHz sample rates)						
Passband (-0.1 dB) (Note 5)			0	-	0.45	Fs
Passband Ripple			-0.1	-	0.035	dB
Stopband (Note 5)			0.68	-	-	Fs
Stopband Attenuation			-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		t_{gd}	-	9/Fs	-	s
Interchannel Phase Deviation			-	0.0001	-	Deg
Quad-Speed Mode (100 kHz to 204 kHz sample rates)						
Passband (-0.1 dB) (Note 5)			0	-	0.24	Fs
Passband Ripple			-0.1	-	0.035	dB
Stopband (Note 5)			0.78	-	-	Fs
Stopband Attenuation			-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)		t_{gd}	-	5/Fs	-	s
Interchannel Phase Deviation			-	0.0001	-	Deg
High-Pass Filter Characteristics						
Frequency Response -3.0 dB			-	1	-	Hz
-0.13 dB (Note 6)				20	-	Hz
Phase Deviation @ 20 Hz (Note 6)			-	10	-	Deg
Passband Ripple			-	-	0	dB
Filter Settling Time				10^5/Fs		s

Notes: 5. The filter frequency response scales precisely with Fs.

6. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.
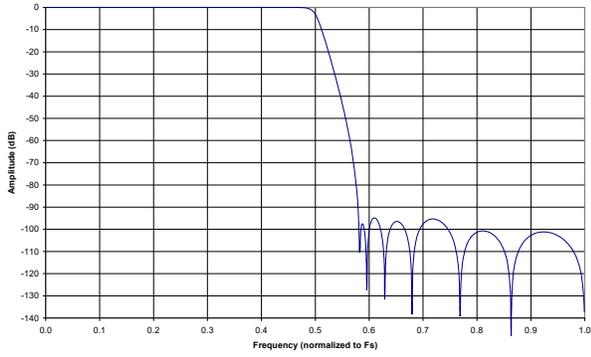
Figure 1. Single-Speed Mode Stopband Rejection
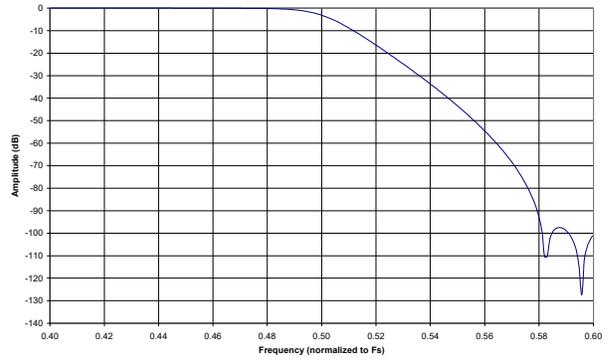
Figure 2. Single-Speed Mode Transition Band
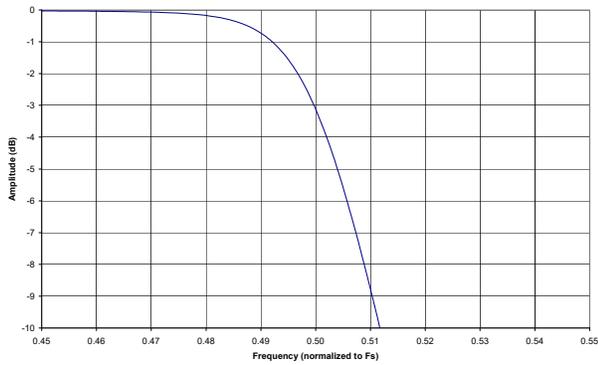
Figure 3. Single-Speed Mode Transition Band (Detail)
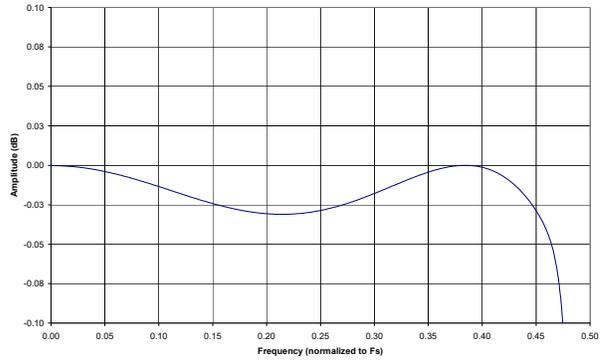
Figure 4. Single-Speed Mode Passband Ripple
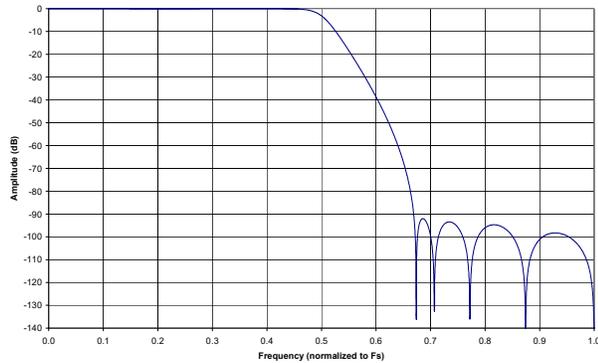
Figure 5. Double-Speed Mode Stopband Rejection
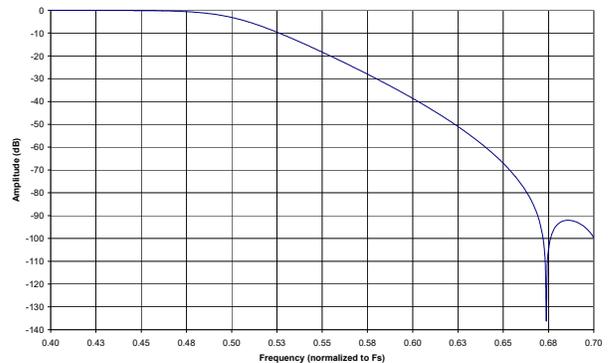
Figure 6. Double-Speed Mode Transition Band
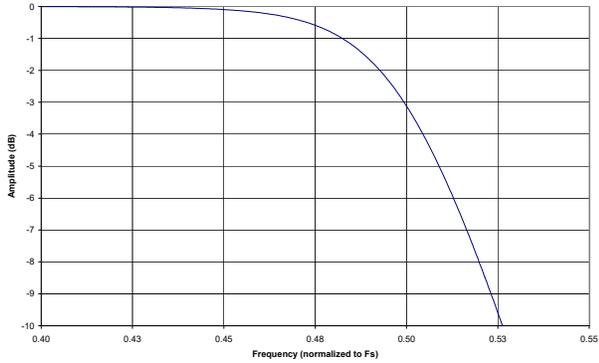
Figure 7. Double-Speed Mode Transition Band (Detail)
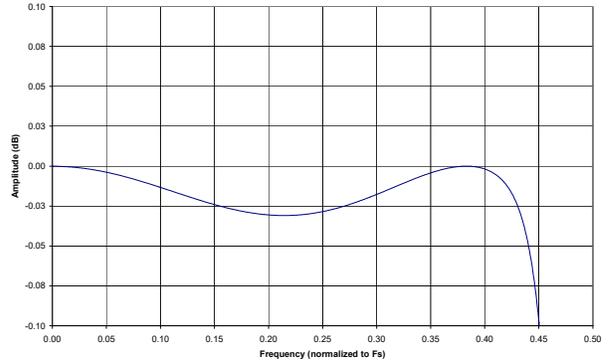
Figure 8. Double-Speed Mode Passband Ripple
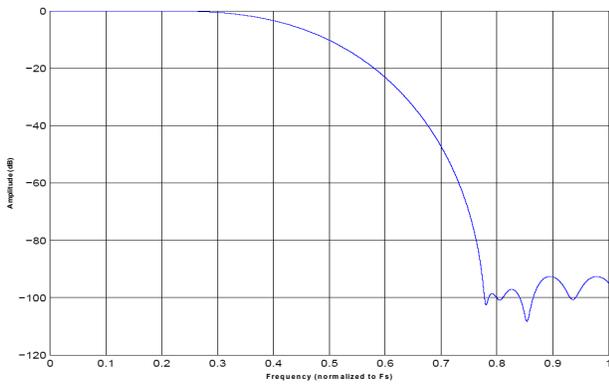
Figure 9. Quad-Speed Mode Stopband Rejection
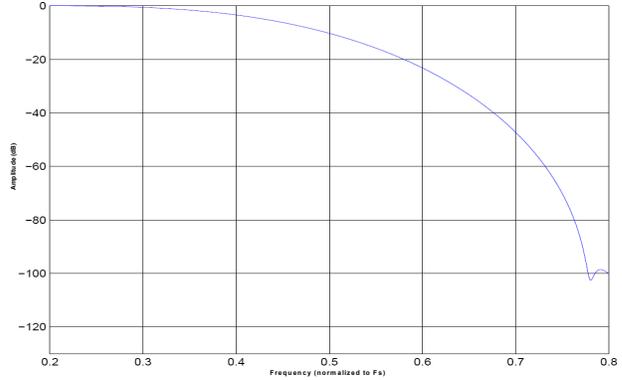
Figure 10. Quad-Speed Mode Transition Band
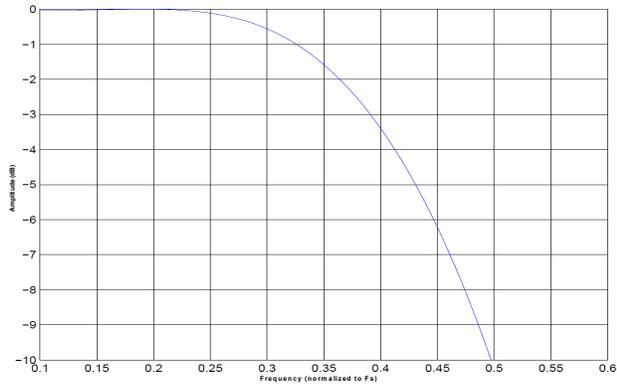
Figure 11. Quad-Speed Mode Transition Band (Detail)
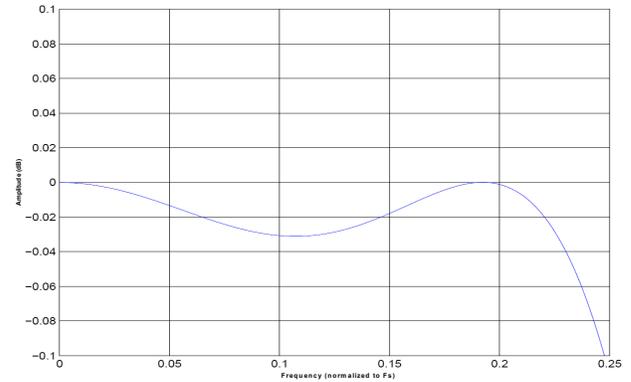
Figure 12. Quad-Speed Mode Passband Ripple

DC ELECTRICAL CHARACTERISTICS (GND = 0 V, all voltages with respect to ground.

MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	17.5	21.5	mA
(Normal Operation)	VL,VD = 5 V	I_D	-	22	27.5	mA
	VL,VD = 3.3 V	I_D	-	14.5	17	mA
Power Supply Current	VA = 5 V	I_A	-	100	-	µA
(Power-Down Mode) (Note 7)	VL,VD = 5 V	I_D	-	100	-	µA
Power Consumption						
(Normal Operation)	VA, VD, VL = 5 V	-	-	198	243	mW
	VA = 5 V, VL, VD = 3.3 V	-	-	135	161	mW
	(Power-Down Mode)	-	-	1	-	mW
Power Supply Rejection Ratio (1 kHz) (Note 8)		PSRR	-	65	-	dB
V_Q Nominal Voltage			-	2.5	-	V
Output Impedance			-	25	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	5	-	V
Output Impedance			-	15	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

Notes: 7. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

8. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 100 µA	(% of VL)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_o = 100 µA	(% of VL)	V_{OL}	-	-	15%	V
$\overline{OVFL}$ Current Sink		I_{ovfl}	-	-	4.0	mA
Input Leakage Current (all pins except SCLK and LRCK)		I_{in}	-10	-	10	µA
Input Leakage Current (SCLK and LRCK)		I_{in}	-25	-	25	µA

THERMAL CHARACTERISTICS

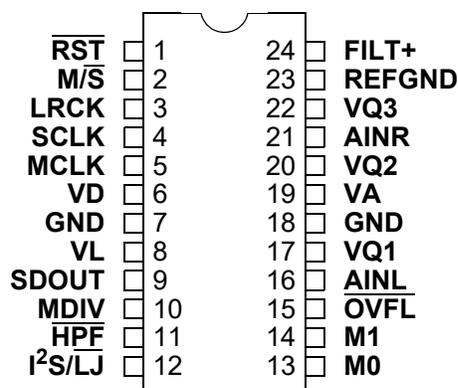| Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Junction to Ambient Thermal Impedance					
(Multi-layer PCB) TSSOP	θ_{JA-TM}	-	70	-	°C/W
(Multi-layer PCB) SOIC	θ_{JA-SM}	-	60	-	°C/W
(Single-layer PCB) TSSOP	θ_{JA-TS}	-	105	-	°C/W
(Single-layer PCB) SOIC	θ_{JA-SS}	-	80	-	°C/W

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (Logic "0" = GND = 0 V;

Logic "1" = VL, C_L = 20 pF)

| Parameter		Symbol	Min	Typ	Max	Unit
Output Sample Rate	Single-Speed Mode	Fs	2	-	51	kHz
	Double-Speed Mode	Fs	50	-	102	kHz
	Quad-Speed Mode	Fs	100	-	204	kHz
$\overline{OVFL}$ to LRCK edge setup time		t_{setup}	$16/f_{sclk}$	-	-	s
$\overline{OVFL}$ to LRCK edge hold time		t_{hold}	$1/f_{sclk}$	-	-	s
$\overline{OVFL}$ time-out on overrange condition						
	Fs = 44.1, 88.2, 176.4 kHz		-	740	-	ms
	Fs = 48, 96, 192 kHz		-	680	-	ms
MCLK Specifications						
MCLK Period		t_{clkw}	38	-	1953	ns
MCLK Pulse Duty Cycle			40	50	60	%
Master Mode						
SCLK falling to LRCK		t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	32	ns
SCLK Duty Cycle			-	50	-	%
Slave Mode						
Single-Speed						
Output Sample Rate		Fs	2	-	51	kHz
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclkw}	153	-	-	ns
SCLK Duty Cycle			45	50	55	%
SCLK falling to SDOUT valid		t_{dss}	-	-	32	ns
SCLK falling to LRCK edge		t_{slrd}	-20	-	20	ns
Double-Speed						
Output Sample Rate		Fs	50	-	102	kHz
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclkw}	153	-	-	ns
SCLK Duty Cycle			45	50	55	%
SCLK falling to SDOUT valid		t_{dss}	-	-	32	ns
SCLK falling to LRCK edge		t_{slrd}	-20	-	20	ns
Quad-Speed						
Output Sample Rate		Fs	100	-	204	kHz
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclkw}	77	-	-	ns
SCLK Duty Cycle			45	50	55	%
SCLK falling to SDOUT valid		t_{dss}	-	-	32	ns
SCLK falling to LRCK edge		t_{slrd}	-8	-	3	ns
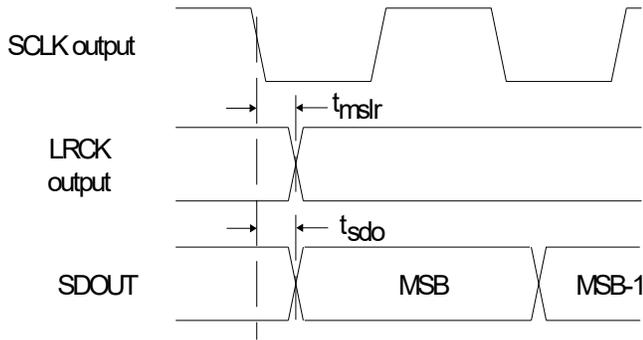
Figure 13. Master Mode, Left-Justified SAI
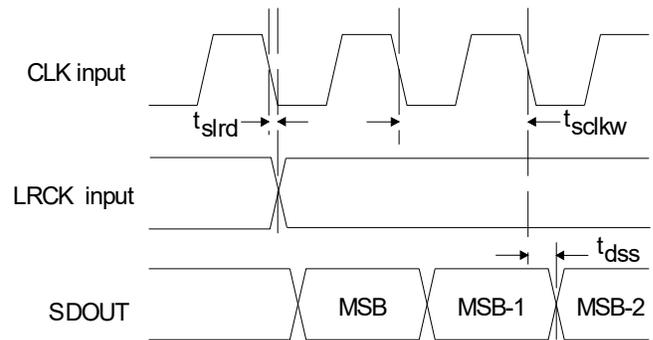
Figure 14. Slave Mode, Left-Justified SAI
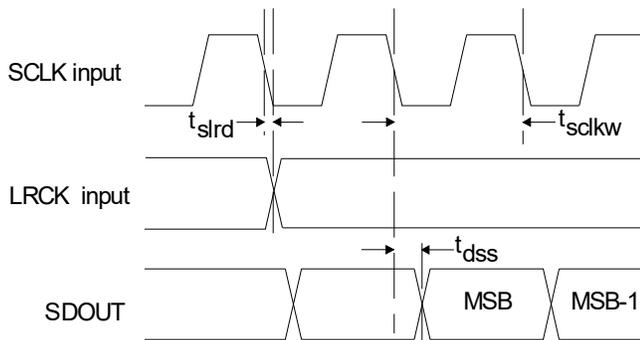
Figure 15. Master Mode, I^{2}S SAI
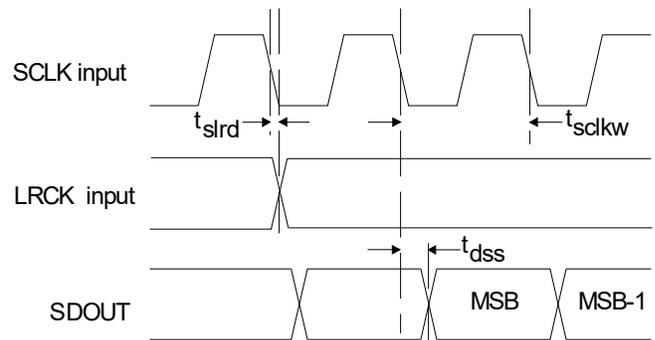
Figure 16. Slave Mode, I^{2}S SAI
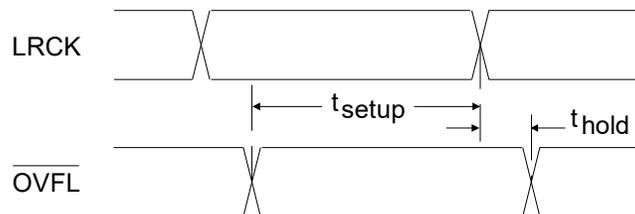
Figure 17. $\overline{\text{OVFL}}$ Output Timing
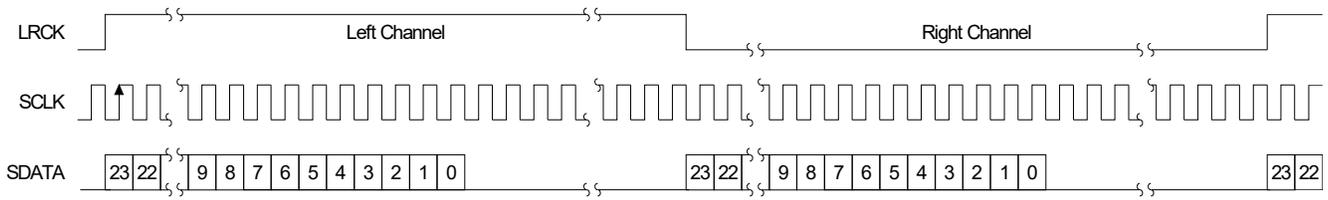
Figure 18. Left-Justified Serial Audio Interface
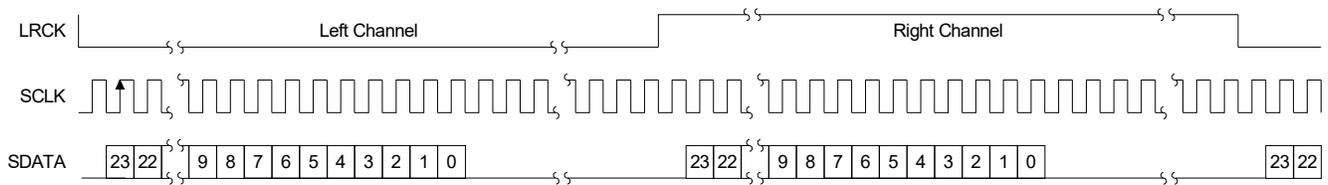
Figure 19. I²S Serial Audio Interface
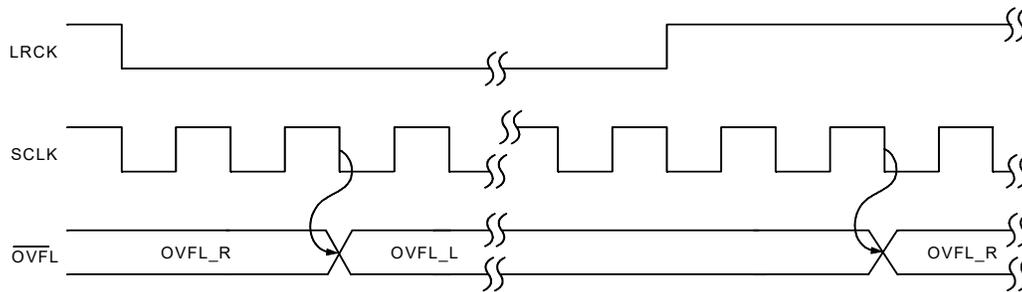
Figure 20. $\overline{\text{OVFL}}$ Output Timing, I²S Format
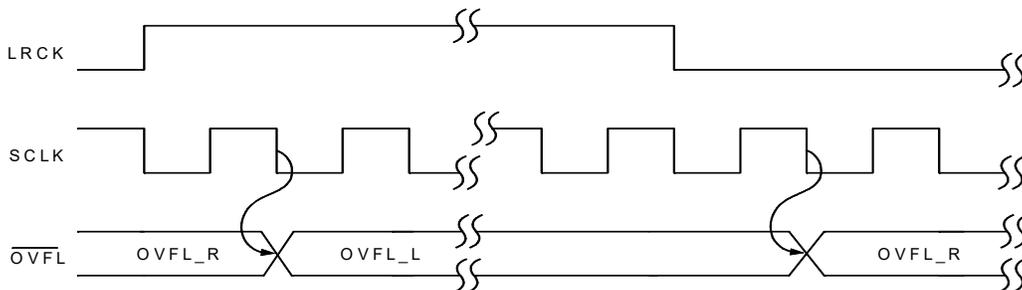
Figure 21. $\overline{\text{OVFL}}$ Output Timing, Left-Justified Format

2. PIN DESCRIPTIONS

```
        RST ☐ 1        24 ☐ FILT+
        M/S ☐ 2        23 ☐ REFGND
       LRCK ☐ 3        22 ☐ VQ3
       SCLK ☐ 4        21 ☐ AINR
       MCLK ☐ 5        20 ☐ VQ2
         VD ☐ 6        19 ☐ VA
        GND ☐ 7        18 ☐ GND
         VL ☐ 8        17 ☐ VQ1
      SDOUT ☐ 9        16 ☐ AINL
       MDIV ☐ 10       15 ☐ OVFL
        HPF ☐ 11       14 ☐ M1
     I²S/LJ ☐ 12       13 ☐ M0
```

Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - The device enters a low power mode when low.
M/S	2	**Master/Slave Mode** (*Input*) - Selects operation as either clock master or slave.
LRCK	3	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	4	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	7 18	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VL	8	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	9	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
MDIV	10	**MCLK Divider** (*Input*) **-** Enables a master clock divide by two function.
HPF	11	**High-Pass Filter Enable** (*Input*) **-** Enables the Digital High-Pass Filter.
I²S/LJ	12	**Serial Audio Interface Format Select** (*Input*) -Selects either the Left-Justified or I²S format for the SAI.
M0 M1	13 14	**Mode Selection** (*Input*) - Determines the operational mode of the device.
OVFL	15	**Overflow** (*Output, open drain*) **-** Detects an overflow condition on both left and right channels.
AINL AINR	16 21	**Analog Inputs** (*Input*) - The full-scale analog input level is specified in the Analog Characteristics specification table.
VQ1 VQ2 VQ3	17 20 22	**Quiescent Voltage** (*Output*) **-** Filter connection for the internal quiescent reference voltage.
VA	19	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
REF_GND	23	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
FILT+	24	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

3. TYPICAL CONNECTION DIAGRAM
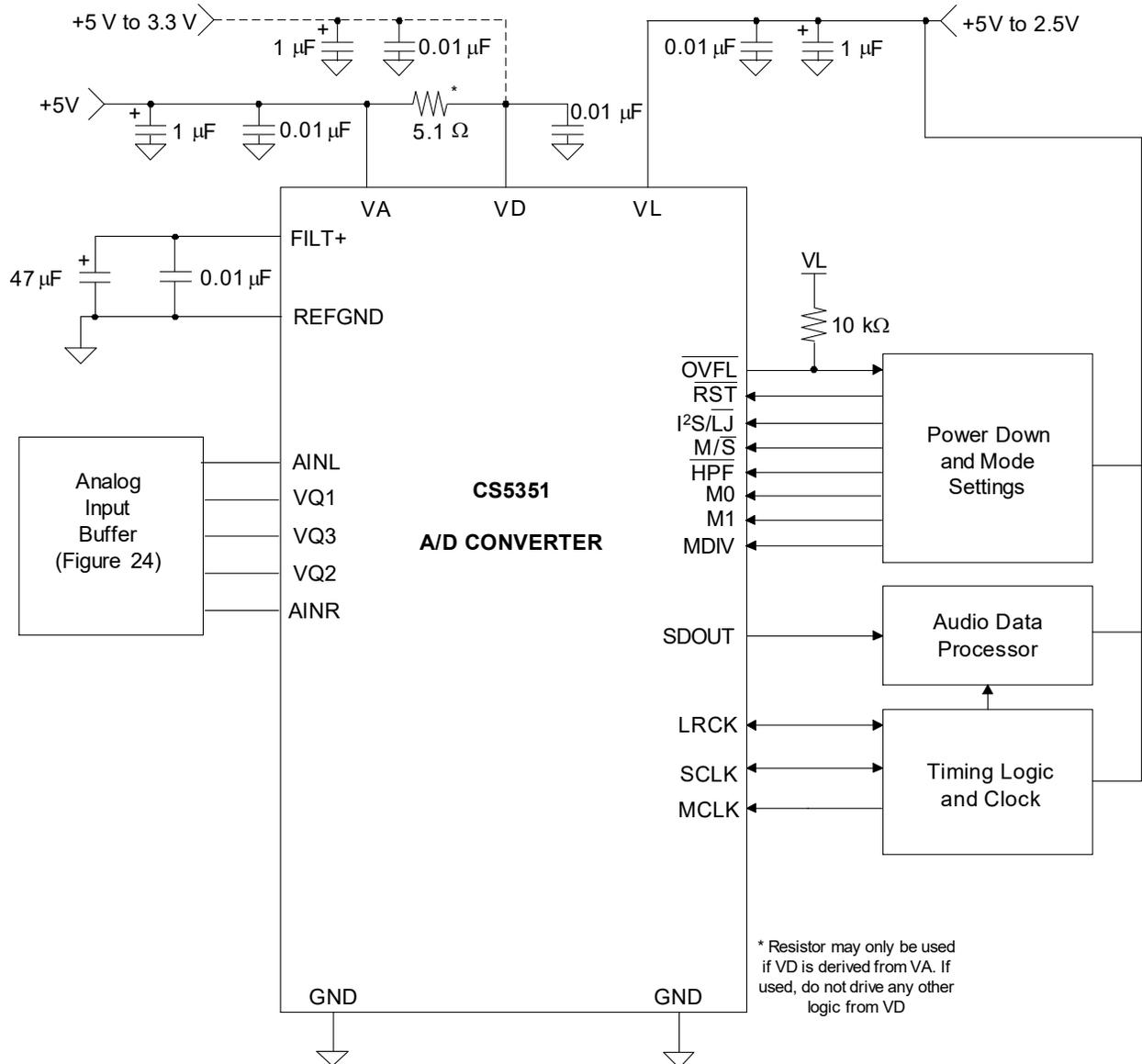
Figure 22. Typical Connection Diagram

4. APPLICATIONS

4.1 Operational Mode/Sample Rate Range Select

The output sample rate, Fs, can be adjusted from 2 kHz to 204 kHz. The CS5351 must be set to the proper speed mode via the mode pins, M1 and M0. Refer to Table 1.

M1 (Pin 14)	M0 (Pin 13)	MODE	Output Sample Rate (Fs)
0	0	Single-Speed Mode	2 kHz - 51 kHz
0	1	Double-Speed Mode	50 kHz - 102 kHz
1	0	Quad-Speed Mode	100 kHz - 204 kHz
1	1	Reserved	

Table 1. CS5351 Mode Control

4.2 System Clocking

The device supports operation in either Master Mode, where the left/right and serial clocks are synchronously generated on-chip, or Slave Mode, which requires external generation of the left/right and serial clocks. The device also includes a master clock divider in Master Mode where the master clock will be internally divided prior to any other internal circuitry when MDIV is enabled, set to logic 1. In Slave Mode, the MDIV pin needs to be disabled, set to logic 0.

4.2.1 Slave Mode

LRCK and SCLK operate as inputs in Slave Mode. The left/right clock must be synchronously derived from the master clock and be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance. Refer to Table 2 for required clock ratios.

	Single-Speed Mode Fs = 2 kHz to 51 kHz	Double-Speed Mode Fs = 50 kHz to 102 kHz	Quad-Speed Mode Fs = 100 kHz to 204 kHz
MCLK/LRCK Ratio	256x, 512x	128x, 256x	128x
SCLK/LRCK Ratio	32x, 64x, 128x	32x, 64x	32x, 64x

Table 2. CS5351 Slave Mode Clock Ratios

4.2.2 Master Mode

In Master Mode, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 23. Refer to Table 3 for common master clock frequencies.
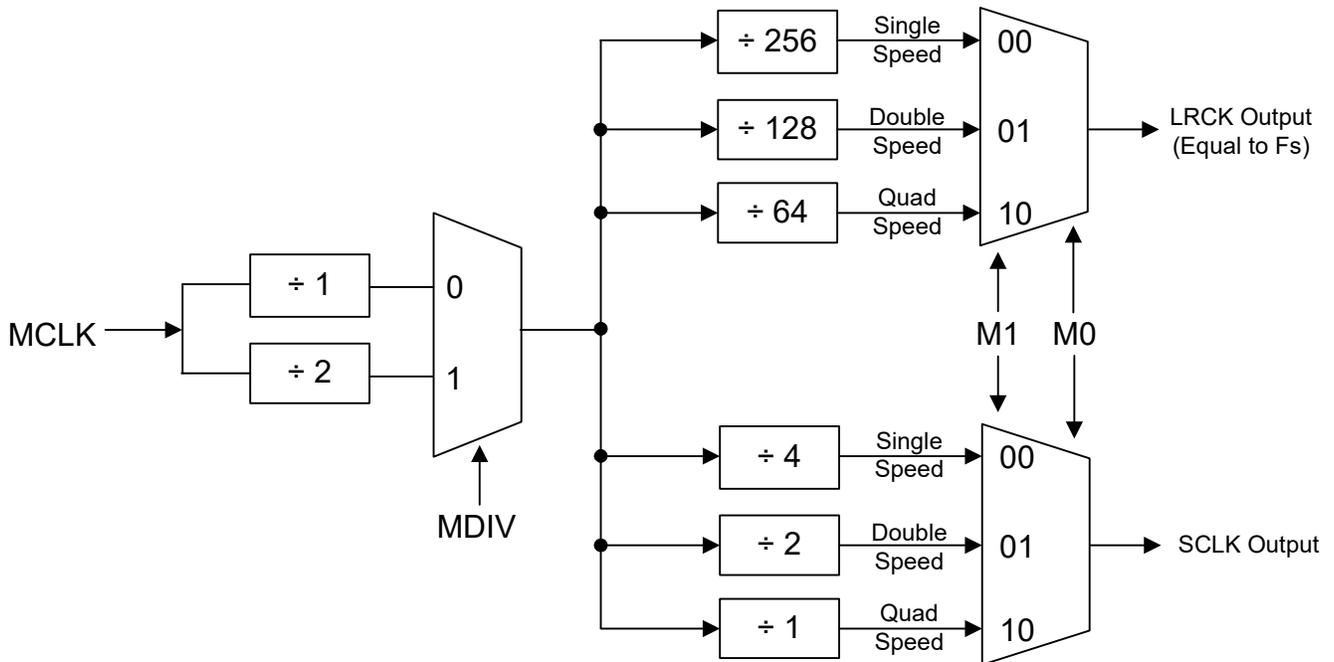
Figure 23. CS5351 Master Mode Clocking

SAMPLE RATE (kHz)	MDIV = 0 MCLK (MHz)	MDIV = 1 MCLK (MHz)
32	8.192	16.384
44.1	11.2896	22.5792
48	12.288	24.576
64	8.192	16.384
88.2	11.2896	22.5792
96	12.288	24.576
176.4	11.2896	22.5792
192	12.288	24.576

Table 3. CS5351 Common Master Clock Frequencies

4.3 Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

The internal reference voltage must be stable for the device to produce valid data. Therefore, there is a delay between the release of reset and the generation of valid output, due to the finite output impedance of FILT+ and the presence of the external capacitance.

4.4 Analog Connections

The analog modulator samples the input at 6.144 MHz. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are (n × 6.144 MHz) the digital passband frequency, where n=0,1,2,...Refer to Figure 24 which shows the suggested filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.
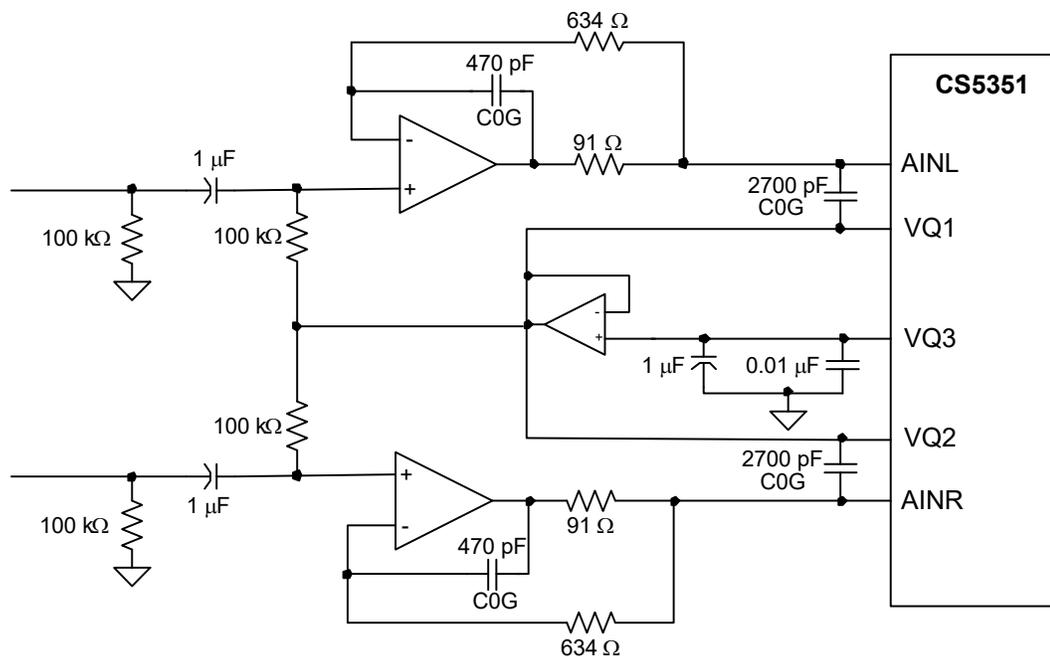
Figure 24. CS5351 Recommended Analog Input Buffer

4.5 High-Pass Filter and DC Offset Calibration

The operational amplifiers in the input circuitry driving the CS5351 may generate a small DC offset into the A/D converter. The CS5351 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPF pin is taken high during normal operation, the current value of the DC offset register is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

Running the CS5351 with the high pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.

Disabling the high pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5351.

4.6 Overflow Detection

The CS5351 includes overflow detection on both the left and right channels. This time multiplexed information is presented as open drain, active low on pin 15, $\overline{OVFL}$. The OVFL_L and OVFL_R data will go to a logical low as soon as an overrange condition in either channel is detected. The data will remain low as specified in the Switching Characteristics - Serial Audio Port section. This ensures sufficient time to detect an overrange condition regardless of the speed mode. After the timeout, the OVFL_L and OVFL_R data will return to a logical high if there has not been any other overrange condition detected. Please note that an overrange condition on either channel will restart the timeout period for both channels.

4.6.1 $\overline{OVFL}$ Output Timing

In left-justified format, the $\overline{OVFL}$ pin is updated one SCLK period after an LRCK transition. In I^{2}S format, the $\overline{OVFL}$ pin is updated two SCLK periods after an LRCK transition. Refer to Figures 23 and 24. In both cases the $\overline{OVFL}$ data can be easily demultiplexed by using the LRCK to latch the data. In left-justified format, the rising edge of LRCK would latch the right channel overflow status, and the falling edge of LRCK would latch the left channel overflow status. In I^{2}S format, the falling edge of LRCK would latch the right channel overflow status and the rising edge of LRCK would latch the left channel overflow status.

4.7 Grounding and Power Supply Decoupling

As with any high-resolution converter, the CS5351 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 22 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from FILT+ and REFGND. The CDB5351 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

4.8 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS5351's in the system. If only one master clock source is needed, one solution is to place one CS5351 in Master Mode, and slave all of the other CS5351's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5351 reset with the inactive edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

5. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

6. PACKAGE DIMENSIONS

24L SOIC (300 MIL BODY) PACKAGE DRAWING
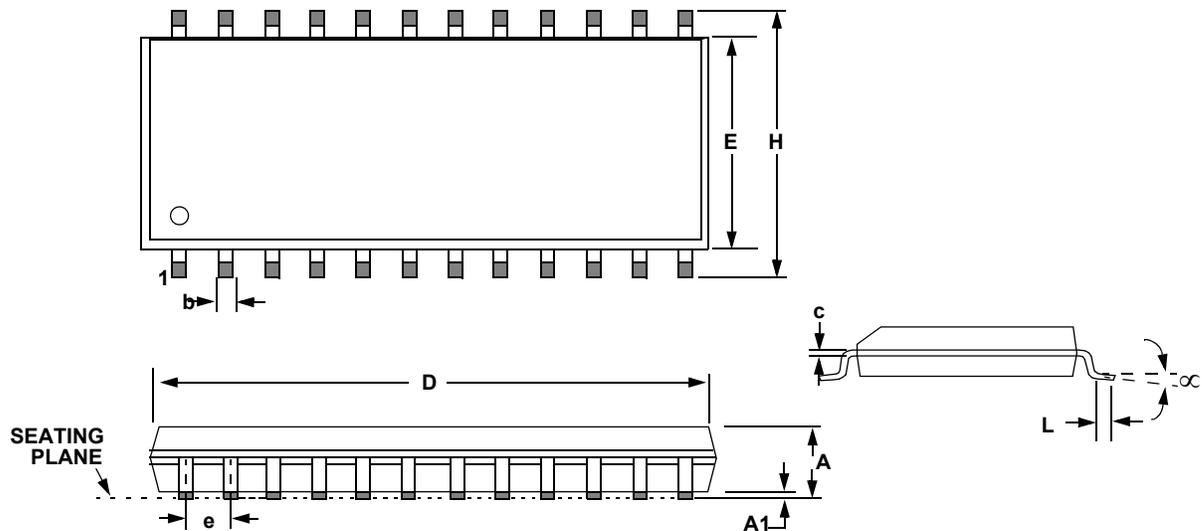
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING
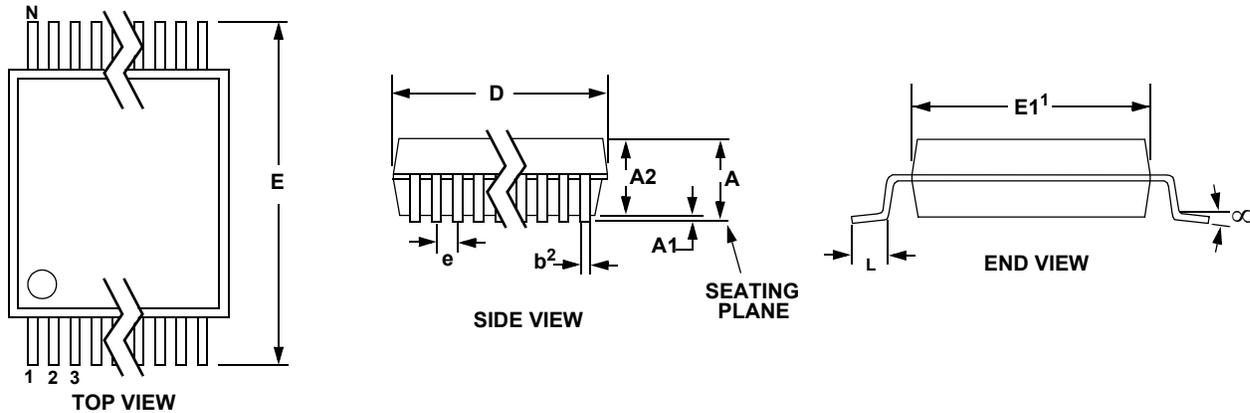
DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.303	0.307	0.311	7.70	7.80	7.90	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
$\propto$	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153
Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

7. REVISION HISTORY

Release	Changes
PP2	Preliminary datasheet.
F1	Improve Gain Error specification under Analog Characteristics. Specify Full-scale Input Voltage in terms of VA under Analog Characteristics. Update Differential Input Impedance under Analog Characteristics. Increase maximum Power-Supply Current, I_A, under DC Electrical Characteristics. Reduce maximum Power Consumption under DC Electrical Characteristics. Update FILT+ Output Impedance specification under DC Electrical Characteristics. Extend maximum Fs in Single-Speed Mode to 51 kHz. Extend maximum Fs in Double-Speed Mode to 102 kHz. Extend maximum Fs in Quad-Speed Mode to 204 kHz. Decrease maximum SCLK falling to LRCK edge specification in Quad-Speed Mode. Replace minimum MCLK high/low timing specifications with duty cycle specification. Replace minimum SCLK high/low timing specifications with duty cycle specification.Replace recommended analog input buffer with new input buffer topology.
F2	Updated ordering information.
F3	Updated ordering information as per PCN-2020-141. Adopted more recent document template.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.