HIGH-PERFORMANCE USB PD SINK CONTROLLER

Description

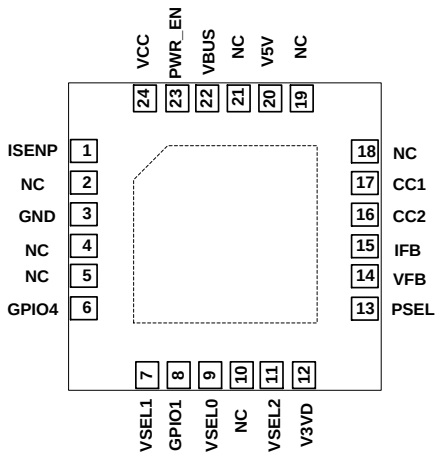
The AP33771 is a highly integrated USB Type-C® PD3.0/PPS sink controller. The device is targeted for DC power requests and control for Type-C connector-equipped devices (TCD). To leverage increasing popularity of standard Type-C PD3.0 power adaptors, the AP33771 negotiates with an existing PD3.0 adaptor to acquire the required power profile to supply the TCD.

Working its role as DC-power requests from USB PD sources, the AP33771 interprets power input requirements (voltage/current and maximum power) from the TCD, and then establishes a power link with an external USB PD3.0 adaptor to output a suitable DC power. The voltage requests are specified by three pins (VSEL2, VSEL1, VSEL0). Up to eight voltages can be selected, and both fixed PDO and PPS APDO in the PD source adapter are supported in the AP33771 search algorithm. Up to ten maximum power levels can also be selected through different resistance values of the resistor connected to the PSEL pin (refer to figure 1 and 2).

Rich power functions are embedded on the chip to reduce total BOM while maintaining maximum flexibility. A one-time-programmable (OTP) ROM is provided to store the PD/sink controller firmware.

Pin Assignments

(Top View)



W-QFN4040-24 (Type A1)

Features

- Compliant with USB PD Rev. 3.0 v1.2
- USB-IF certificated TID: 5000
- Supports up to eight voltage selections by pin setting
- Supports voltage selection with dynamic pin setting
- Supports power capability selection
- Supports flash FAULT LED indication for negotiation mismatch
- Supports OTP (One-Time-Programmable) for main firmware
- Supports OVP with hard reset and auto restart
- Supports driver for N-MOS VBUS power switch
- Supports dead-battery mode
- Operating voltage range: 3.3V to 24V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- USB Type-C connector-equipped battery-powered devices
- USB Type-C connector-equipped dc-power input devices
- USB PD3.0 PPS testers
- USB Type C-to-traditional barrel connector power adaptor cables

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit

The AP33771 is a USB Type-C power delivery sink controller and that is used to request power from a standard USB PD source adapter, as shown in the figure below.

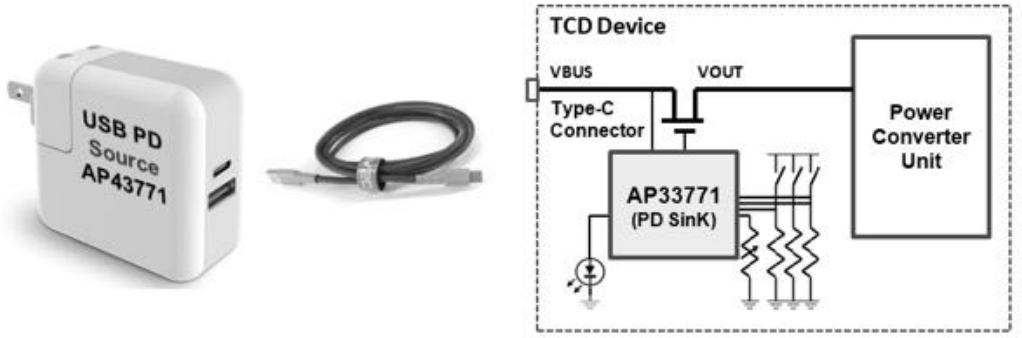
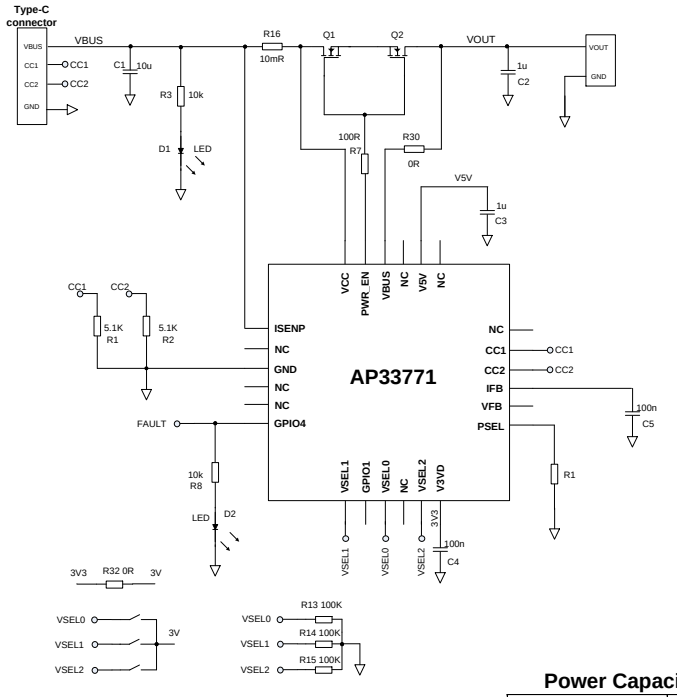


Figure 1. Typical Application structure of AP33771

The AP33771 can request power through the resistor setting. A typical setting of AP33771 to get a DC power is shown as below.



Voltage Selection

VSEL2	VSEL1	VSEL0	Target Voltage
0	0	0	5V
0	0	1	9V
0	1	0	15V
0	1	1	20V
1	0	0	4.3V
1	0	1	8.6V
1	1	0	12.9V
1	1	1	17.2V

Power Capacity Selection

Value of R1	Power Capacity
6.8K	12W
16K	15W
27K	18W
36K	20W
45.3K	27W
56K	36W
64.9K	45W
75K	60W
82K	90W
91K	100W

Figure 2. Typical Application Circuit of AP33771

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Pin Descriptions

Pin No	Pin Name	Type*	Pin Function
1	ISENP	AIO	Current Sense Positive Node.
2	NC	—	No Connection
3	GND	GND	Ground
4	NC	—	No Connection
5	NC	—	No Connection
6	GPIO4	DIO	General Purpose Input/Output pin, for LED usage.
7	VSEL1	DIO	For Voltage Select Pin1
8	GPIO1	DIO	General Purpose Input / Output
9	VSEL0	DIO	For Voltage Select Pin0
10	NC	—	No Connection
11	VSEL2	DIO	For Voltage Select Pin2
12	V3VD	DP	3.3V LDO Output. Power for Digital circuit and Digital I/O pins, with 0.1μF to Ground
13	PSEL	AIO	For Power Capability Selection.
14	VFB	AI	For Voltage Measurement.
15	IFB	AI	For Current Measurement, with 100nF to Ground
16	CC2	AIO	Type-C configuration channel 2
17	CC1	AIO	Type-C configuration channel 1
18	NC	—	No Connection
19	NC	—	No Connection
20	V5V	AP	5V LDO output. Power for Analog circuit and Analog I/O pins, with 1μF to Ground
21	NC	—	No Connection
22	VBUS	AHV	Terminal for Discharge Path.
23	PWR_EN	AHV	To control external NMOS switch ON (High) or OFF (Low).
24	VCC	AHV	The power supply of the IC, connected to a ceramic capacitor.
—	EP	GND	Exposed pad is connected to Ground

*AHV– Analog High Voltage pin
*AP – Power for Analog Circuit and Analog I/O pins, 5.0V operation
*AI – Analog Input pin
*DP – Power for Digital Circuit and I/O pins, 3.3V operation
*AIO – Analog I/O pin.
*DIO – Digital I/O pin.

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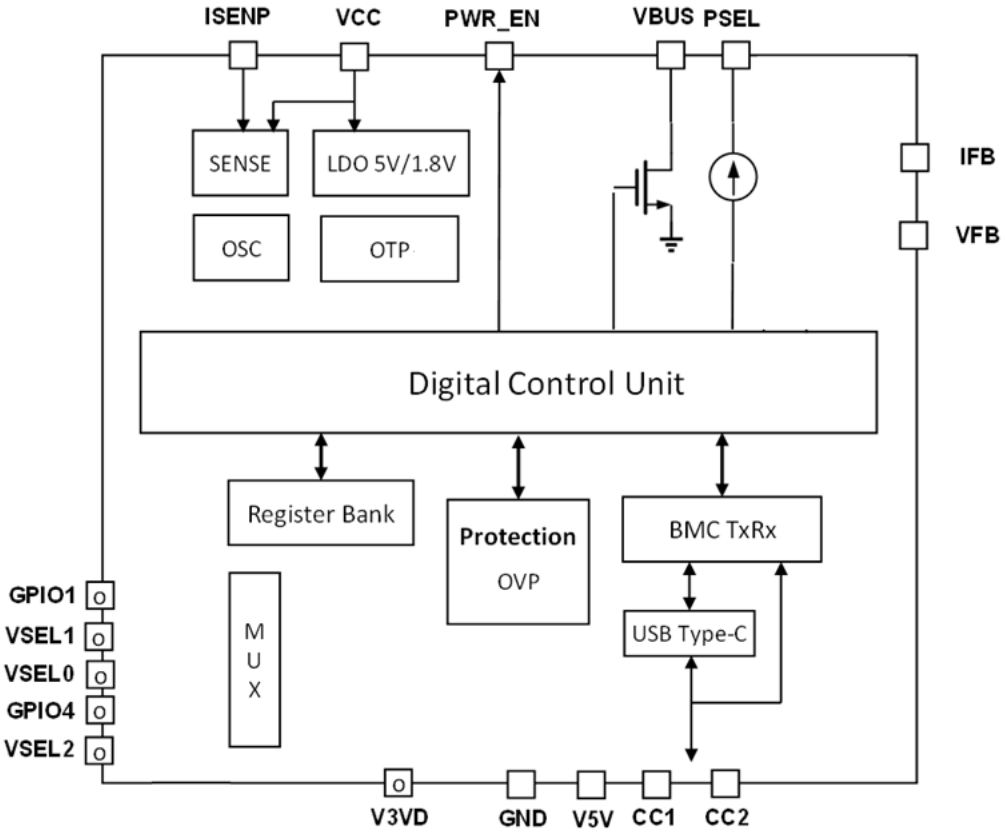
Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Input Voltage at VCC Pin	-0.3 to 24	V
V_{FB}, V_{IFB}, V_{PSEL}	Input Voltage at VFB, IFB, PSEL Pins	-0.3 to 7	V
V_{BUS}, V_{PWR_EN}, V_{ISENP}	Input Voltage at VBUS, PWR_EN, ISENP Pins	-0.3 to 24	V
—	Voltage from PWR_EN to VCC Pin	-16 to 7	V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V_{V3VD}	Input Voltage at V3VD Pin	-0.3 to 5	V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 7	V
V_{GPIO1}, V_{GPIO4}, V_{VSEL0} – V_{VSEL2}	Input Voltage at GPIO1,GPIO4,VSEL0 – VSEL2 Pins	-0.3 to 5	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	28	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	16	°C/W
ESD	Human Body Model	2	kV
ESD	Charged Device Model	750	V

Notes: 4. Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.
5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Voltage	3.3	24	V
V_{PSEL}	Input Voltage at PSEL Pin	0	3.7	V
V_{VSEL0} ~ V_{VSEL2}	Input Voltage at VSEL0 ~ VSEL2 Pins	0	3.7	V
V_{GPIO1}, V_{GPIO4}	Input Voltage at GPIO1, GPIO4 Pins	0	3.7	V
T_{OP}	Operating Temperature Range	-40	+85	°C

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Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC SECTION						
V_{ST}	Startup Voltage	—	2.5	2.8	3.2	V
V_{UVLO}	Minimum Operating Voltage	—	2.4	2.7	3	V
V_{CC_HYS}	V_{CC} Hysteresis (V_{ST}-V_{UVLO})	—	0.05	—	—	V
$I_{CC\_DEEP\ SLEEP}$	V_{IN} Current in Deep Sleep Mode	CC1/2 Detach after 3s V_{CC} = 5V	—	550	900	μA
I_{CC_OPR}	Operating Supply Current	V_{CC} = 5V	—	3.3	6	mA
CC1/CC2 SECTION						
V_{L_RD3A}	Low Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V_{H_RD3A}	High Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	2.0	—	V
VOLTAGE SELECTION AND POWER SELECTION						
V_{VSEL_HI}	VSEL0 ~ VSEL2 High Voltage (Note 7)	V_{CC} = 5V	1.4	—	—	V
V_{VSEL_LO}	VSEL0 ~ VSEL2 Low Voltage (Note 7)	V_{CC} = 5V	—	—	0.4	V
T_{VSEL_S}	VSEL0 ~ VSEL2 Scan Interval	—	—	250	—	ms
T_{VSEL_TD}	VSEL0 ~ VSEL2 Trap Debounce	—	—	70	—	μs
I_{PSEL}	PSEL Current Source (Note 7)	—	—	20	—	μA
I_{PSEL_Range}	PSEL Current Source Range (Note 7)	—	-3	—	+3	%
GPIO SECTION						
V_{GPIO_HI}	GPIO1, GPIO4 High Voltage (Note 7)	V_{CC} = 5V	1.4	—	—	V
V_{GPIO_LO}	GPIO1, GPIO4 Low Voltage (Note 7)	V_{CC} = 5V	—	—	0.4	V
I_{GPIO}	GPIO1, GPIO4 Sink/Source Capability (Note 7)	—	2	—	—	mA
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Note 6, 7)	—	—	7	—	V
V_{OVP20V}	OVP_20V Enable Voltage (Note 6, 7)	—	—	22	—	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 8)	—	—	90	—	ms
I_{OVD}	Overvoltage Discharge Current	V_{CC} = 5V	150	200	250	mA
t_{OV_DELAY}	Delay from OVP Threshold Trip to NMOS Gate Turn-Off (Note 7)	—	—	—	50	ms

Notes: 6. 110% OVP setting @PDO>18V. PDO+2V OVP setting @PDO≤18V.
7. Guaranteed by design.
8. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

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Performance Characteristics

Function Description

The AP33771 meets USB Power Delivery specification Rev. 3.0 v1.2 (USB-IF certificated TID: 5000). The device provides a cost-effective solution without the need for external, discrete, high-voltage components like LDOs. During the protocol handshake process, packets are transmitted and received through the embedded BMC (Biphase Mark Coding) transceiver with good eye diagram and high noise immunity. The OTP ROM is also used to store main protocol, application firmware, and system configuration parameters. The desired PDO for the AP33771-embedded TCD can be specified through a resistor setting scheme.

CC Interface and BMC Transceiver

For inter-operability consideration, CC interface detection and the CC's BMC transceiver are optimally designed to maintain operating voltage tolerance and noise immunity.

USB Power Delivery Controller

To be in full compliance with critical USB Power Delivery specification Rev. 3.0 v1.2, the AP33771 is implemented through a combination of hardware and OTP firmware to leverage quick response time in hardware and flexibility in software.

Sink Voltage Selection

The AP33771 provides a search algorithm for voltage request through high/low voltage settings at the VSEL0, VSEL1, and VSEL2 pins. While the AP33771 latches the pin setting at power-on, the device auto-scans and periodically latches the pin setting. Both fixed PDO and PPS APDO in the PD source adapter are supported in the AP33771 voltage search algorithm. With the three-resistor-setting combination, the design may use the AP33771 to specify up to eight voltage levels to fit the needs of a specific TCD.

Power Capability Selection

With a small constant current source output from the PSEL pin, the AP33771 measures voltage level at the PSEL pin with the attached resistor through internal ADC. Up to ten power selections are supported. TCD designers are recommended to use the resistor within ±1% accuracy to connect to the PSEL pin, ensuring the request power selection.

NMOS VBUS Switch Control

Once the PDO negotiations are successful in both voltage selection and power selection, PWR_EN will enable NMOS VBUS switch. If any mismatch in voltage selection or power selection is found, the NMOS VBUS switch will not turn on.

LED Indication

GPIO4 is used to control LED flickering. The user is notified of the system status from the LED flashing pattern, defined in Table 1. Any non-PD power source is not supported in the AP33771, and the LED will show the mismatch accordingly.

Condition	LED Pattern	Description
Charging	Breathing light (2s dimming)	1 cycle is 4s
Fully charged	Continuously lit	Charging current < 500mA
Mismatch	1s flicker	Voltage or power mismatch. Non-PD power source. 1 cycle is 2s
Fault	300ms flicker	OVP. 1 cycle is 600ms

Table 1 – LED Indication Table

OVP Protection

The AP33771 provides an overvoltage protection (OVP) feature by sending a hard reset to the PD source when VBUS is higher than OVP threshold voltage. As soon as overvoltage conditions occur, the device provides an internal discharge path to reduce the overvoltage duration.

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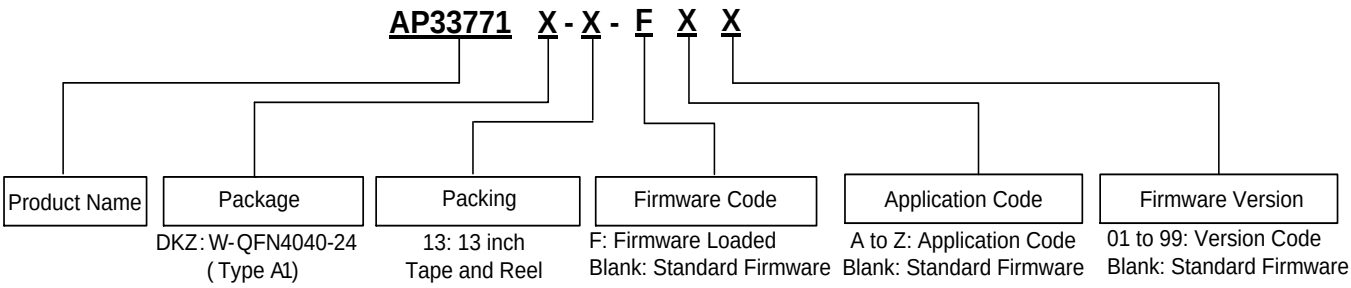
Ordering Information

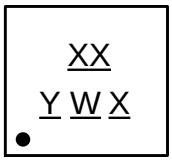


Orderable Part Number	Package	Identification Code	Packing		
			Quantity	Carrier	Part Number Suffix
AP33771DKZ-13-FXX	W-QFN4040-24 (Type A1)	6C	3,000	13” Tape & Reel	-13

Marking Information

W-QFN4040-24

(Top View)



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week; a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

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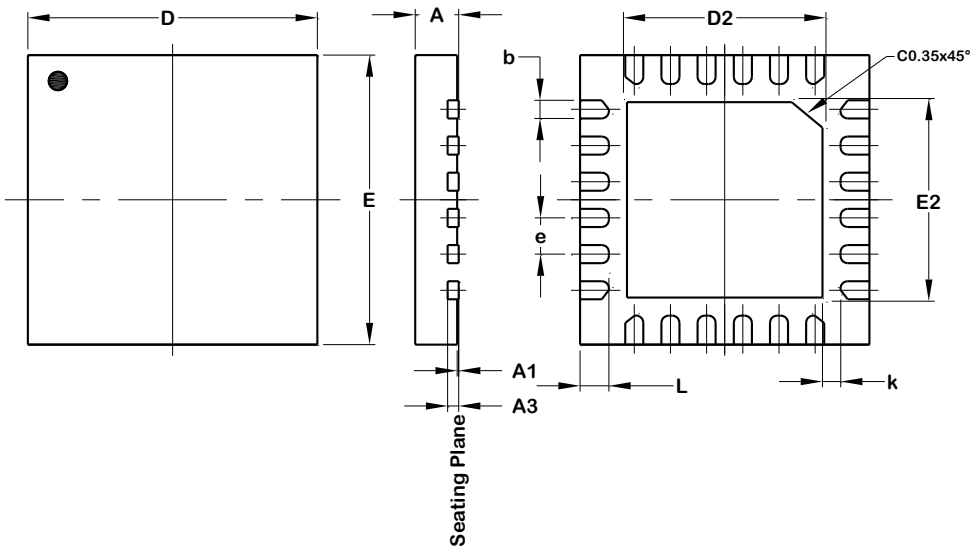
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)

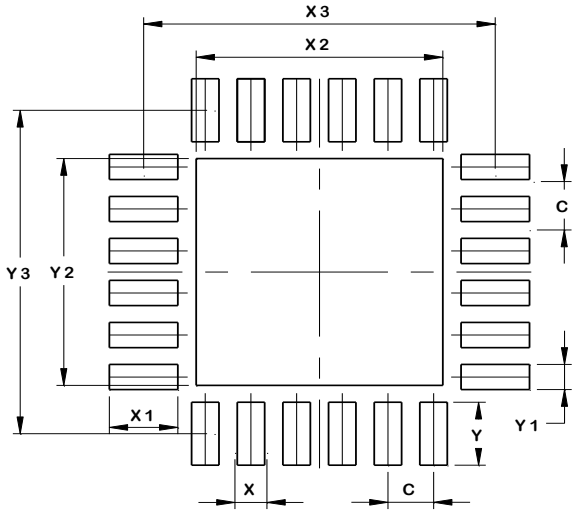


W-QFN4040-24 (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	4.00 BSC		
D2	2.65	2.75	2.70
E	4.00 BSC		
E2	2.65	2.75	2.70
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.700
X3	3.850
Y	0.750
Y1	0.300
Y2	2.700
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—Matte Tin Plated Leads, Solderable per J-STD-202 (e3)
- Weight: 0.041 grams (Approximate)

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