- **Members of the Texas Instruments *Widebus*™ Family**
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT162500 . . . WD PACKAGE
SN74ABT162500 . . . DL PACKAGE
(TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	$\overline{\text{CLKAB}}$
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
$\overline{\text{OEBA}}$	27	30	$\overline{\text{CLKBA}}$
LEBA	28	29	GND

description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

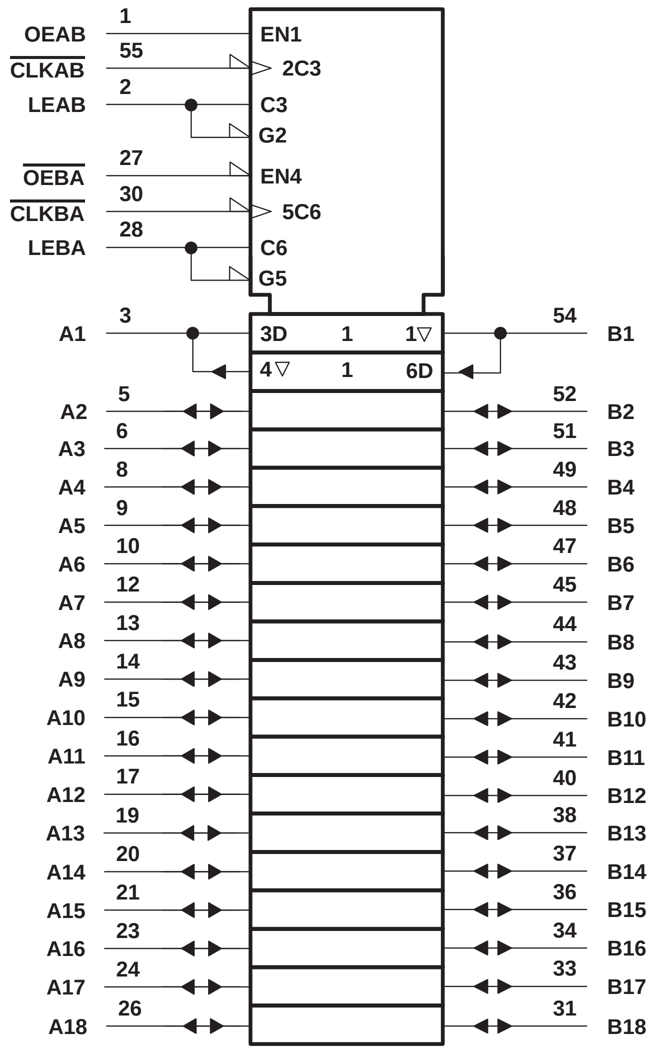
The SN54ABT162500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162500 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

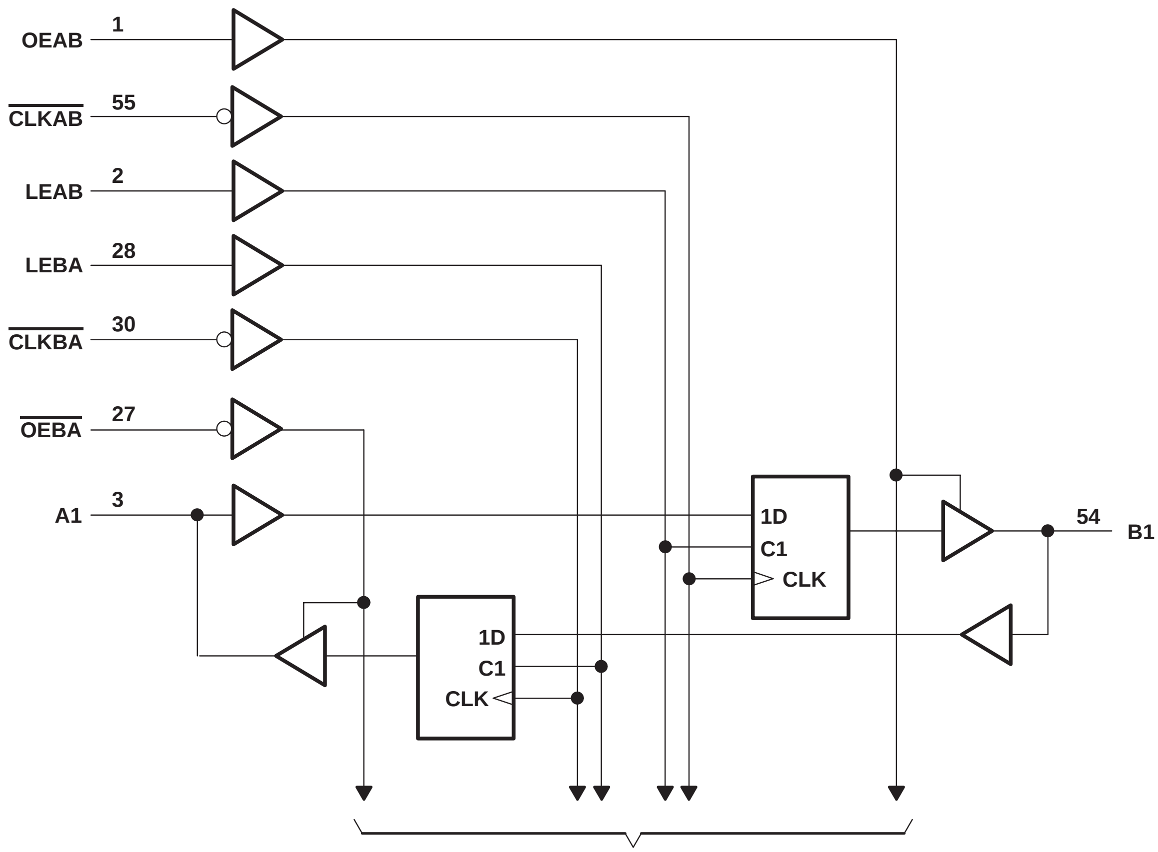
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
‡ Output level before the indicated steady-state input conditions were established
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O		–0.5 V to 5.5 V
Current into any output in the low state, I_O:	SN54ABT162500 (A port)	96 mA
	SN74ABT162500 (A port)	128 mA
	B port	30 mA
Input clamp current, I_{IK} (V_I < 0)		–18 mA
Output clamp current, I_{OK} (V_O < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DL package		74°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			SN54ABT162500		SN74ABT162500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		–24		–32	mA
		B port		–12		–12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162500		SN74ABT162500		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	A port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
			I_{OH} = –32 mA	2*					2		
	B port	V_{CC} = 4.5 V,	I_{OH} = –1 mA	3.35			3.3		3.35		
		V_{CC} = 5 V,	I_{OH} = –1 mA	3.85			3.8		3.85		
		V_{CC} = 4.5 V	I_{OH} = –3 mA	3.1			3		3.1		
			I_{OH} = –12 mA	2.6					2.6		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55*				0.55	
	B port	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	
V_{hys}					100						mV
I_I	Control inputs	V_{CC} = 0 to 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports	V_{CC} = 2.1 V to 5.5 V, V_I = V_{CC} or GND				±20		±20		±20	
I_{OZPU}		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ or OE = X§				±50		±50		±50	µA
I_{OZPD}		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ or OE = X§				±50		±50		±50	µA
I_{OZH}‡		V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, $\overline{OE}$ ≥ 2 V or OE ≤ 0.8 V				10		10		10	µA
I_{OZL}‡		V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, $\overline{OE}$ ≥ 2 V or OE ≤ 0.8 V				–10		–10		–10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–110	–180	–50	–180	–50	–180	mA
	B port			–25	–55	–90	–25	–90	–25	–90	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ For V_{CC} between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
\# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

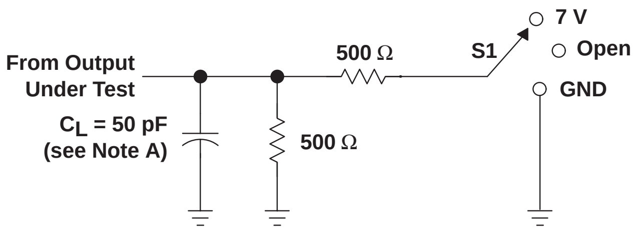
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT162500		SN74ABT162500		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				150		150	MHz
t_w	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low		3		3		
t_{su}	Setup time	A before $\overline{CLKAB}$↓		3.3		3.3		ns
		B before $\overline{CLKBA}$↓		3.3		3.3		
		A before LEAB↓ or B before LEBA↓	$\overline{CLK}$ high	1		1		
			$\overline{CLK}$ low	2.5		2.5		
t_h	Hold time	A after $\overline{CLKAB}$↓ or B after $\overline{CLKBA}$↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

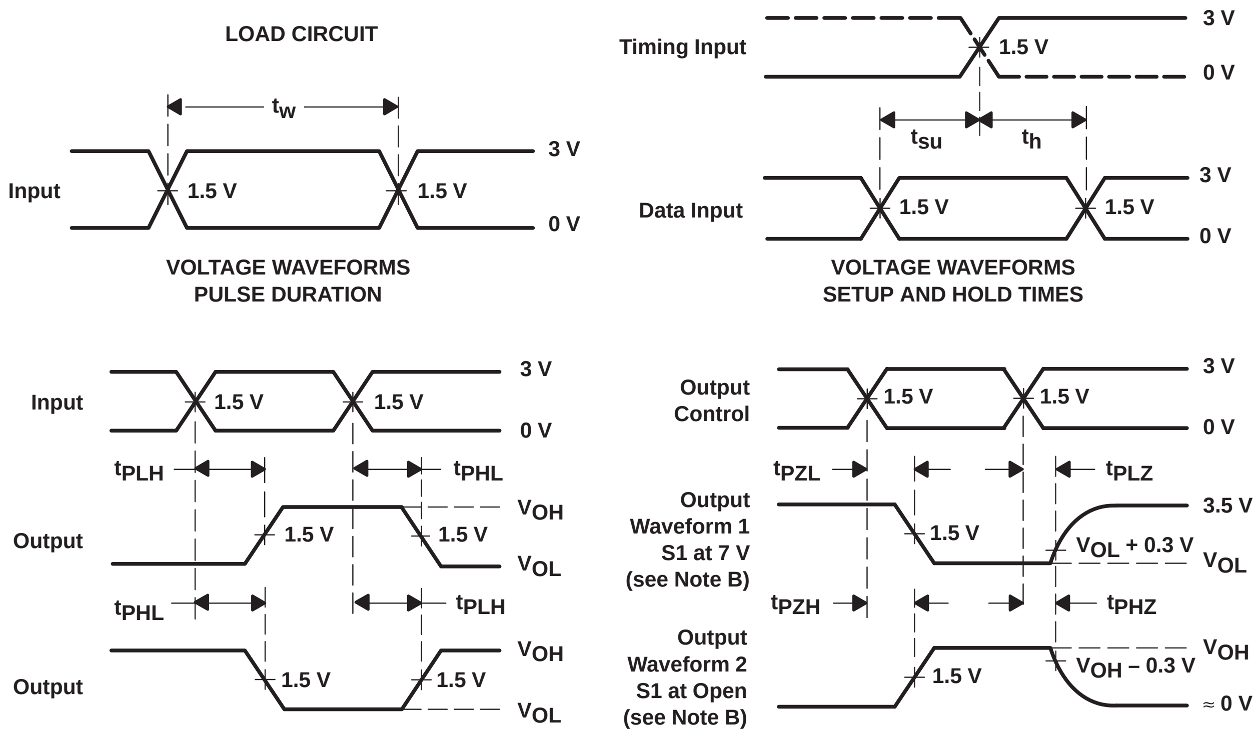
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162500		SN74ABT162500		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A	1.5	2.6	4	1.5	5.1	1.5	4.8	ns
t_{PHL}			2	3.4	5.2	2	6.1	2	5.7	
t_{PLH}	LEAB or LEBA	B or A	2	3.3	4.8	2	6.1	2	5.6	ns
t_{PHL}			2	3.8	5.2	2	6.4	2	5.9	
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	1.5	3.7	4.9	1.5	6.4	1.5	5.9	ns
t_{PHL}			1.5	3.8	5.2	1.5	6.4	1.5	6	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	1.5	3.4	4.6	1.5	5.6	1.5	5.3	ns
t_{PZL}			2	3.8	4.7	2	5.6	2	5.4	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	2	4.5	5.7	2	6.9	2	6.5	ns
t_{PLZ}			1.5	3.8	5.3	1.5	6.3	1.5	5.8	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT162500DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162500	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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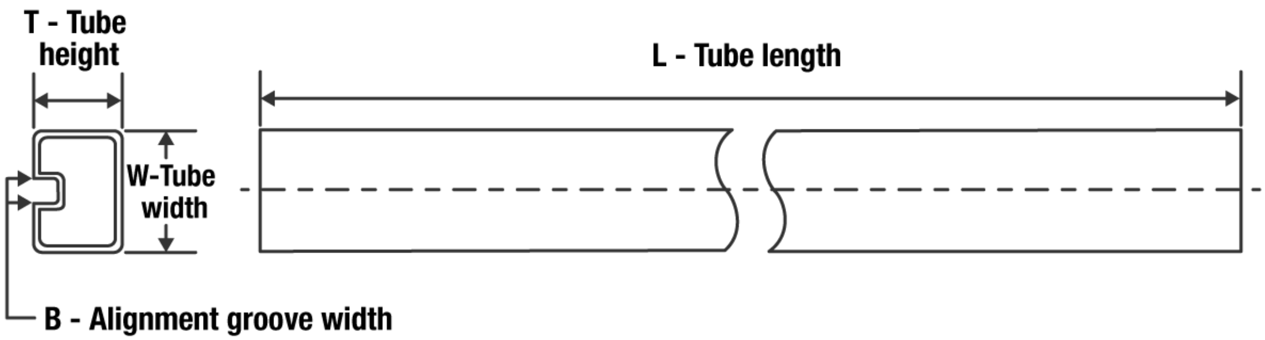
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT162500DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

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