

74AUP2G79-Q100

Low-power dual D-type flip-flop; positive-edge trigger

Rev. 4 — 18 July 2023

Product data sheet

1. General description

The 74AUP2G79-Q100 provides the dual positive-edge triggered D-type flip-flop. Information on the data input (nD) is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse (nCP). The nD input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AUP2G79DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G79DC-Q100	p79

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

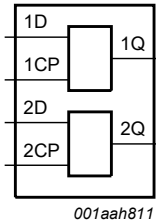


Fig. 1. Logic symbol

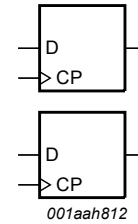


Fig. 2. IEC logic symbol

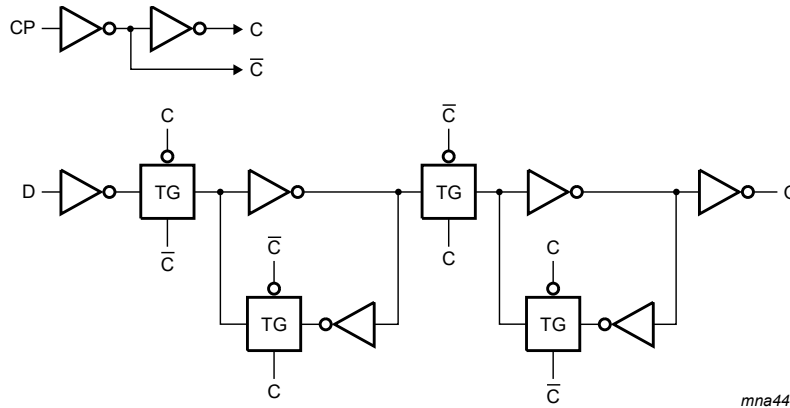


Fig. 3. Logic diagram (one flip-flop)

6. Pinning information

6.1. Pinning

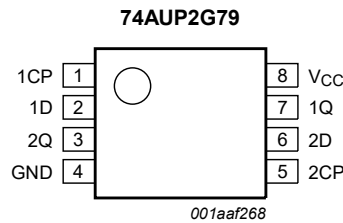


Fig. 4. Pin configuration SOT765-1 (VSSOP8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 5	clock pulse input
1D, 2D	2, 6	data input
GND	4	ground (0 V)
1Q, 2Q	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition; X = don't care;
q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

Input		Output
nCP	nD	nQ
↑	L	L
↑	H	H
L	X	q

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	Active mode and Power-down mode	[1] -0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CC}	-	±20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.75V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.11	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.32	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	μA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.2	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	[1]	-	40	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.6	-	pF
C _O	output capacitance	V _O = GND; V _{CC} = 0 V	-	1.3	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.7V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.03	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.30	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	µA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.6	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.9	µA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	[1]	-	50	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	µA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	µA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	[1]	-	75	µA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t _{pd}	propagation delay	nCP to nQ; see Fig. 5 [2]								
		V _{CC} = 0.8 V	-	19.7	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.6	5.5	11.0	2.4	12.9	2.4	14.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.0	3.8	7.0	1.8	8.1	1.8	9.0	ns
		V _{CC} = 1.65 V to 1.95 V	1.7	3.1	5.4	1.5	6.4	1.5	7.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.3	4.0	1.1	4.7	1.1	5.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	2.0	3.4	0.9	4.0	0.9	4.4	ns
f _{max}	maximum frequency	nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	53	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	203	-	170	-	170	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	347	-	310	-	300	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz
C_L = 10 pF										
t _{pd}	propagation delay	nCP to nQ; see Fig. 5 [2]								
		V _{CC} = 0.8 V	-	23.1	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.1	6.3	12.3	2.8	14.4	2.8	15.9	ns
		V _{CC} = 1.4 V to 1.6 V	2.5	4.4	8.1	2.2	9.5	2.2	10.5	ns
		V _{CC} = 1.65 V to 1.95 V	2.1	3.6	6.3	1.9	7.5	1.9	8.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.8	2.8	4.7	1.5	5.6	1.5	6.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.7	2.5	4.1	1.3	4.5	1.3	5.0	ns
f _{max}	maximum frequency	nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	52	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz
C_L = 15 pF										
t _{pd}	propagation delay	nCP to nQ; see Fig. 5 [2]								
		V _{CC} = 0.8 V	-	26.6	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.5	7.1	13.6	3.2	15.6	3.2	17.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.8	5.0	9.2	2.5	10.7	2.5	11.8	ns
		V _{CC} = 1.65 V to 1.95 V	2.4	4.1	7.1	2.2	8.5	2.2	9.4	ns
		V _{CC} = 2.3 V to 2.7 V	2.2	3.2	5.4	1.9	6.3	1.9	7.0	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	2.9	4.5	1.6	5.0	1.6	5.5	ns

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	50	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
C_L = 30 pF										
t _{pd}	propagation delay	nCP to nQ; see Fig. 5 [2]								
		V _{CC} = 0.8 V	-	36.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.7	9.3	17.3	4.2	23.3	4.2	25.6	ns
		V _{CC} = 1.4 V to 1.6 V	3.8	6.4	11.8	3.3	14.3	3.3	15.7	ns
		V _{CC} = 1.65 V to 1.95 V	3.3	5.3	9.4	3.0	11.3	3.0	12.4	ns
		V _{CC} = 2.3 V to 2.7 V	3.0	4.3	7.0	2.7	8.5	2.7	9.4	ns
		V _{CC} = 3.0 V to 3.6 V	2.8	3.9	5.8	2.6	7.2	2.6	7.9	ns
f _{max}	maximum frequency	nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	28	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	128	-	70	-	70	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	206	-	120	-	110	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	262	-	150	-	120	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	269	-	190	-	170	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	309	-	200	-	190	-	MHz
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
t _{su}	set-up time	HIGH; nD to nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	3.4	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	0.8	-	1.5	-	1.5	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.5	-	1.0	-	1.0	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.5	-	0.9	-	0.9	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.4	-	0.7	-	0.7	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.4	-	0.6	-	0.6	-	ns
		LOW; nD to nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	3.0	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	0.9	-	1.6	-	1.6	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.6	-	1.0	-	1.0	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.5	-	0.9	-	0.9	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.5	-	0.9	-	0.9	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.7	-	1.0	-	1.0	-	ns

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _h	hold time	nD to nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	-1.9	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	-0.6	-	0	-	0	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	-0.4	-	0	-	0	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	-0.4	-	0	-	0	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	-0.4	-	0	-	0	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	-0.3	-	0	-	0	-	ns
t _w	pulse width	HIGH or LOW; nCP; see Fig. 6								
		V _{CC} = 0.8 V	-	5.6	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	2.4	-	3.5	-	3.5	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	1.3	-	2.0	-	2.0	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.9	-	1.9	-	1.9	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.7	-	2.0	-	2.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.6	-	2.2	-	2.2	-	ns
C _{PD}	power dissipation capacitance	f = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 0.8 V	-	1.6	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	1.7	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	1.8	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	1.9	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	2.3	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	2.7	-	-	-	-	-	pF

- [1] All typical values are measured at nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11.1. Waveforms and test circuit

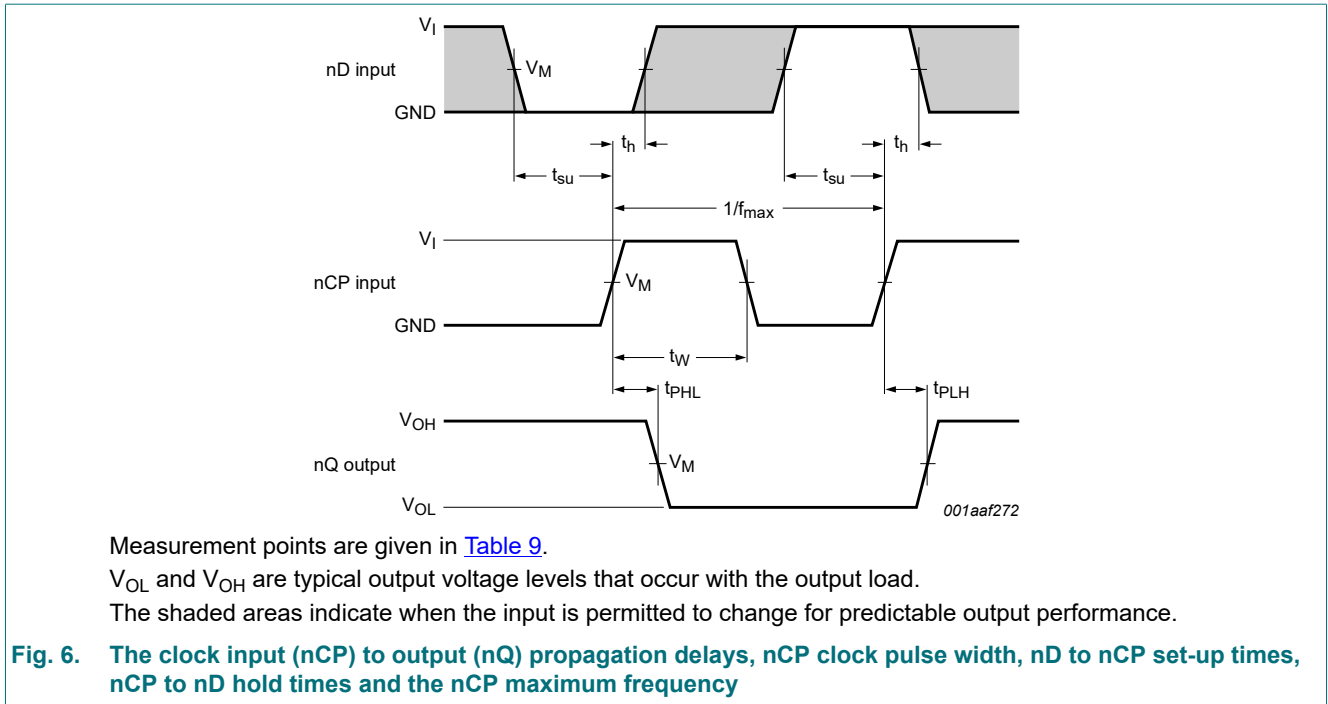
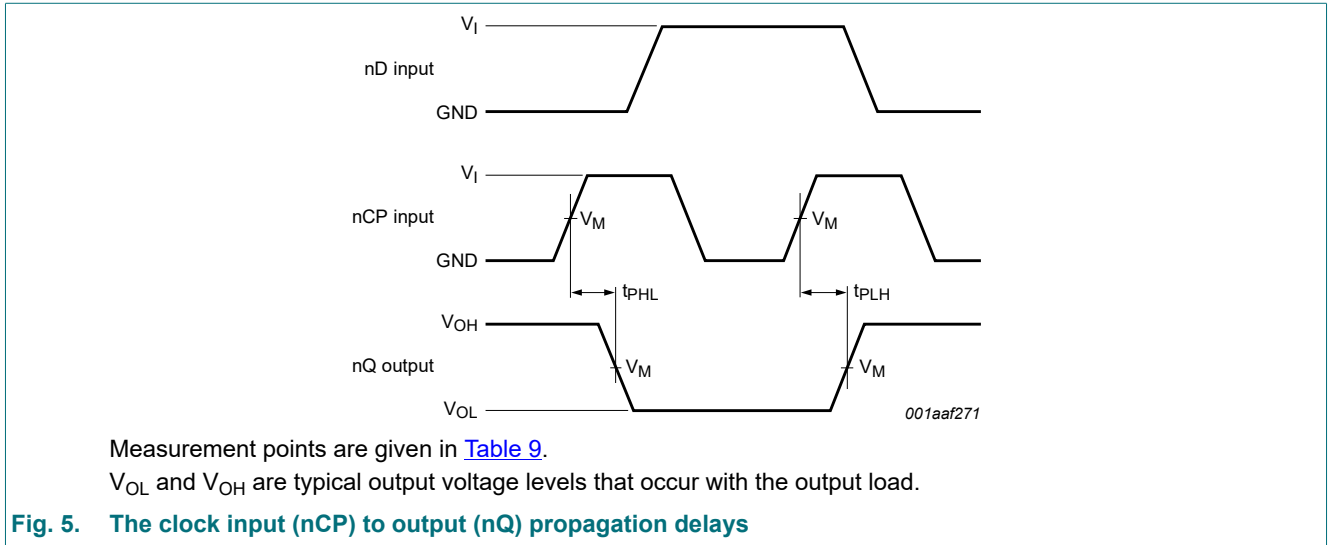
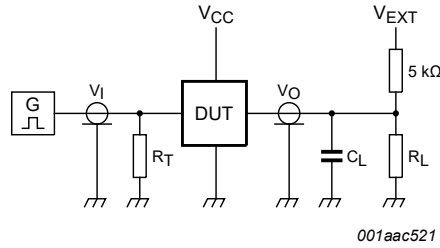


Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage		Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$	

[1] For measuring enable and disable times $R_L = 5 \text{ k}\Omega$.

For measuring propagation delays, set-up and hold times and pulse width $R_L = 1 \text{ M}\Omega$.

12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

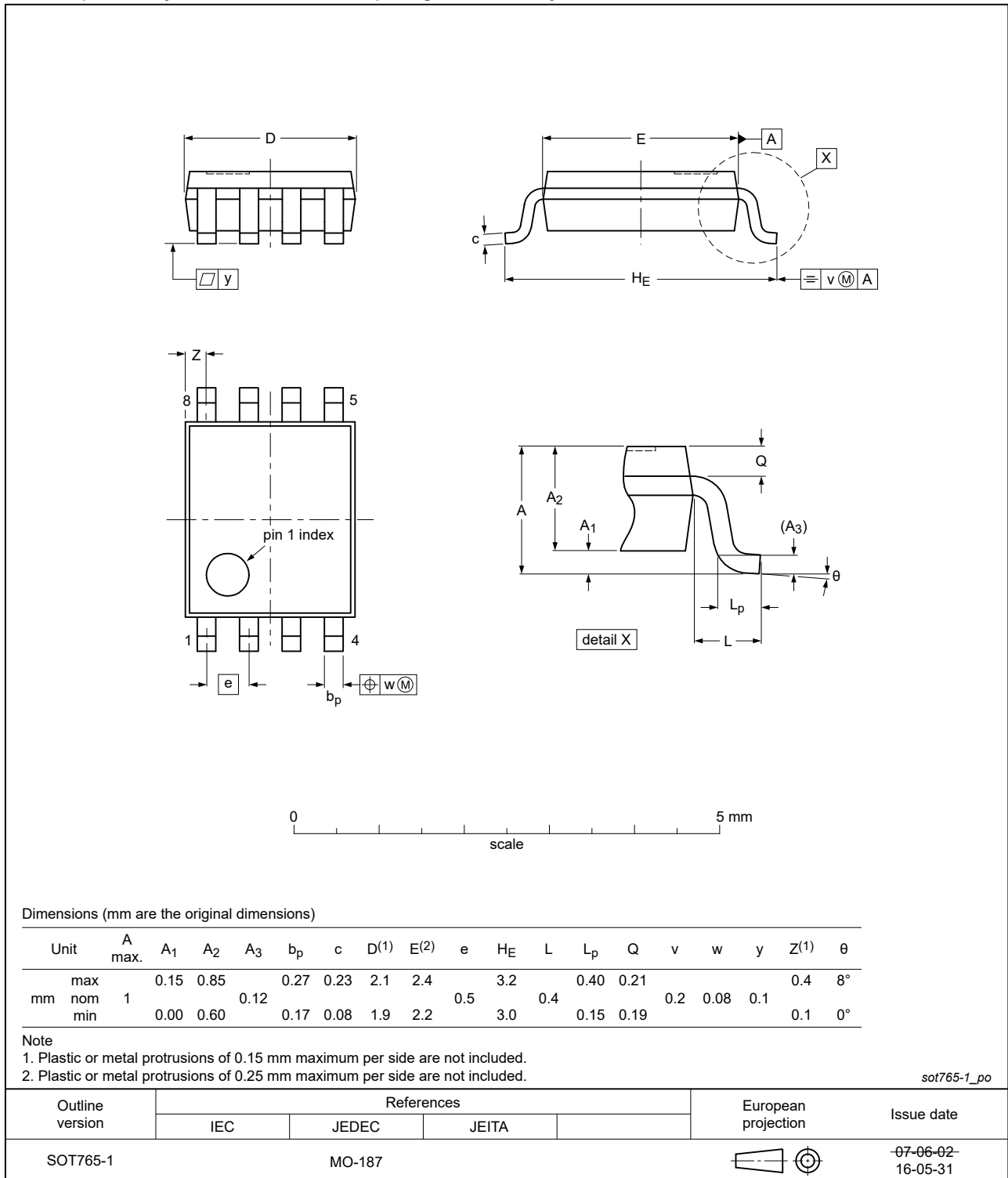


Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G79_Q100 v.4	20230718	Product data sheet	-	74AUP2G79_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74AUP2G79_Q100 v.3	20201203	Product data sheet	-	74AUP2G79_Q100 v.2
Modifications:	<ul style="list-style-type: none"> Table 5: Derating values for P_{tot} total power dissipation have been updated. 			
74AUP2G79_Q100 v.2	20190327	Product data sheet	-	74AUP2G79_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Package outline drawing SOT765-1 (VSSOP8) updated. 			
74AUP2G79_Q100 v.1	20130611	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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