

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

Synchronous Presetable Binary Counter

The MC74AC161/74ACT161 and MC74AC163/74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presetable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters.

The MC74AC161/74ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC163/74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- 'ACT161 and 'ACT163 Have TTL Compatible Inputs
- These are Pb-Free Devices

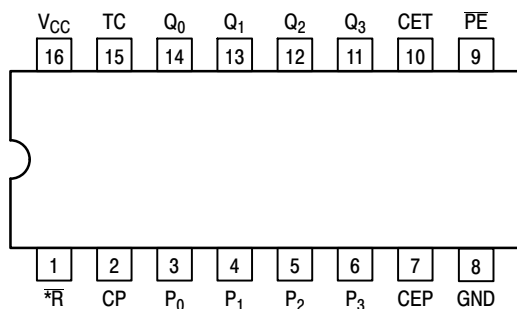


Figure 1. Pinout: 16-Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

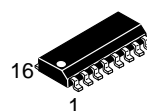
PIN	FUNCTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
\overline{MR}	('161) Asynchronous Master Reset Input
\overline{SR}	('163) Synchronous Reset Input
P ₀ -P ₃	Parallel Data Inputs
\overline{PE}	Parallel Enable Input
Q ₀ -Q ₃	Flip-Flop Outputs
TC	Terminal Count Output



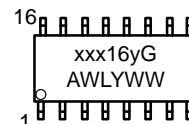
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM



SOIC-16
D SUFFIX
CASE 751B



xxx = AC or ACT
y = 1 or 3
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

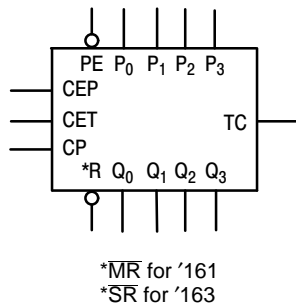


Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC161/ACT161 and MC74AC163/ACT163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('161), synchronous reset ('163), parallel load, count-up and hold. Five control inputs – Master Reset (\overline{MR} , '161), Synchronous Reset (\overline{SR} , '163), Parallel Enable (\overline{PE}), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – determine the mode of

operation, as shown in the Mode Select Table. A LOW signal on \overline{MR} overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \overline{SR} overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on \overline{PE} overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With \overline{PE} and \overline{MR} ('161) or \overline{SR} ('163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC161/ACT161 and MC74AC163/ACT163 use D-type edge-triggered flip-flops and changing the \overline{SR} , \overline{PE} , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations:

$$\text{Count Enable} = \text{CEP} \cdot \text{CET} \cdot \overline{\text{PE}}$$

$$\text{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \text{CET}$$

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge ()
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '163 only
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

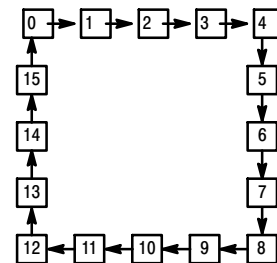
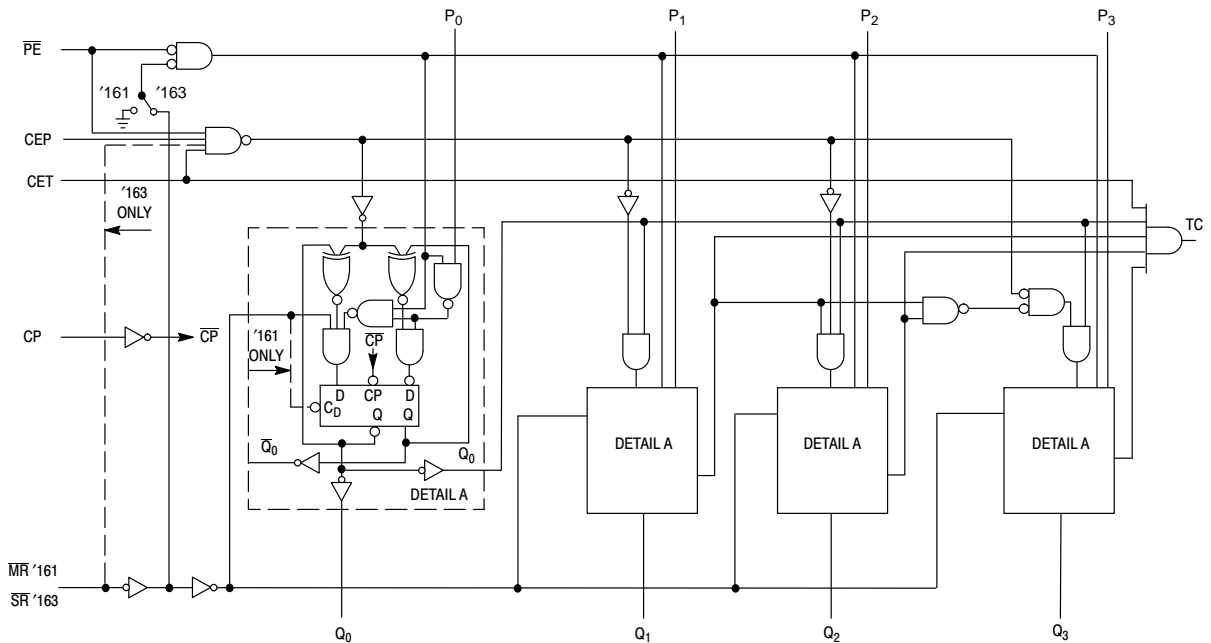


Figure 3. State Diagram

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 4. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq V_{CC} + 0.5$	V
V_O	DC Output Voltage (Note 1)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 50	mA
I_O	DC Output Sink/Source Current	± 50	mA
I_{CC}	DC Supply Current per Output Pin	± 50	mA
I_{GND}	DC Ground Current per Output Pin	± 50	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction temperature under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2)	69.1	°C/W
P_D	Power Dissipation in Still Air at 65°C (Note 3)	500	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 4) Machine Model (Note 5) Charged Device Model (Note 6)	V
$I_{Latch-Up}$	Latch-Up Performance Above V_{CC} and Below GND at 85°C (Note 7)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51-7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/°C from 65°C to 85°C.
4. Tested to EIA/JESD22-A114-A.
5. Tested to EIA/JESD22-A115-A.
6. Tested to JESD22-C101-A.
7. Tested to EIA/JESD78.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V _{CC}	V	
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	–	ns/V
		V _{CC} @ 4.5 V	–	40	–	
		V _{CC} @ 5.5 V	–	25	–	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	–	ns/V
		V _{CC} @ 5.5 V	–	8.0	–	
T _J	Junction Temperature (PDIP)	–	–	140	°C	
T _A	Operating Ambient Temperature Range	–40	25	85	°C	
I _{OH}	Output Current – High	–	–	–24	mA	
I _{OL}	Output Current – Low	–	–	24	mA	

- V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Unit	Conditions	
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0	–	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
			4.5	–	3.86	3.76		
			5.5	–	4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0	–	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
			4.5	–	0.36	0.44		
			5.5	–	0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	–	–	–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC161			74AC161		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0	70 110	111 167	– –	60 95	– –	MHz	3–3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.0 5.0	12.0 9.0	1.5 1.0	13.5 9.5	ns	3–6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	1.5 1.5	7.0 5.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3–6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.0 6.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3–6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	8.5 6.5	14.0 11.0	2.5 2.0	15.5 11.5	ns	3–6
t _{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	5.5 3.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3–6
t _{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	6.5 5.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3–6
t _{PHL}	Propagation Delay MR to Q _n	3.3 5.0	2.0 1.5	6.0 5.5	12.0 9.5	1.5 1.5	13.5 10.0	ns	3–6
t _{PHL}	Propagation Delay MR to TC	3.3 5.0	3.5 2.5	10.0 8.5	15.0 13.0	3.0 2.5	17.5 13.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC163			74AC163		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0	70 110	95 140	– –	60 95	– –	MHz	3–3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.5 1.0	13.5 9.5	ns	3–6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3–6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3–6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	2.5 2.0	15.5 11.5	ns	3–6
t _{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3–6
t _{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC161		74ACT161		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	3.3	6.0	13.5	16.0	ns	3-9	
		5.0	3.5	8.5	10.5			
t _h	Hold Time, HIGH or LOW P _n to CP	3.3	-7.0	-1.0	-0.5	ns	3-9	
		5.0	-4.0	0	0			
t _s	Setup Time, HIGH or LOW PE to CP	3.3	6.5	11.5	14.0	ns	3-9	
		5.0	4.0	7.5	8.5			
t _h	Hold Time, HIGH or LOW PE to CP	3.3	-6.0	0	0	ns	3-9	
		5.0	-3.5	0.5	1.0			
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3	3.0	6.0	7.0	ns	3-9	
		5.0	2.0	4.5	5.0			
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3	-3.5	0	0	ns	3-9	
		5.0	-2.0	0	0.5			
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3	2.0	3.5	4.0	ns	3-6	
		5.0	2.0	2.5	3.0			
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3	2.0	4.0	4.5	ns	3-6	
		5.0	2.0	3.0	3.5			
t _w	MR Pulse Width, LOW	3.3	3.0	5.5	7.5	ns	3-6	
		5.0	2.5	4.5	6.0			
t _{rec}	Recovery Time MR to CP	3.3	-2.0	-0.5	0	ns	3-9	
		5.0	-1.0	0	0.5			

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC163		74ACT163		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	3.3	5.5	13.5	16.0	ns	3-9	
		5.0	4.0	8.5	10.5			
t _h	Hold Time, HIGH or LOW P _n to CP	3.3	-7.0	-1.0	-0.5	ns	3-9	
		5.0	-5.0	0	0			
t _s	Setup Time, HIGH or LOW SR to CP	3.3	5.5	14	16.5	ns	3-9	
		5.0	4.0	9.5	11.0			
t _h	Hold Time, HIGH or LOW SR to CP	3.3	-7.5	-1.0	-0.5	ns	3-9	
		5.0	-5.5	-0.5	0			
t _s	Setup Time, HIGH or LOW PE to CP	3.3	5.5	11.5	14.0	ns	3-9	
		5.0	4.0	7.5	8.5			
t _h	Hold Time, HIGH or LOW PE to CP	3.3	-7.5	-1.0	-0.5	ns	3-9	
		5.0	-5.0	-0.5	0			
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3	3.5	6.0	7.0	ns	3-9	
		5.0	2.5	4.5	5.0			
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3	-4.5	0	0	ns	3-9	
		5.0	-3.0	0	0.5			
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3	3.0	3.5	4.0	ns	3-6	
		5.0	2.0	2.5	3.0			
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3	3.0	4.0	4.5	ns	3-6	
		5.0	2.0	3.0	3.5			

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA	
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA	
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	-	-	-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT161			74ACT161		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	115	125	–	100	–	MHz	3–3
t _{PLH}	Propagation Delay CP to Q _n (\overline{PE} Input HIGH or LOW)	5.0	1.5	8.0	9.5	1.5	10.5	ns	3–6
t _{PHL}	Propagation Delay CP or Q _n (\overline{PE} Input HIGH or LOW)	5.0	1.5	8.0	10.5	1.5	11.5	ns	3–6
t _{PLH}	Propagation Delay CP to TC	5.0	2.0	11.0	11.0	1.5	12.5	ns	3–6
t _{PHL}	Propagation Delay CP to TC	5.0	1.5	11.0	12.5	1.5	13.5	ns	3–6
t _{PLH}	Propagation Delay CET to TC	5.0	1.5	7.5	8.5	1.5	10.0	ns	3–6
t _{PHL}	Propagation Delay CET to TC	5.0	1.5	8.0	9.5	1.5	10.5	ns	3–6
t _{PHL}	Propagation Delay \overline{MR} to Q _n	5.0	1.5	8.0	10.0	1.5	11.0	ns	3–6
t _{PHL}	Propagation Delay \overline{MR} to TC	5.0	2.5	10.0	13.5	2.0	14.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT163			74ACT163		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	120	140	–	105	–	MHz	3–3
t _{PLH}	Propagation Delay CP to Q _n (\overline{PE} Input HIGH or LOW)	5.0	1.5	5.5	10.0	1.5	11.0	ns	3–6
t _{PHL}	Propagation Delay CP to Q _n (\overline{PE} Input HIGH or LOW)	5.0	1.5	6.0	11.0	1.5	12.0	ns	3–6
t _{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5	2.0	13.5	ns	3–6
t _{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5	2.0	15.0	ns	3–6
t _{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0	1.5	10.5	ns	3–6
t _{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0	2.0	11.0	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT161		74ACT161		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	5.0	7.0	9.5	11.5	ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to CP	5.0	-3.0	0	0	ns	3-9	
t _s	Setup Time, HIGH or LOW PE to CP	5.0	6.0	8.5	9.5	ns	3-9	
t _h	Hold Time, HIGH or LOW PE to CP	5.0	-3.5	-0.5	-0.5	ns	3-9	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	4.0	5.5	6.5	ns	3-9	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-2.0	0	0	ns	3-9	
t _w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3-6	
t _w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3-6	
t _w	MR Pulse Width, LOW	5.0	3.0	3.0	7.5	ns	3-6	
t _{rec}	Recovery Time MR to CP	5.0	0	0	0.5	ns	3-9	

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT163		74ACT163		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	5.0	4.0	10.0	12.0	ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to CP	5.0	-5.0	0.5	0.5	ns	3-9	
t _s	Setup Time, HIGH or LOW SR to CP	5.0	4.0	10.0	11.5	ns	3-9	
t _h	Hold Time, HIGH or LOW SR to CP	5.0	-5.5	-0.5	-0.5	ns	3-9	
t _s	Setup Time, HIGH or LOW PE to CP	5.0	4.0	8.5	10.5	ns	3-9	
t _h	Hold Time, HIGH or LOW PE to CP	5.0	-5.5	-0.5	0	ns	3-9	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3-9	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0	0.5	ns	3-9	
t _w	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6	
t _w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6	

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

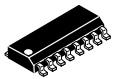
Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V

ORDERING INFORMATION

Device	Package	Shipping†
MC74AC161DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74AC161DR2G		2500 / Tape & Reel
MC74ACT161DG		48 Units / Rail
MC74ACT161DR2G		2500 / Tape & Reel
MC74AC163DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74AC163DR2G		2500 / Tape & Reel
MC74ACT163DG		48 Units / Rail
MC74ACT163DR2G		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

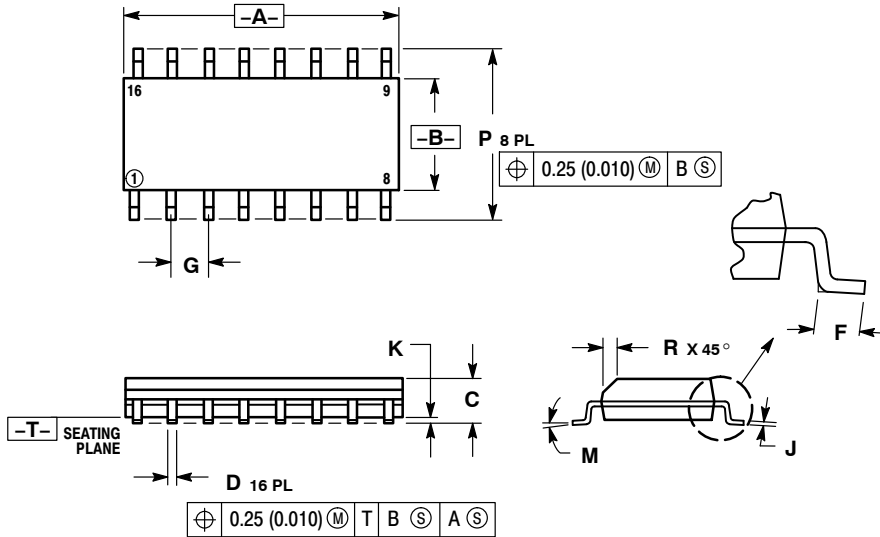
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-16
CASE 751B-05
ISSUE K

DATE 29 DEC 2006



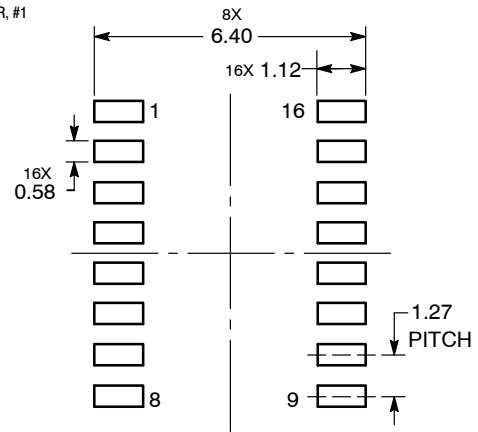
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

