

## 2.3 GHz Dual Integrated DCL with PPMU, Level Setting DACs, and On-Chip Calibration Registers

### FEATURES

- ▶ 2.3 GHz, 4.6 Gbps maximum toggle rate
- ▶ DCL disable mode (low leakage typically <5 nA)
- ▶ 2 W power dissipation per channel (high voltage driver active)
- ▶ Integrated 16-bit DACs with offset and gain correction
- ▶ High voltage driver
  - ▶ 3-level driver with high-Z and reflection clamps
  - ▶ Voltage range: -1.5 V to +7.0 V
  - ▶ Precision trimmed output resistance
  - ▶ Functional amplitude ( $V_{IH} - V_{IL}$ , unterminated swing): 0.05 V (minimum) to 8.5 V (maximum)
  - ▶ 400 ps minimum pulse width, 2.0 V programmed swing
  - ▶ 25 ps deterministic jitter, 1 ps random jitter
- ▶ Low voltage driver
  - ▶ Multilevel voltage range: -1.5 V to +6.5 V
  - ▶ Terminated swings of 25 mV p-p to 600 mV p-p into 50  $\Omega$
  - ▶ 215 ps minimum pulse width, 1.2 V programmed swing
  - ▶ 20 ps deterministic jitter, 1 ps random jitter
- ▶ Comparator
  - ▶ Normal window (NWC), differential mode (DMC), and zero-crossing (ZCC)
  - ▶ Voltage range: -1.5 V to +6.5 V
  - ▶ <60 ps ERT/EFT NWC 1.0V, terminated
- ▶ Active load:  $\pm 25$  mA current range
- ▶ Per pin PPMU
  - ▶ Force voltage and compliance range: -1.5 V to +6.5 V
  - ▶ 5 current ranges (Range A to Range E)
    - ▶  $\pm 60$  mA,  $\pm 1$  mA,  $\pm 100$   $\mu$ A,  $\pm 10$   $\mu$ A, and  $\pm 2$   $\mu$ A
  - ▶ Dedicated go/no go comparators
- ▶ DC levels
  - ▶ Fully integrated and dedicated 16-bit DACs
  - ▶ On-chip gain and offset calibration registers with automatic add/multiply function
- ▶ On-chip temperature sensor, OVD alarms, temperature alarm, and relay driver functions
- ▶ 9 mm  $\times$  9 mm, 121-ball CSP\_BGA

### APPLICATIONS

- ▶ ATE
- ▶ Semiconductor and board test systems
- ▶ Instrumentation and characterization equipment

### GENERAL DESCRIPTION

The ADATE334 is a complete dual-channel automatic test equipment (ATE) solution that performs the pin electronics functions of a driver, comparator, and active load (DCL), and a four-quadrant per pin parametric measurement unit (PPMU). Dedicated, 16-bit DACs with on-chip calibration registers provide all necessary dc levels for device operation.

The high voltage driver features three active states: high mode, low mode, and terminate mode, as well as a high impedance inhibit state. The inhibit state, in conjunction with the integrated dynamic clamps, facilitates significant attenuation of transmission line reflections when the driver is not actively terminating the line. The open-circuit drive capability is -1.5 V to +7.0 V to accommodate a wide range of ATE and instrumentation applications.

The low voltage driver, working in conjunction with the high voltage driver, can provide 25 mV p-p to 600 mV p-p signals at up to 4.6 Gbps in a 50  $\Omega$  environment.

The ADATE334 can be used either as a dual, single-ended pin electronics channel or as a single differential channel. In addition to per-channel, high speed window comparators, the ADATE334 provides a programmable threshold differential comparator for differential ATE applications and a zero-crossing comparator.

All dc levels for DCL and PPMU functions are generated by dedicated, on-chip, 16-bit DACs. To facilitate accurate level programming, the ADATE334 includes an integrated calibration function that corrects gain and offset errors of each functional block. Correction coefficients can be stored on-chip, and any values written to the DACs automatically adjust using the appropriate correction factors.

The ADATE334 uses a serial programmable interface (SPI) bus to program all functional blocks, DACs, and on-chip calibration constants. The ADATE334 has an on-chip temperature sensor to monitor temperature and overvoltage and undervoltage alarms that monitor and report any output pin or transient PPMU voltage faults that can occur during operation. The ADATE334 also provides a per channel, open-drain relay driver.

For more information on the ADATE334, contact [ADATE334@analog.com](mailto:ADATE334@analog.com).

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. SpB

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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