TW6874

Quad (SD/HD) SDI Receiver with Adaptive Equalizer, VC-2 Decoder and Audio CODEC

FN8430
Rev 1.00
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The TW6874 is a quad (SD/HD) SDI receiver. It has four independent channels, each consisting of an adaptive equalizer, clock data recovery, audio decoder and VC-2 decompression engine. Each channel receives high speed serial data over extended coaxial cable lengths and deserialize the data into video/audio streams for the back-end device.

The video streams are output as: 8-bit BT.656 for SD; BT.1120 in 8/16 bit mode for HD. The audio streams are output through an I2S audio digital interface in a multichannel interleaving format. In addition to the extraction of embedded SDI audio, the TW6874 incorporates a 5-channel audio ADC decoder to decode analog audio inputs and output them through the same I2S interface.

A visually lossless VC-2 (Dirac) compression/decompression engine is implemented in the TW6872/TW6874 SDI Tx/Rx pair to extend the reach of HD-SDI to that of SD-SDI. An interrupt pin can be used to signal the host processor of ancillary data packet detection. Finally, integrated audio test patterns and PRBS checker ease system design and implementation.

Applications

- SD/HD DVR

Features

- Quad (SD/HD) SDI receiver for standard (SD) and high (HD) definition 10-bit component video
- Automatic SDI detection of SMPTE 259M Level C (SD-SDI), SMPTE ST 292 (1.5G SDI) signals
- Each SDI input standard supported with ITU-R BT.656 (SD) or ITU-R BT.1120 (1.5G) interface
- Converts 10-bit serial digital component video input to 8-bit parallel video output
- Adaptive equalizer/clock data recovery/VC-2 decompression engine for each channel
- 4 separate video output ports with BT.656/BT.1120 output format
- 5-channel audio ADC (Analog-to-Digital Converter)
- Single multiplexed audio output DAC (Digital-to-Analog Converter)
- Supports I2S master/slave interface for record output and playback input with cascade
- I^2C and SPI interface
- Pb-free (RoHS compliant) 256 ball LFBGA

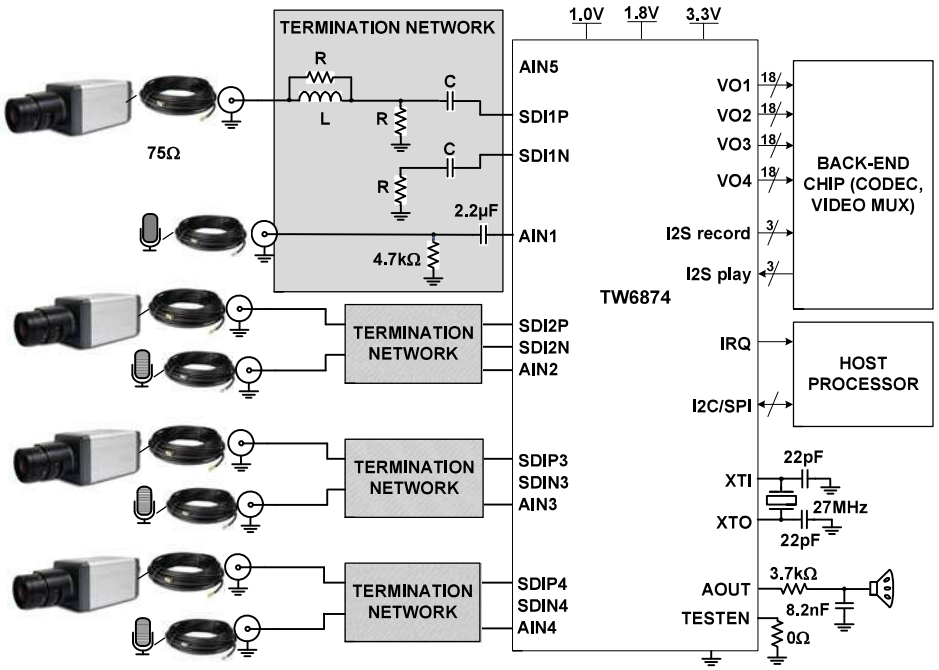

FIGURE 1. TW6874 TYPICAL APPLICATION

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Block Diagram

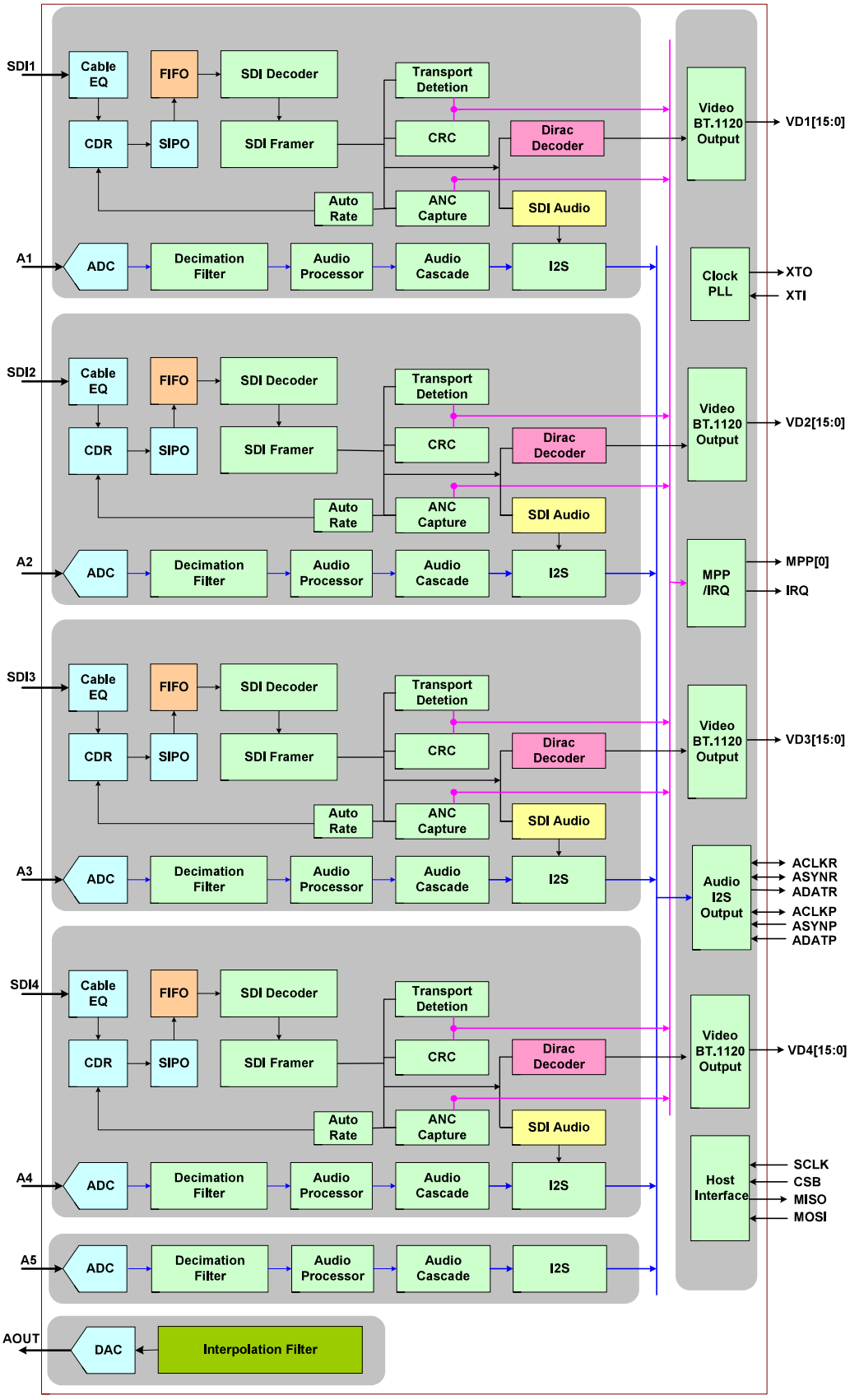


FIGURE 2. BLOCK DIAGRAM

Pin Configuration

TW6874
(256 BALL 13.5mmx13.5mm LFBGA)
TOP VIEW

Analog Power

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	AVSS_CDR1	AVDD_CDR1	AVSS_PLL18	DNC	DNC	DNC	XTO	AVDD_MISC18	AVDD_GUARD	SPIB	DNC	ASYNP	DNC	TESTEN	MOSI_SDA	ADATR
B	SDIP1	DNC	AVDD_PLL18	DNC	DNC	DNC	XTI	AVSS_MISC18	AVSS_GUARD	DNC	ALINKI	DNC	MISO_ADDR1	ACLKR	SCL	ALINKO
C	SDIN1	AVSS_EQ	AVDD_PLL10	AVSS_TST1	AVDD_TST1	AVSS_ESD	AVDD_XTAL	AVDD_MISC10	DNC	ADATP	ACLKP	DNC	RSTB	DNC	VD1_14	VD1_12
D	AVDD_REG1	AVSS_REG1	AVSS_PLL10	AVSS_EQ	AVSS_ESD	AVSS_ESD	AVSS_XTAL	AVSS_MISC10	DNC	MPP0	CSB_ADDR0	IRQ	ASYNR	VD1_13	VD1_10	VD1_8
E	AVDD_REG2	AVSS_REG2	AVSS_EQ	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDE	DVDDE	DVDDE	DVDDE	DVDDE	DVDDI	VD1_15	VD1_11	CLKN1	CLKP1
F	SDIN2	AVSS_EQ	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDE	DVDDE	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_9	VD1_7	VD1_6	VD1_4
G	SDIP2	DNC	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDE	DVDDE	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_5	VD1_3	VD1_2	VD1_1
H	AVDD_CDR2	AVSS_CDR2	AVDD_BG	AVSS_ESD	AVSS_ESD	AVSS_ESD	DVSS	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_0	VD2_14	VD2_13	VD2_15
J	AVDD_CDR3	AVSS_CDR3	AVSS_BG	AVSS_ESD	AVSS_ESD	AVSS_ESD	DVSS	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_10	VD2_8	VD2_12	VD2_11
K	SDIP3	DNC	AVSS_EQ	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDI	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_4	VD2_6	VD2_9	CLKN2
L	SDIN3	AVSS_EQ	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDI	DVDDI	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_1	VD2_3	VD2_7	CLKP2
M	AVDD_REG3	AVSS_REG3	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDI	DVDDI	DVDDI	DVDDI	DVDDI	DVDDI	DVDDE	VD3_13	VD3_15	VD2_2	VD2_5
N	AVDD_REG4	AVSS_REG4	AVSS_TST4	AVSS_DAC	AOUT	AIN1	AVSS_FPLL18	ADCREF	VD4_5	VD4_8	VD4_12	VD3_2	VD3_9	VD3_11	VD3_12	VD2_0
P	SDIN4	AVSS_EQ	AVDD_TST4	AVDD_DAC	AIN2	AIN5	AVDD_FPLL18	VD4_1	VD4_3	VD4_7	VD4_10	VD4_14	VD3_0	VD3_7	VD3_10	VD3_14
R	SDIP4	DNC	DNC	DNC	AIN3	AVSS_AFE	AVSS_FPLL10	VD4_0	VD4_4	CLKN4	VD4_11	VD4_15	VD3_3	VD3_4	CLKN3	CLKP3
T	AVSS_CDR4	AVDD_CDR4	DNC	DNC	AIN4	AVDD_AFE	AVDD_FPLL10	VD4_2	VD4_6	CLKP4	VD4_9	VD4_13	VD3_1	VD3_5	VD3_6	VD3_8

: Analog 1.0V
: Analog 1.8V
: Analog ground
: VDD/VSS pair

Pin Configuration (Continued)

TW6874
(256 BALL 13.5mmx13.5mm LFBGA)
TOP VIEW

Digital Power

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	AVSS_CDR1	AVDD_CDR1	AVSS_PLL18	DNC	DNC	DNC	XTO	AVDD_MISC18	AVDD_GUARD	SPIB	DNC	ASYNP	DNC	TESTEN	MOSI_SDA	ADATR
B	SDIP1	DNC	AVDD_PLL18	DNC	DNC	DNC	XTI	AVSS_MISC18	AVSS_GUARD	DNC	ALINKI	DNC	MISO_ADDR1	ACLKR	SCL	ALINKO
C	SDIN1	AVSS_EQ	AVDD_PLL10	AVSS_TST1	AVDD_TST1	AVSS_ESD	AVDD_XTAL	AVDD_MISC10	DNC	ADATP	ACLKP	DNC	RSTB	DNC	VD1_14	VD1_12
D	AVDD_REG1	AVSS_REG1	AVSS_PLL10	AVSS_EQ	AVSS_ESD	AVSS_ESD	AVSS_XTAL	AVSS_MISC10	DNC	MPP0	CSB_ADDR0	IRQ	ASYNR	VD1_13	VD1_10	VD1_8
E	AVDD_REG2	AVSS_REG2	AVSS_EQ	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDE	DVDDE	DVDDE	DVDDE	DVDDE	DVDDI	VD1_15	VD1_11	CLKN1	CLKP1
F	SDIN2	AVSS_EQ	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDE	DVDDE	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_9	VD1_7	VD1_6	VD1_4
G	SDIP2	DNC	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDE	DVDDE	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_5	VD1_3	VD1_2	VD1_1
H	AVDD_CDR2	AVSS_CDR2	AVDD_BG	AVSS_ESD	AVSS_ESD	AVSS_ESD	DVSS	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_0	VD2_14	VD2_13	VD2_15
J	AVDD_CDR3	AVSS_CDR3	AVSS_BG	AVSS_ESD	AVSS_ESD	AVSS_ESD	DVSS	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_10	VD2_8	VD2_12	VD2_11
K	SDIP3	DNC	AVSS_EQ	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDI	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_4	VD2_6	VD2_9	CLKN2
L	SDIN3	AVSS_EQ	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDI	DVDDI	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_1	VD2_3	VD2_7	CLKP2
M	AVDD_REG3	AVSS_REG3	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDI	DVDDI	DVDDI	DVDDI	DVDDI	DVDDI	DVDDE	VD3_13	VD3_15	VD2_2	VD2_5
N	AVDD_REG4	AVSS_REG4	AVSS_TST4	AVSS_DAC	AOUT	AIN1	AVSS_FPLL18	ADCREF	VD4_5	VD4_8	VD4_12	VD3_2	VD3_9	VD3_11	VD3_12	VD2_0
P	SDIN4	AVSS_EQ	AVDD_TST4	AVDD_DAC	AIN2	AIN5	AVDD_FPLL18	VD4_1	VD4_3	VD4_7	VD4_10	VD4_14	VD3_0	VD3_7	VD3_10	VD3_14
R	SDIP4	DNC	DNC	DNC	AIN3	AVSS_AFE	AVSS_FPLL10	VD4_0	VD4_4	CLKN4	VD4_11	VD4_15	VD3_3	VD3_4	CLKN3	CLKP3
T	AVSS_CDR4	AVDD_CDR4	DNC	DNC	AIN4	AVDD_AFE	AVDD_FPLL10	VD4_2	VD4_6	CLKP4	VD4_9	VD4_13	VD3_1	VD3_5	VD3_6	VD3_8

: Digital 1.0V
: Digital 3.3V
: Digital ground

Pin Configuration (Continued)

TW6874
(256 BALL 13.5mmx13.5mm LFBGA)
TOP VIEW

Signals

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	AVSS_CDR1	AVDD_CDR1	AVSS_PLL18	DNC	DNC	DNC	XTO	AVDD_MISC18	AVDD_GUARD	SPIB	DNC	ASYNP	DNC	TESTEN	MOSI_SDA	ADATR
B	SDIP1	DNC	AVDD_PLL18	DNC	DNC	DNC	XTI	AVSS_MISC18	AVSS_GUARD	DNC	ALINKI	DNC	MISO_ADDR1	ACLKR	SCL	ALINKO
C	SDIN1	AVSS_EQ	AVDD_PLL10	AVSS_TST1	AVDD_TST1	AVSS_ESD	AVDD_XTAL	AVDD_MISC10	DNC	ADATP	ACLKP	DNC	RSTB	DNC	VD1_14	VD1_12
D	AVDD_REG1	AVSS_REG1	AVSS_PLL10	AVSS_EQ	AVSS_ESD	AVSS_ESD	AVSS_XTAL	AVSS_MISC10	DNC	MPP0	CSB_ADDR0	IRQ	ASYNR	VD1_13	VD1_10	VD1_8
E	AVDD_REG2	AVSS_REG2	AVSS_EQ	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDE	DVDDE	DVDDE	DVDDE	DVDDE	DVDDI	VD1_15	VD1_11	CLKN1	CLKP1
F	SDIN2	AVSS_EQ	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDE	DVDDE	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_9	VD1_7	VD1_6	VD1_4
G	SDIP2	DNC	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDE	DVDDE	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_5	VD1_3	VD1_2	VD1_1
H	AVDD_CDR2	AVSS_CDR2	AVDD_BG	AVSS_ESD	AVSS_ESD	AVSS_ESD	DVSS	DVSS	DVSS	DVSS	DVSS	DVDDI	VD1_0	VD2_14	VD2_13	VD2_15
J	AVDD_CDR3	AVSS_CDR3	AVSS_BG	AVSS_ESD	AVSS_ESD	AVSS_ESD	DVSS	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_10	VD2_8	VD2_12	VD2_11
K	SDIP3	DNC	AVSS_EQ	AVSS_EQ	AVSS_ESD	AVSS_ESD	DVDDI	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_4	VD2_6	VD2_9	CLKN2
L	SDIN3	AVSS_EQ	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDI	DVDDI	DVSS	DVSS	DVSS	DVSS	DVDDE	VD2_1	VD2_3	VD2_7	CLKP2
M	AVDD_REG3	AVSS_REG3	AVSS_EQ	AVSS_EQ	AVSS_ESD	DVDDI	DVDDI	DVDDI	DVDDI	DVDDI	DVDDI	DVDDE	VD3_13	VD3_15	VD2_2	VD2_5
N	AVDD_REG4	AVSS_REG4	AVSS_TST4	AVSS_DAC	AOUT	AIN1	AVSS_FPLL18	ADCREF	VD4_5	VD4_8	VD4_12	VD3_2	VD3_9	VD3_11	VD3_12	VD2_0
P	SDIN4	AVSS_EQ	AVDD_TST4	AVDD_DAC	AIN2	AIN5	AVDD_FPLL18	VD4_1	VD4_3	VD4_7	VD4_10	VD4_14	VD3_0	VD3_7	VD3_10	VD3_14
R	SDIP4	DNC	DNC	DNC	AIN3	AVSS_AFE	AVSS_FPLL10	VD4_0	VD4_4	CLKN4	VD4_11	VD4_15	VD3_3	VD3_4	CLKN3	CLKP3
T	AVSS_CDR4	AVDD_CDR4	DNC	DNC	AIN4	AVDD_AFE	AVDD_FPLL10	VD4_2	VD4_6	CLKP4	VD4_9	VD4_13	VD3_1	VD3_5	VD3_6	VD3_8

: Analog SDI input signals
: Analog audio I/O signals
: X-tal I/O pins
: DNC & Misc pins

: CH1 digital output port
: CH2 digital output port
: CH3 digital output port
: CH4 digital output port

Pin Descriptions

PIN LOCATION	PIN NAME	TYPE	DESCRIPTION
B1	SDIP1	Analog Input	SDI input for channel 1. Terminate with 75Ω to ground and AC-couple with 1µF.
C1	SDIN1	Analog Input	Inverting SDI input for channel 1. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin.
G1	SDIP2	Analog Input	SDI input for channel 2. Terminate with 75Ω to ground and AC-couple with 1µF.
F1	SDIN2	Analog Input	Inverting SDI input for channel 2. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin.
K1	SDIP3	Analog Input	SDI input for channel 3. Terminate with 75Ω to ground and AC-couple with 1µF.
L1	SDIN3	Analog Input	Inverting SDI input for channel 3. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin.
R1	SDIP4	Analog Input	SDI input for channel 4. Terminate with 75Ω to ground and AC-couple with 1µF.
P1	SDIN4	Analog Input	Inverting SDI input for channel 4. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin.
N6	AIN1	Analog Input	Audio input for channel 1. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF.
P5	AIN2	Analog Input	Audio input for channel 2. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF.
R5	AIN3	Analog Input	Audio input for channel 3. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF.
T5	AIN4	Analog Input	Audio input for channel 4. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF.
P6	AIN5	Analog Input	Audio input for channel 5. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF.
N8	ADCREF	Analog Input	Audio ADC reference. Terminate with 2.2µF to ground. Do not connect external audio signal to this pin.
N5	AOUT	Analog Output	Analog audio output.
H13	VD1_0	Digital Output	Video data output for channel 1.
G16	VD1_1	Digital Output	Video data output for channel 1.
G15	VD1_2	Digital Output	Video data output for channel 1.
G14	VD1_3	Digital Output	Video data output for channel 1.
F16	VD1_4	Digital Output	Video data output for channel 1.
G13	VD1_5	Digital Output	Video data output for channel 1.
F15	VD1_6	Digital Output	Video data output for channel 1.
F14	VD1_7	Digital Output	Video data output for channel 1.
D16	VD1_8	Digital Output	Video data output for channel 1.
F13	VD1_9	Digital Output	Video data output for channel 1.
D15	VD1_10	Digital Output	Video data output for channel 1.
E14	VD1_11	Digital Output	Video data output for channel 1.
C16	VD1_12	Digital Output	Video data output for channel 1.
D14	VD1_13	Digital Output	Video data output for channel 1.
C15	VD1_14	Digital Output	Video data output for channel 1.
E13	VD1_15	Digital Output	Video data output for channel 1.
E16	CLKP1	Digital Output	Reserved
E15	CLKN1	Digital Output	Clock for VD1.
N16	VD2_0	Digital Output	Video data output for channel 2.

Pin Descriptions (Continued)

PIN LOCATION	PIN NAME	TYPE	DESCRIPTION
L13	VD2_1	Digital Output	Video data output for channel 2.
M15	VD2_2	Digital Output	Video data output for channel 2.
L14	VD2_3	Digital Output	Video data output for channel 2.
K13	VD2_4	Digital Output	Video data output for channel 2.
M16	VD2_5	Digital Output	Video data output for channel 2.
K14	VD2_6	Digital Output	Video data output for channel 2.
L15	VD2_7	Digital Output	Video data output for channel 2.
J14	VD2_8	Digital Output	Video data output for channel 2.
K15	VD2_9	Digital Output	Video data output for channel 2.
J13	VD2_10	Digital Output	Video data output for channel 2.
J16	VD2_11	Digital Output	Video data output for channel 2.
J15	VD2_12	Digital Output	Video data output for channel 2.
H15	VD2_13	Digital Output	Video data output for channel 2.
H14	VD2_14	Digital Output	Video data output for channel 2.
H16	VD2_15	Digital Output	Video data output for channel 2.
L16	CLKP2	Digital Output	Reserved
K16	CLKN2	Digital Output	Clock for VD2.
P13	VD3_0	Digital Output	Video data output for channel 3.
T13	VD3_1	Digital Output	Video data output for channel 3.
N12	VD3_2	Digital Output	Video data output for channel 3.
R13	VD3_3	Digital Output	Video data output for channel 3.
R14	VD3_4	Digital Output	Video data output for channel 3.
T14	VD3_5	Digital Output	Video data output for channel 3.
T15	VD3_6	Digital Output	Video data output for channel 3.
P14	VD3_7	Digital Output	Video data output for channel 3.
T16	VD3_8	Digital Output	Video data output for channel 3.
N13	VD3_9	Digital Output	Video data output for channel 3.
P15	VD3_10	Digital Output	Video data output for channel 3.
N14	VD3_11	Digital Output	Video data output for channel 3.
N15	VD3_12	Digital Output	Video data output for channel 3.
M13	VD3_13	Digital Output	Video data output for channel 3.
P16	VD3_14	Digital Output	Video data output for channel 3.
M14	VD3_15	Digital Output	Video data output for channel 3.
R16	CLKP3	Digital Output	Reserved
R15	CLKN3	Digital Output	Clock for VD3.
R8	VD4_0	Digital Output	Video data output for channel 4.
P8	VD4_1	Digital Output	Video data output for channel 4.
T8	VD4_2	Digital Output	Video data output for channel 4.
P9	VD4_3	Digital Output	Video data output for channel 4.
R9	VD4_4	Digital Output	Video data output for channel 4.
N9	VD4_5	Digital Output	Video data output for channel 4.

Pin Descriptions (Continued)

PIN LOCATION	PIN NAME	TYPE	DESCRIPTION
T9	VD4_6	Digital Output	Video data output for channel 4.
P10	VD4_7	Digital Output	Video data output for channel 4.
N10	VD4_8	Digital Output	Video data output for channel 4.
T11	VD4_9	Digital Output	Video data output for channel 4.
P11	VD4_10	Digital Output	Video data output for channel 4.
R11	VD4_11	Digital Output	Video data output for channel 4.
N11	VD4_12	Digital Output	Video data output for channel 4.
T12	VD4_13	Digital Output	Video data output for channel 4.
P12	VD4_14	Digital Output	Video data output for channel 4.
R12	VD4_15	Digital Output	Video data output for channel 4.
T10	CLKP4	Digital Output	Reserved
R10	CLKN4	Digital Output	Clock for VD4.
D12	IRQ	Digital Output	Interrupt request.
B11	ALINKI	Digital Input	Serial audio multidevice link input.
B16	ALINKO	Digital Output	Serial audio multidevice link output.
C11	ACLKP	Digital I/O	Serial audio playback clock input/output.
A12	ASYNP	Digital I/O	Serial audio playback sync input/output.
C10	ADATP	Digital Input	Serial audio playback data input.
B14	ACLKR	Digital I/O	Serial audio record clock input/output.
D13	ASYNR	Digital I/O	Serial audio record sync input/output.
A16	ADATR	Digital Output	Serial audio record data output.
A10	SPIB	Digital Input	LO: Enable SPI interface. HI: Enable I^2C interface.
B15	SCL	Digital Input	SPI/I^2C clock input. I^2C interface requires pull-up resistor to DVDDE.
A15	MOSI_SDA	Digital I/O	SPI: Serial data input. I^2C: Serial data I/O. I^2C interface requires pull-up resistor to DVDDE.
B13	MISO_ADDR1	Digital I/O	SPI: Serial data output. I^2C: Bit 1 of slave address select.
D11	CSB_ADDR0	Digital Input	SPI: chip-select. SPI interface is active when LO. I^2C: Bit 0 of slave address select. ADDR1 ADDR0 address LO LO 0x68 LO HI 0x69 HI LO 0x6A HI HI 0x6B
C13	RSTB	Digital Input	Resets device when pulled LO.
A14	TESTEN	Digital Input	For internal use only. Tie LO.
D10	MPP0 (= ADATM)	Digital Output	The ADATM is the serial audio mix data output. The ADATM outputs through the MPP0 pin.
A4, A5, A6, A11, A13, B2, B4, B5, B6, B10, B12, C9, C12, C14, D9, G2, K2, R2, R3, R4, T3, T4	DNC	Do Not Connect	Do not connect anything to these pins.
A7	XTO	Analog Output	27MHz crystal connection.
B7	XTI	Analog Input	27MHz crystal connection or 27MHz/1.0V oscillator input.

Pin Descriptions (Continued)

PIN LOCATION	PIN NAME	TYPE	DESCRIPTION
A2	AVDD_CDR1	Analog Power	1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
A1	AVSS_CDR1	Analog Ground	Analog ground.
H1	AVDD_CDR2	Analog Power	1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
H2	AVSS_CDR2	Analog Ground	Analog ground.
J1	AVDD_CDR3	Analog Power	1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
J2	AVSS_CDR3	Analog Ground	Analog ground.
T2	AVDD_CDR4	Analog Power	1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
T1	AVSS_CDR4	Analog Ground	Analog ground.
C2, D4, E3, E4, F2, F3, F4, G3, K3, K4, L2, L3, L4, M3, M4, P2	AVSS_EQ	Analog Ground	Analog ground.
D1	AVDD_REG1	Analog Power	1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
D2	AVSS_REG1	Analog Ground	Analog ground.
E1	AVDD_REG2	Analog Power	1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
E2	AVSS_REG2	Analog Ground	Analog ground.
M1	AVDD_REG3	Analog Power	1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
M2	AVSS_REG3	Analog Ground	Analog ground.
N1	AVDD_REG4	Analog Power	1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
N2	AVSS_REG4	Analog Ground	Analog ground.
H3	AVDD_BG	Analog Power	1.8V analog power supply for band-gap. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
J3	AVSS_BG	Analog Ground	Analog ground.
C5	AVDD_TST1	Analog Power	1.0V analog power supply for test outputs. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
C4	AVSS_TST1	Analog Ground	Analog ground.
P3	AVDD_TST4	Analog Power	1.0V analog power supply for test outputs. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
N3	AVSS_TST4	Analog Ground	Analog ground.
P4	AVDD_DAC	Analog Power	1.8V analog power supply for audio DAC. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
N4	AVSS_DAC	Analog Ground	Analog ground.
T6	AVDD_AFE	Analog Power	1.8V analog power supply for audio AFE (Audio Front-End). Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
R6	AVSS_AFE	Analog Ground	Analog ground.
T7	AVDD_FPLL10	Analog Power	1.0V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
R7	AVSS_FPLL10	Analog Ground	Analog ground.
P7	AVDD_FPLL18	Analog Power	1.8V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.

Pin Descriptions (Continued)

PIN LOCATION	PIN NAME	TYPE	DESCRIPTION
N7	AVSS_FPLL18	Analog Ground	Analog ground.
A9	AVDD_GUARD	Analog Power	1.0V analog power supply guard ring. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
B9	AVSS_GUARD	Analog Ground	Analog ground.
C8	AVDD_MISC10	Analog Power	1.0V analog miscellaneous power supply. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
D8	AVSS_MISC10	Analog Ground	Analog ground.
A8	AVDD_MISC18	Analog Power	1.8V analog miscellaneous power supply. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
B8	AVSS_MISC18	Analog Ground	Analog ground.
C7	AVDD_XTAL	Analog Power	1.0V analog power supply for crystal oscillator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
D7	AVSS_XTAL	Analog Ground	Analog ground.
C3	AVDD_PLL10	Analog Power	1.0V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
D3	AVSS_PLL10	Analog Ground	Analog ground.
B3	AVDD_PLL18	Analog Power	1.8V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
A3	AVSS_PLL18	Analog Ground	Analog ground.
C6, D5, D6, E5, E6, F5, G4, G5, H4, H5, H6, J4, J5, J6, K5, K6, L5, M5	AVSS_ESD	Analog Ground	Analog ground.
E7, E8, E9, E10, E11, F6, F7, G6, G7, J12, K12, L12, M12	DVDDE	Digital Power	3.3V digital power supply for I/O. Place a local 0.1µF ceramic bypass capacitor to the digital ground as close to the pin as possible.
E12, F12, G12, H12, K7, L6, L7, M6, M7, M8, M9, M10, M11	DVDDI	Digital Power	1.0V digital power supply for core. Place a local 0.1µF ceramic bypass capacitor to the digital ground as close to the pin as possible.
F8, F9, F10, F11, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11	DVSS	Digital Ground	Digital ground.

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
TW6874-BB1-CR	TW6874 BB1-CR	0 to +70	256 ball LFBGA (13.5mmx13.5mm)	V256.13.5x13.5
TW6874-BB1-CR-EVALZ	Evaluation Board			

NOTES:

1. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCuNi- e8 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see product information page for TW6874. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

Supply Pins
- AVDD_CDR1 to AVSS_CDR1 . . . . . +1.2V
- AVDD_CDR2 to AVSS_CDR2 . . . . . +1.2V
- AVDD_CDR3 to AVSS_CDR3 . . . . . +1.2V
- AVDD_CDR4 to AVSS_CDR4 . . . . . +1.2V
- AVDD_FPLL10 to AVSS_FPLL10 . . . . . +1.2V
- AVDD_PLL10 to AVSS_PLL10 . . . . . +1.2V
- AVDD_XTAL to AVSS_XTAL . . . . . +1.2V
- AVDD_MISC10 to AVSS_MISC10 . . . . . +1.2V
- AVDD_GUARD to AVSS_GUARD . . . . . +1.2V
- AVDD_TST1 to AVSS_TST1 . . . . . +1.2V
- AVDD_TST4 to AVSS_TST4 . . . . . +1.2V
- AVDD_BG to AVSS_BG . . . . . +2.5V
- AVDD_REG1 to AVSS_REG1 . . . . . +2.5V
- AVDD_REG2 to AVSS_REG2 . . . . . +2.5V
- AVDD_REG3 to AVSS_REG3 . . . . . +2.5V
- AVDD_REG4 to AVSS_REG4 . . . . . +2.5V
- AVDD_AFE to AVSS_AFE . . . . . +2.5V
- AVDD_DAC to AVSS_DAC . . . . . +2.5V
- AVDD_FPLL18 to AVSS_FPLL18 . . . . . +2.5V
- AVDD_PLL18 to AVSS_PLL18 . . . . . +2.5V
- AVDD_MISC18 to AVSS_MISC18 . . . . . +2.5V
- DVDDI to DVSS . . . . . +1.2V
- DVDDE to DVSS . . . . . +4.0V

Other Pins
- Analog Audio Input Voltage . . . . . AVSS_AFE V to AVDD_AFE V
- Analog Audio Output Voltage . . . . . AVSS_DAC V to AVDD_DAC V
- Voltage on any Digital Pin . . . . . DVSS V to DVDDE V

ESD Ratings
- Human Body Model (JS-001-2010) 2kV
- Charged Device Model (JESD22-C101E) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
LFBGA Package (Notes 3, 4)	22.7	7.9

Power Dissipation . . . . . See Electrical Specifications page 14
Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Operating Temperature . . . . . 0°C to +70°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
4. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications

AVDD_1V0 = AVDD_CDR1 = AVDD_CDR2 = AVDD_CDR3 = AVDD_CDR4 = AVDD_PLL10 = AVDD_FPLL10 = AVDD_XTAL = AVDD_MISC10 = AVDD_GUARD = AVDD_TST1 = AVDD_TST4 = 1.0V, AVDD_1V8 = AVDD_BG = AVDD_REG1 = AVDD_REG2 = AVDD_REG3 = AVDD_REG4 = AVDD_AFE = AVDD_PLL18 = AVDD_FPLL18 = AVDD_MISC18 = AVDD_DAC = 1.8V, DVDD_1V0 = DVDDI = 1.0V, DVDD_3V3 = DVDDE = 3.3V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
POWER SUPPLY VOLTAGE						
AVDD_1V0	Analog 1.0V Supply Voltage		0.95	1.0	1.05	V
AVDD_1V8	Analog 1.8V Supply Voltage		1.7	1.8	1.9	V
DVDD_1V0	Digital 1.0V Core Supply Voltage		0.95	1.0	1.05	V
DVDD_3V3	Digital 3.3V IO Supply Voltage		3.0	3.3	3.6	V
POWER DISSIPATION						
I_AVDD_1V0	Analog 1.0V Supply Current			250		mA
I_AVDD_1V8	Analog 1.8V Supply Current			450		mA
I_DVDD_1V0	Digital 1.0V Core Supply Current			400		mA
I_DVDD_3V3	Digital 3.3V IO Supply Current	16-bit		85		mA
		8-bit		215		mA
P_{TOTAL}	Total Power	16-bit		1740		mW
		8-bit		2170		mW
PARALLEL VIDEO OUTPUT (Note 8)						
f_{CLK}	Pixel Clock Frequency	SD 270Mbps uncompressed serial data input to 8-bit parallel output format. Figure 5		27		MHz
		1. HD 1.485Gbps uncompressed serial data input to 16-bit parallel output format. Figure 6. 2. HD 270Mbps compressed serial data input to 16-bit parallel output format. Figure 6.		74.25		MHz
		1. HD 1.485Gbps uncompressed serial data input to 8-bit parallel output format. Figure 7. 2. HD 270Mbps compressed serial data input to 8-bit parallel output format. Figure 7.		148.5		MHz
DCYC	Pixel Clock Duty Cycle		45		55	%
t_S	Setup Time (1a in Figure 4)	From VDn transition to rising edge of CLKNn	3			ns
t_H	Hold Time (1b in Figure 4	From rising edge of CLKNn to VDn transition	0.5			ns
SDI ANALOG INPUTS						
SDR	Serial Data Rate		0.27		1.5	Gbps
VIS	Serial Data Input Swing				880	mV
CL59	Achievable Cable Length RG59 (Note 6)	1.485Gbps		150		m
		270Mbps (SD or VC-2)		300		m
CL3C2V	Achievable Cable Length 3C-2V (Note 6)	1.485Gbps		70		m
		270Mbps (SD or VC-2)		120		m
DIGITAL INPUTS						
VIH	Input High Voltage		2.0		DVDD_3V3	V
VIL	Input Low Voltage		0		0.8	V
I_L	Input Leakage Current		-10	0	+10	µA
C_{IN}	Input Capacitance	f = 1MHz, V_{IN} 2.4V		2		pF

Electrical Specifications

AVDD_1V0 = AVDD_CDR1 = AVDD_CDR2 = AVDD_CDR3 = AVDD_CDR4 = AVDD_PLL10 = AVDD_FPLL10 = AVDD_XTAL = AVDD_MISC10 = AVDD_GUARD = AVDD_TST1 = AVDD_TST4 = 1.0V, AVDD_1V8 = AVDD_BG = AVDD_REG1 = AVDD_REG2 = AVDD_REG3 = AVDD_REG4 = AVDD_AFE = AVDD_PLL18 = AVDD_FPLL18 = AVDD_MISC18 = AVDD_DAC = 1.8V, DVDD_1V0 = DVDDI = 1.0V, DVDD_3V3 = DVDDE = 3.3V, T_A = +25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
DIGITAL OUTPUTS						
VOH	Output High Voltage	IO = -2mA	2.4			V
VOL	Output Low Voltage	IO = +2mA			0.4	V
I_{OZ}	Tri-State Current				10	µA
CRYSTAL						
f_{XTAL}	Nominal Frequency (Fundamental)			27		MHz
DEV_{XTAL}	Deviation (Note 7)				±30	ppm
CL	Load Capacitance			22		pF
RS	Series Resistor (ESR)			50		Ω
ANALOG AUDIO INPUT						
ViFULL	Full Scale Input Voltage Range (Note 9)		0.13		1.76	V_{P-P}
	Interchannel Isolation (Note 10)			90		dB
ANALOG AUDIO OUTPUT						
VOFULL	Full Scale Output Voltage (Note 11)			1.4		V_{P-P}
	Total Harmonic Distortion (THD)			51		dB
	Signal to Noise Ratio (SNR)			64		dB
DIGITAL AUDIO						
t_{A_pd}	ASYNR, ADATR, ADATM Propagation Delay		1.0		4	ns
t_{A_hw}	ACLKP High Pulse Duration		27			ns
t_{A_lw}	ACLKP Low Pulse Duration (Note 12)		54			ns
t_{A_su}	ASYNP, ADATP Setup Time (Note 12)		26			ns
t_{A_h}	ASYNP, ADATP Hold Time		25			ns
I^2C SERIAL CONFIGURATION INTERFACE (Figure 25)						
f_{SCL}	SCL Clock Frequency				400	kHz
$t_{SU:STA}$	Set-up Time for a START Condition		370			ns
$t_{HD:STA}$	Hold Time for a START Condition		74			ns
$t_{SU:STO}$	Set-up Time for a STOP Condition		370			ns
t_{BUF}	Bus Free Time between a STOP and START Condition		740			ns
$t_{SU:DAT}$	Data Set-up Time		74			ns
$t_{HD:DAT}$	Data Hold Time		50		900	ns
t_r	Rise Time of SDA and SCL				300	ns
t_f	Fall Time of SDA and SCL				300	ns
CBUS	Capacitive Load for each Bus Line				400	pF

Electrical Specifications

AVDD_1V0 = AVDD_CDR1 = AVDD_CDR2 = AVDD_CDR3 = AVDD_CDR4 = AVDD_PLL10 = AVDD_FPLL10 = AVDD_XTAL = AVDD_MISC10 = AVDD_GUARD = AVDD_TST1 = AVDD_TST4 = 1.0V, AVDD_1V8 = AVDD_BG = AVDD_REG1 = AVDD_REG2 = AVDD_REG3 = AVDD_REG4 = AVDD_AFE = AVDD_PLL18 = AVDD_FPLL18 = AVDD_MISC18 = AVDD_DAC = 1.8V, DVDD_1V0 = DVDDI = 1.0V, DVDD_3V3 = DVDDE = 3.3V, T_A = +25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
SPI SERIAL CONFIGURATION INTERFACE (Figures 31 and 32)						
f_{SER}	SCL Maximum Operating Frequency				10	MHz
DC_{SCL}	SCL Duty Cycle		40	50	60	%
t_{EL}	CSB High Time		20			ns
t_{ERSR}	CSB Falling Edge to the First SCL Rising Edge		10			ns
t_{DS}	MOSI Set-up Time		5			ns
t_{DH}	MOSI Hold Time		5			ns
t_{SREF}	Last SCL Rising Edge to CSB Rising Edge		10			ns
t_{WRITE}	Write Wait Period		$3*t_{scl}$			ns
t_{READ}	Read Wait Period		$9*t_{scl}$			ns

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. Performance is cable dependent. Bare copper conductor cable offers better performance than copper clad steel/aluminum conductor cable.
7. Crystal deviation is based on normal operating condition.
8. CLKn timing is affected by the CLK_DEL register.
9. Tested at input gain of 0dB. f_{IN} = 1kHz.
10. Tested at input gain of 0dB. f_S = 8kHz and 16kHz.
11. Tested at output gain of 0dB. F_{OUT} = 1kHz.
12. t_{A_lw} and t_{A_su} Min values are for f_S = 48kHz mode only. If f_S < 48kHz, the Min values are larger. High period of ACLKR/ACLKP is one 36MHz clock period.

SDI Video Inputs

The TW6874 receives serial digital (SDI) video data on four independent channels. Each channel consists of an equalizer (EQ), a Clock and Data Recovery (CDR) unit, SDI descrambler/deframer, SDI speed/format auto-detection and VC2 decompression.

SDI Video Formats

The supported SDI video formats include:

- 270Mbps (SMPTE 259M Level C)
  - 525i/625i 50, 59.94 fields/s
  - VC-2 compressed 720p 50, 59.94 frames/s
  - VC-2 compressed 1080p 25, 29.97 frames/s
  - VC-2 compressed 1080i 50, 59.94 fields/s
- 1.485Gbps (SMPTE ST 292)
  - 720p 25, 30 frames/s
  - 720p 50, 60 frames/s
  - 1080PsF 25, 30 frames/s
  - 1080p 24, 25, 30 frames/s
  - 1080i 50, 60 fields/s
- 1.485/1.001Gbps (SMPTE ST 292)
  - 720p 59.94 frames/s
  - 1080PsF 29.97 frames/s
  - 1080p 23.976, 29.97 frames/s
  - 1080i 59.94 fields/s

Any of the supported video formats can be driven into any of the four SDI inputs without limitation. The video streams are received in 10-bit YCbCr 4:2:2 sampled format. The deserialized video outputs are truncated into 8-bit YCbCr 4:2:2 sampled format.

Adaptive Equalization

The TW6874 adaptive equalizers (EQ) function to compensate for link losses of various frequency components up to 1.5Gbps. The EQ compensates for nonlinear cable attenuation such that overall end-to-end frequency response is flat.

Clock Data Recovery/Descrambler

The SDI signal embeds its clock in the serialized bit stream. To recover the serial bit data, the embedded clock is recovered from the transition edges of the data stream. The data bit sequence is derived by using the recovered clock to latch the bits from the EQ output signal. The TW6874 clock data recovery module (CDR) recovers the low jitter embedded clock by using a high performance PLL to track the incoming data stream.

To ensure that enough data transitions occur in any video content, the SDI standard employs a scrambling circuit in the transmitter. At the receiver side, after the CDR function is performed, a descrambler circuit is then used to convert the scrambled bit sequences back into the original video data content.

SDI Auto Detection

The link speed mode of SDI is automatically detected by the hardware auto detection module. When the TW6874 is powered up initially or when the link mode has changed, the hardware switches among HD/SD modes until the CDR locks on to the link data.

Once the PLL has locked to the data stream, the hardware detects valid data from the link. The SDI_MODE_LOCKED bit is set in register 0x000/2/4/6 when the TW6874 has locked to a valid bit rate and received valid SDI data. The detected mode is available from SDI_MODE in the same register.

After the link speed mode is locked, the hardware further detects the video formats such as: video resolution, frame rate and scan mode. When a valid format is detected, the T_LOCKED flag is set in register 0x000/2/4/6 and the detected video format is shown in T_SCAN, T_RATE and T_FAMILY status registers at 0x000~0x007.

VC-2 (Dirac) Decompression

Compressed VC-2 serial data streams are received at SD-SDI (270Mbps) data rates. The data formats supported are according to SMPTE 259M standard and are as follows:

- Compressed 720p 50, 59.94 frames/s
- Compressed 1080p 25, 29.97 frames/s
- Compressed 1080i 50, 59.94 fields/s

The generated pixel clock is 74.25MHz in BT.1120 16-bit mode or 148.5MHz in BT.1120 8-bit mode.

Cable Reach

The TW6874 is designed to work with various types of 75Ω coaxial cable: e.g., RG6, RG59, or 3C-2V. Each of these cable types have various core and shielding variations. Cable reach performance is a function of the cable configuration. To achieve the best performance for any given type of cable, the PCB layout guidelines page 88 should be adhered to closely. It is recommended to emulate the reference layout.

Video Output Format

The TW6874 receives serial data and converts it to the equivalent parallel ITU-R BT.656/BT.1120 format. In BT.656/BT.1120 format, timing reference signals (TRS, consisting of SAV and EAV codes) are inserted into the data stream to indicate the active video time. The output timing is illustrated in Figure 3.

Video Output Port Mapping

Each video output port maps only from its associated SDI input port. For example, SDI1 maps to VD1; SDI2 maps to VD2, etc. The output data format is: BT.656 for SD; BT.1120 for HD in either 8-bit or 16-bit mode.

For SD formats, the same BT.656 video data is output on lower byte (VDn[7:0]) of the 16-bit port as shown in the Figure 5.

For HD formats, the output data can be either BT.1120 16-bit, or 8-bit mode with the pixel clock running at twice the speed.

In BT.1120 mode, Y is output on the lower byte (bits 7:0) and C is output on the upper byte (bits 15:8). In 8 bit mode, the Y/C data is output on both bytes of the video port as shown in Figure 7.

Figure 4 shows the timing relationship for the output clock and data for single and double clock rate operation. Figures 5 to 7 show the allowed data output formats.

In Figures 4 to 7, n = 1 to 4.

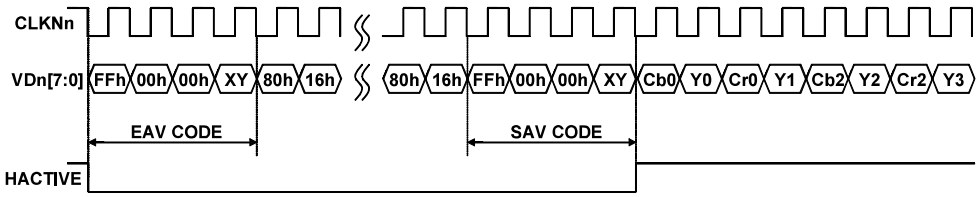


FIGURE 3. BT.656/BT.1120 LIKE FORMAT

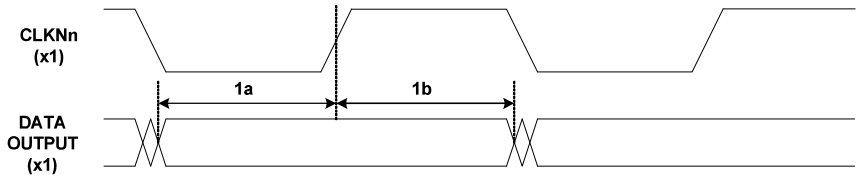


FIGURE 4. CLKNn TO VD[15:0] TIMING

SD BT.656 Output Format

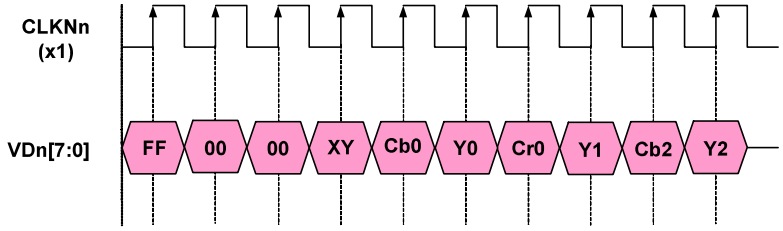


FIGURE 5. ONE SD CHANNEL BT.656 FORMAT, CLKNn AT 27MHz

HD BT.1120 16-Bit or 8-Bit Output Formats

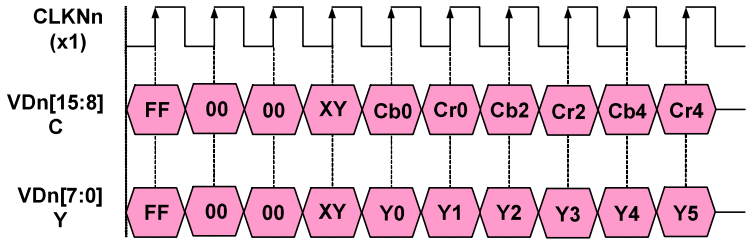


FIGURE 6. ONE HD CHANNEL BT.1120 16-BIT FORMAT, CLKNn AT 74.25MHz (HD)

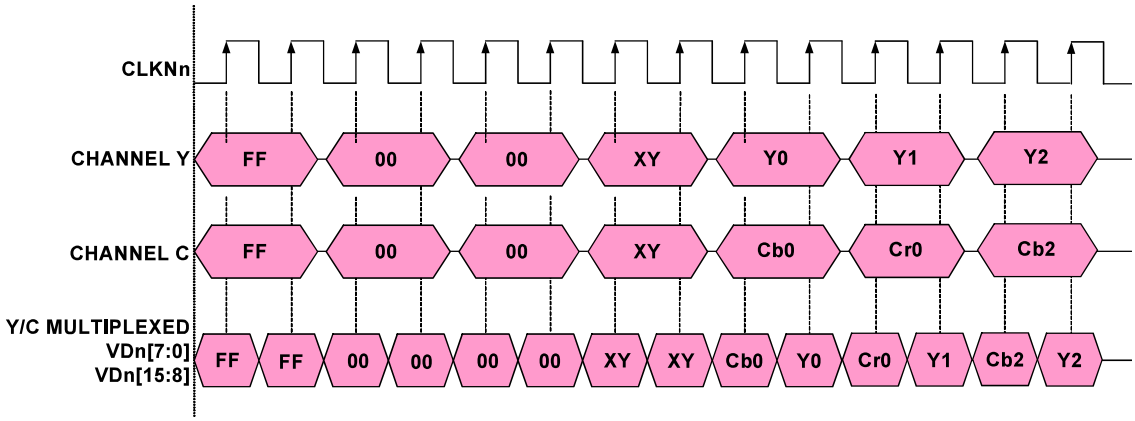


FIGURE 7. ONE HD CHANNEL BT.1120 8-BIT MODE FORMAT, CLKNn AT 148.5MHz

Audio Interface

Audio CODEC

The audio CODEC in the TW6874 is composed of five Analog-to-Digital Converters (ADC), one Digital-to-Analog Converter (DAC), audio mixer and digital serial audio interface as shown in Figure 8. The TW6874 can receive 5 analog audio signals, 4 SDI ancillary audio signals and 1 multi-channel digital serial audio stream. It can produce 1 mixing analog audio signal and 2 digital serial audio streams.

The analog audio input signal gain for the AIN1/2/3/4/5 pins can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1/2/3/4/5 registers before being sampled by the ADCs. If the SDI stream has ancillary audio embedded, these can be used in lieu of AIN1/2/3/4. The ACLKP, ASYNP and ADATP pins from the I2S decoder block are used to receive digital serial audio input data for playback. To record audio data, the I2S encoder block provides the digital serial audio output via the ACLKR, ASYNR and ADATR pins. The AOUT pin sends analog audio data received from the audio DAC. The output level can be controlled by a programmable gain amplifier via the DAC_GAIN register.

The TW6874 can mix all the audio inputs including analog audio and digital audio according to the predefined mixing ratio for each audio via the MIX_RATIO1/2/3/4/5/PB registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio DAC supports the analog mixing audio output. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

The main purpose of the AIN5 pin is to make the standard I2S digital audio output for AIN5 data available on the ADATM pin for audio back channel applications. Usually, AIN1/2/3/4 audio data are output to the CODEC on the ADATR pin.

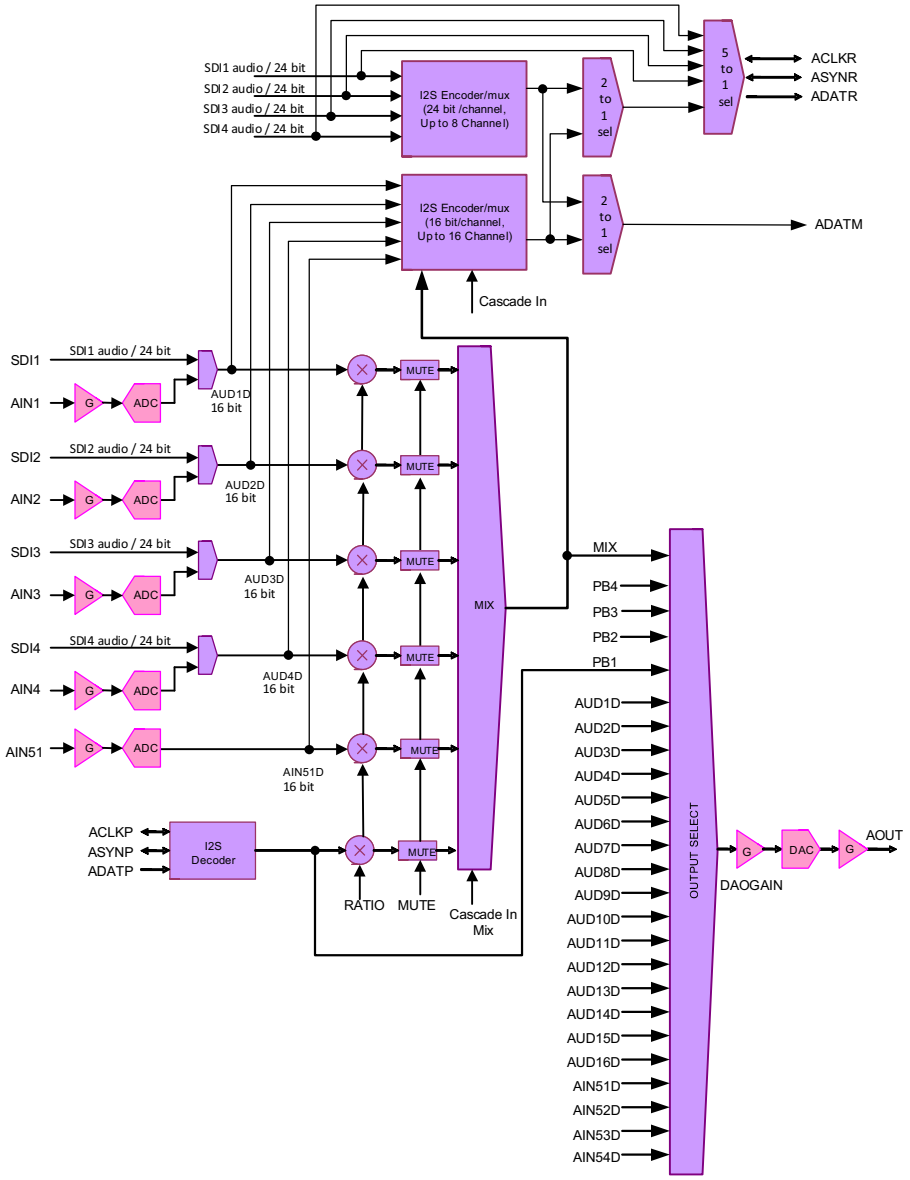


FIGURE 8. AUDIO CODEC BLOCK DIAGRAM

SDI Ancillary Audio

Embedded SDI ancillary audio is formed of 4 groups of 4 channels. Each audio sample is 24 bits wide, depending on whether it is embedded in SD/VC2 or HD. One of these channels can be selected from each SDI input and sent to the TW6874's audio processor. If an SDI audio channel is selected, the respective analog audio input is not used.

SDI ancillary audio uses 48kHz sampling frequencies.

The TW6874 can truncate SDI ancillary audio to 16 bits in order to allow mixing with the analog audio data from channels where SDI audio is not used.

Serial Audio Interface

There are three kinds of digital serial audio interfaces in the TW6874. The first is a multichannel recording output, the second is a mixing output and the third is a playback input. These three digital serial audio interfaces follow a standard I2S interface as shown in Figure 9. The I2S MUX can output audio channels from each of the SDI channel, multiplexed 24-bit audio channels from 4 SDI channels, or multiplexed 16-bit 16 audio channels from SDI, ADC and I2S input.

PLAYBACK INPUT

The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for playback. The ACLKP and ASYNP pins can be operated in master or slave mode. For master mode, these pins work as outputs and generate the standard audio clock and synchronizing signals. For slave mode, these pins are inputs and accept the standard audio clock and synchronizing signals. The ADATP pin is always an input regardless of the operating mode. One channel of audio data (from the left or right channel) should be selected for playback audio by the PB_LRSEL.

RECORD OUTPUT

To record audio data, the TW6874 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. The sampling frequency comes from the $256*f_S$, $320*f_S$ or $384*f_S$ audio system clock setting. Even though the standard I2S and DSP format can have only two audio data on left and right channel, the TW6874 can provide an extended I2S and DSP format, which can have 16 channel audio data through the ADATR pin. The R_MULTCH defines the number of audio channels to be recorded by the ADATR pin. ASYNR's frequency is always at the sampling frequency (f_S). Thus, one ASYNR period is always equal to 256*ACLKR periods when AIN5MD = 0. Figure 10 shows the digital serial audio data organization for multichannel audio.

The ACLKR pin can be operated in master or slave mode. For master mode, this pin works as an output and generates the standard audio clock. For slave mode, this pin is an input and accepts the standard audio clock. The ASYNR pin can be operated as an input or output regardless of the operating mode. The ADATR pin is always an output.

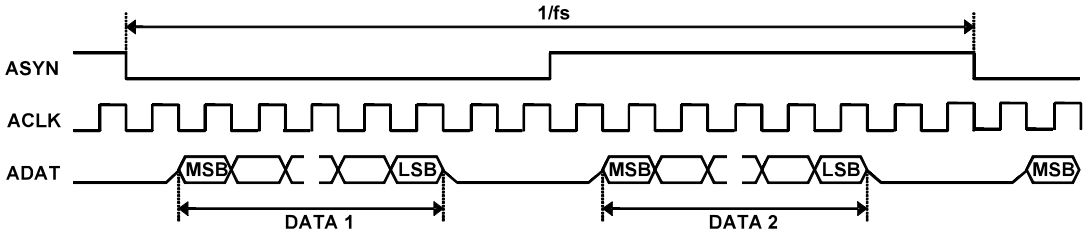


FIGURE 9A. I2S FORMAT

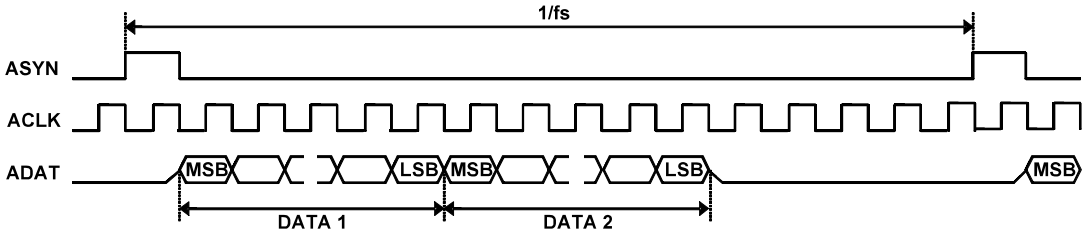


FIGURE 9B. DSP FORMAT

FIGURE 9. SERIAL AUDIO INTERFACE FORMAT

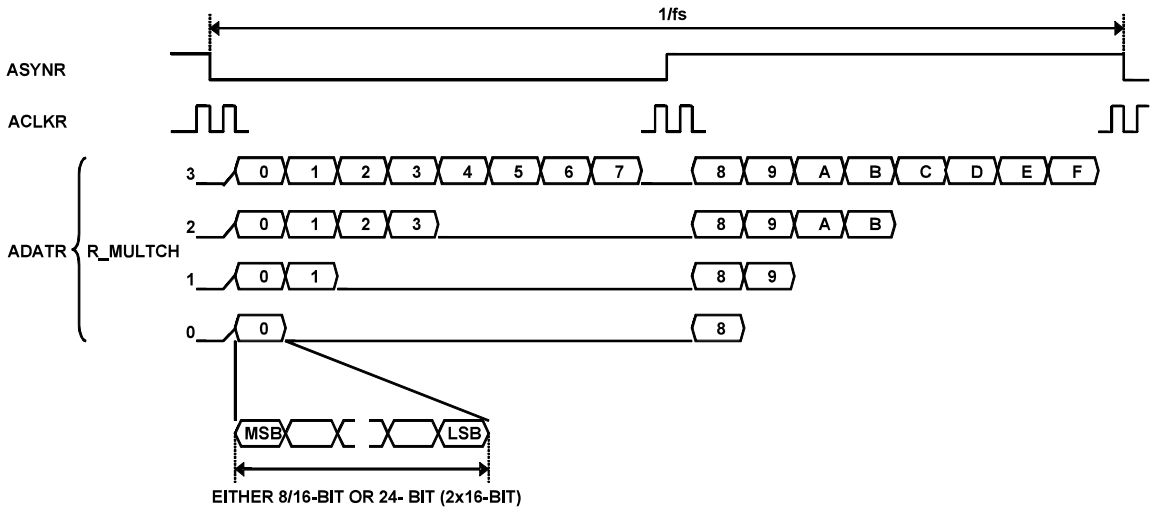


FIGURE 10A. I2S FORMAT

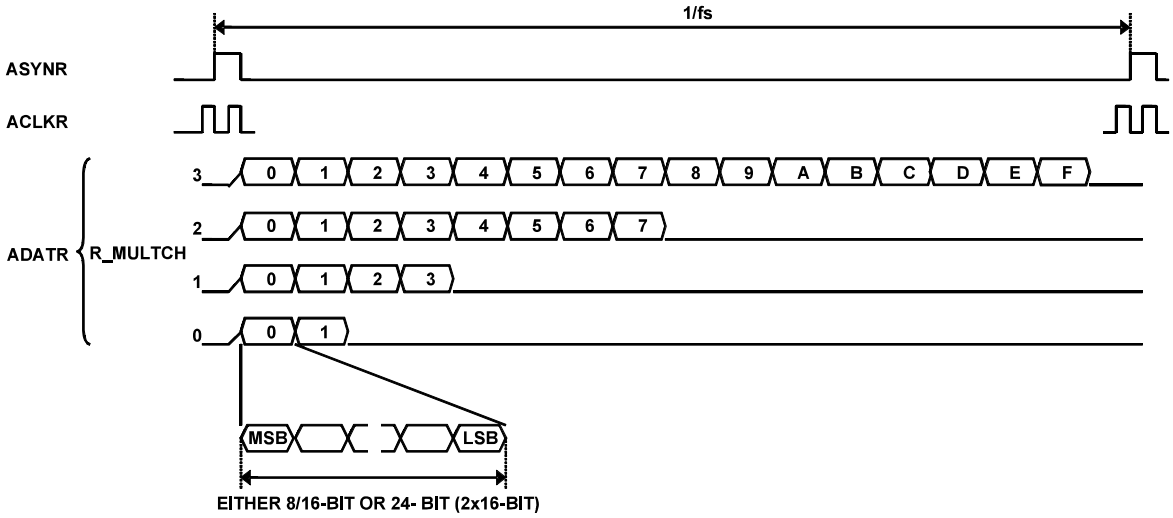


FIGURE 10B. DSP FORMAT

FIGURE 10. MULTICHANNEL AUDIO RECORD FORMAT

TABLE 1. MULTICHANNEL AUDIO RECORD SEQUENCE (I2S)

R_MULTCH	PIN	LEFT CHANNEL								RIGHT CHANNEL							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

TABLE 2. MULTICHANNEL AUDIO RECORD SEQUENCE (DSP)

R_MULTCH	PIN	LEFT/RIGHT CHANNEL															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Tables 1 (I2S) and 2 (DSP) show the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel numbers but represent sequence only. The actual audio channel should be assigned to sequence 0~F by the R_SEQ0~R_SEQF registers. The audio sequence of ADATM is also shown in these two tables. The ADATM pin is configured for record via the R_ADATM register.

MIX OUTPUT

The digital serial audio data on the ADATM has two different audio data: mixing audio and playback audio. The mixing digital serial audio data is the same as the analog mixing output. The sampling frequency, bit width and number of audio channels for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

Multidevice Cascading

The TW6874 can output 16 channel 8-bit/16-bit audio data on the ACLKR/ASYNR/ADATR outputs simultaneously. Therefore, up to 4 devices can be connected in most multidevice application cases.

Since each stage device can accept 4+1 analog audio signals or 4 SDI audio signals, four cascaded devices will be a 16-channel 16-bit audio controller by default {AFS384, AIN5MD} = 00. The first stage device provides 16-channel 8-bit/16-bit digital serial audio data for record. Even though the first stage device has only one digital serial audio data pin ADATR for record, the TW6874 can generate 16 channel data simultaneously using the multichannel method. This first stage device can also output 16 channel mixing audio data of the digital serial audio data, SDI ancillary audio data (16-bit) and analog audio signal. The first stage device accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by the DAC in the first stage.

Several master/slave mode configurations are available. Figure 11 is the most recommended and demanded system with Clock Master mode (ACLKRMASTER = 1). Figure 12 is the most recommended system with Clock Slave/Sync Slave mode (ACLKRMASTER = 0, ASYNROEN = 1). Other system combinations are also available dependent upon the application.

In Figures 11 and 12, Mix1-16-51-54/Pb1 means mix output of AIN1-16, AIN51-54 and Playback1. AIN1-16-51-54/Pb1 means one selected audio output from AIN1-16-51-54/Pb1.

If any one of the TW6874s use {AFS384, AIN5MD} = 01 or {AFS384, AIN5MD} = 10, all other cascaded TW6874s must be set up with the same {AFS384 AIN5MD} mode.

In multidevice audio operation mode, the same oscillator clock source needs to be connected to each TW6874 XTI pin.

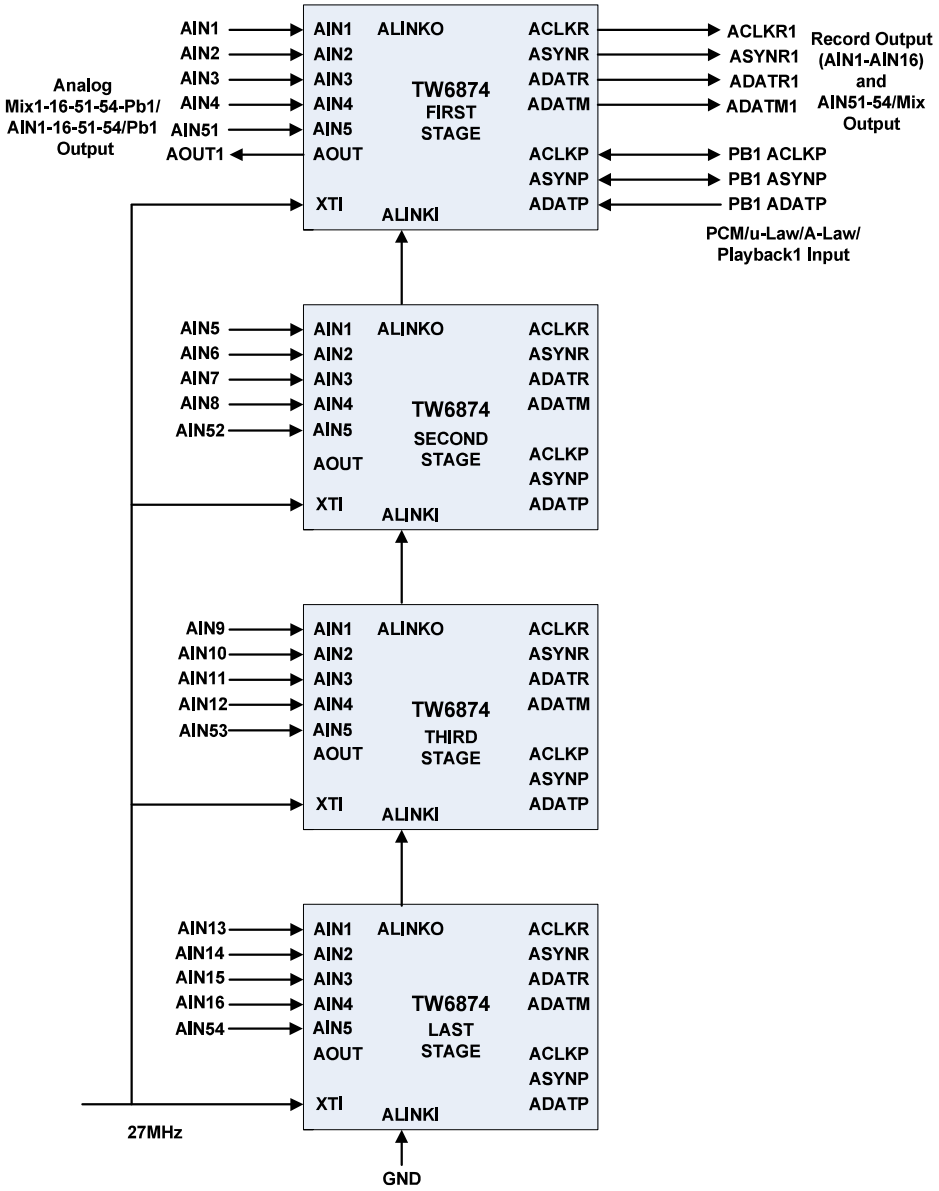


FIGURE 11. RECOMMENDED CLOCK MASTER CASCADE MODE CONFIGURATION

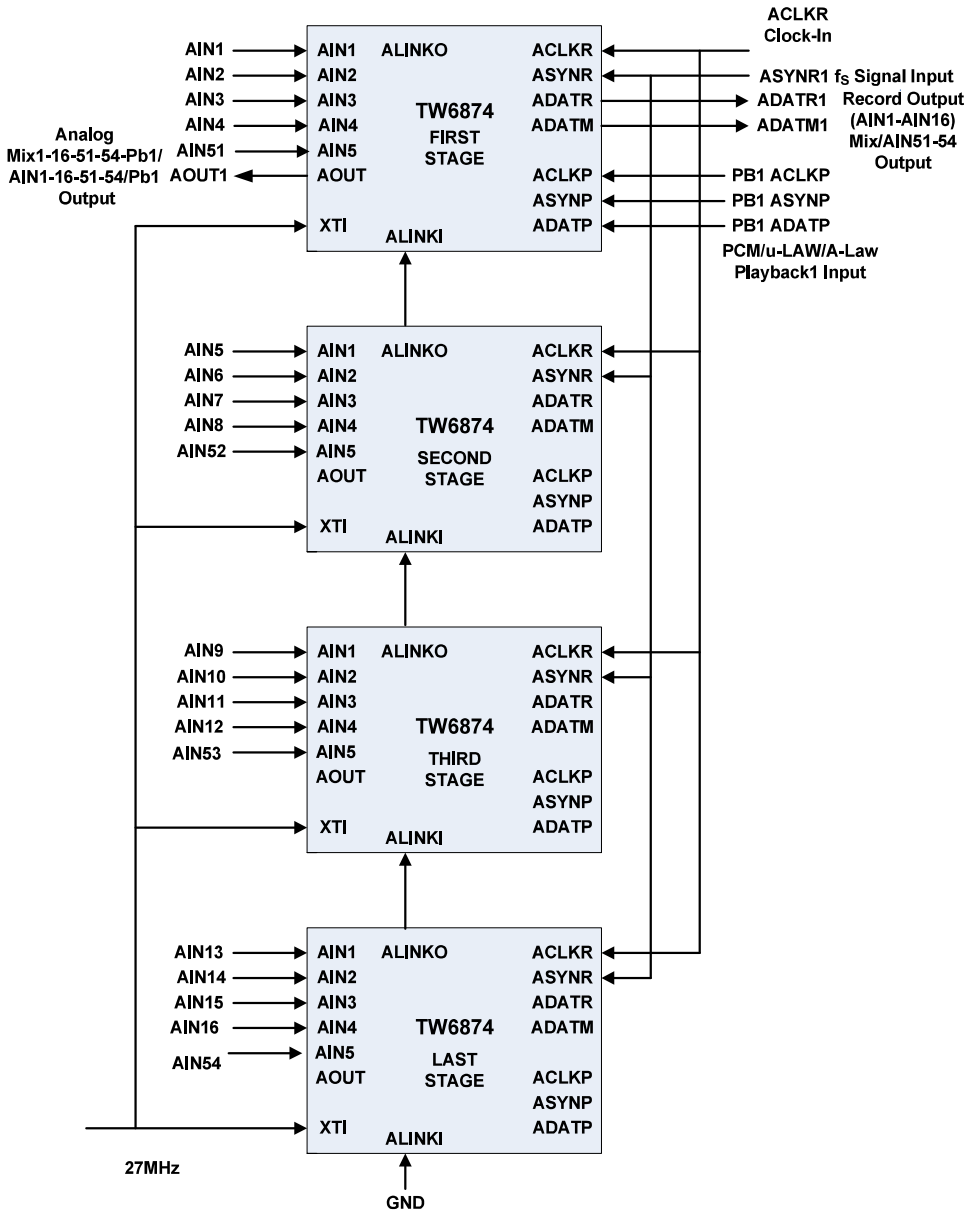


FIGURE 12. RECOMMENDED CLOCK SLAVE/SYNC SLAVE MODE CONFIGURATION

Audio Clock Master/Slave Mode

The TW6874 has two types of audio clock modes. If the ACLKRMASTER register is set to 1, analog audio is sampled by the audio clock internally generated by the ACKG (Audio Clock Generator). In this master mode, ACLKR/ASYNR pins are outputs. The ASYNROEN register for ASYNR pin should be set to 0 (output enable mode). If the ACLKRMASTER register is set to 0, analog audio is sampled by the audio clock on the ACLKR pin input. A 256*f_S, 320*f_S or 384*f_S audio clock should be connected to the ACLKR pin from an external master clock source in this slave mode. The ASYNR pin can be either input or output in slave mode. ASYNR's frequency should match the audio sample frequency (f_S) in both master and slave mode. The AIN5MD and AFS384 registers configure the analog audio sample mode per Table 3.

TABLE 3.

REGISTER		
AIN5MD	AFS384	f_S MODE
0	0	256*f_S
1	0	320*f_S
0	1	384*f_S

ACLKR Slave Mode Data Output Timing

The TW6874 always outputs ASYNR/ADATR/ADATM on the falling edge of ACLKR. A new ADATR/ADATM word (or multiple words if using multichannel mode) is output upon each toggle of ASYNR. If ASYNR is an input, it is sampled on the falling edge of ACLKR.

ASYNR CHANGES ON THE FALLING EDGE OF ACLKR

If ASYNR is an input and changes (by the master) on the falling edge of ACLKR or if ASYNR is an output, ADATR/ADATM become valid on the next ACLKR falling edge as shown in Figures 13 and 14.

ASYNR CHANGES ON THE RISING EDGE OF ACLKR

If ASYNR is an input and changes (by the master) on the rising edge of ACLKR, ADATR/ADATM become valid on the next ACLKR falling edge as shown in Figures 15 and 16.

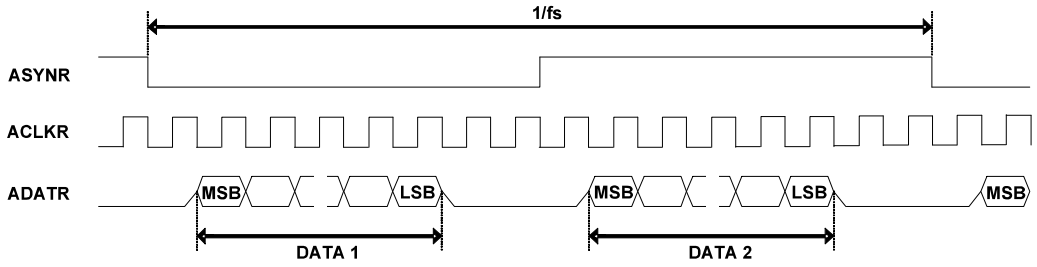


FIGURE 13. ACLKMASTER = 0, RM_SYNC = 0

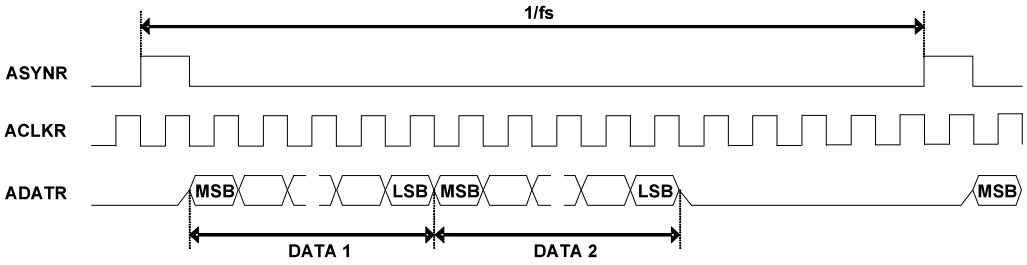


FIGURE 14. ACLKMASTER = 0, RM_SYNC = 1

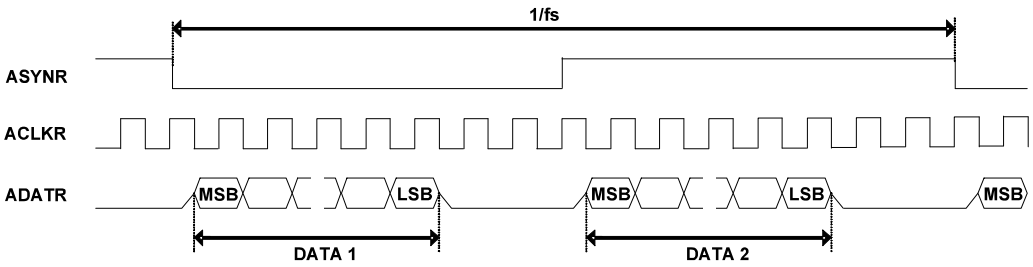


FIGURE 15. ACLKMASTER = 0, RM_SYNC = 0, ASYNROEN = 1

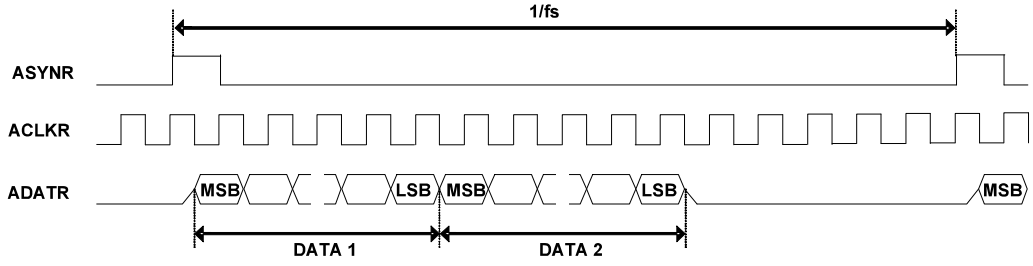


FIGURE 16. ACLKMASTER = 0, RM_SYNC = 1, ASYNROEN = 1

ACLKP/ASYNP Slave Mode Data Input Timing

The following eight data input timings are supported. The ADATPDLY register needs to be set up according to the different ADATP data input timings. Data 1 is only shown as default. The MSB bit is the first input bit as default PBINSWAP = 0. If PBINSWAP = 1, LSB bit is the first input bit.

ASYNP CHANGES ON THE FALLING EDGE OF ACLKP

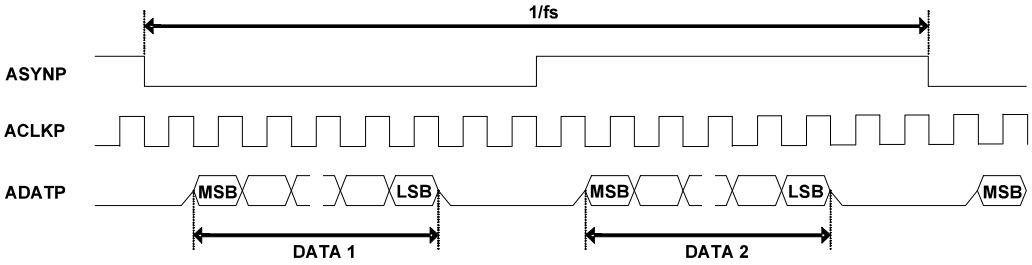


FIGURE 17. RM_SYNC = 0, PB_MASTER = 0, ADATPDLY = 0

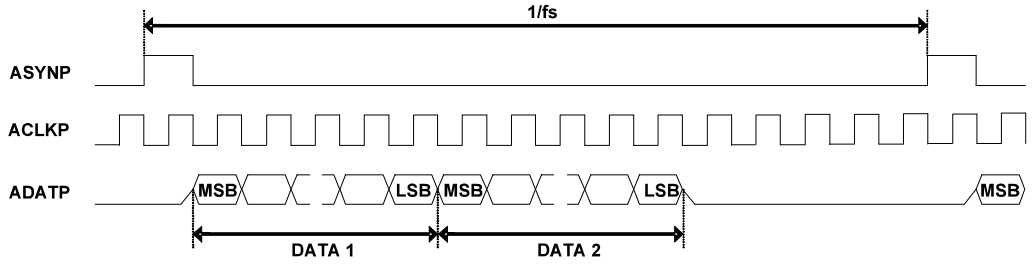


FIGURE 18. RM_SYNC = 1, PB_MASTER = 0, ADATPDLY =

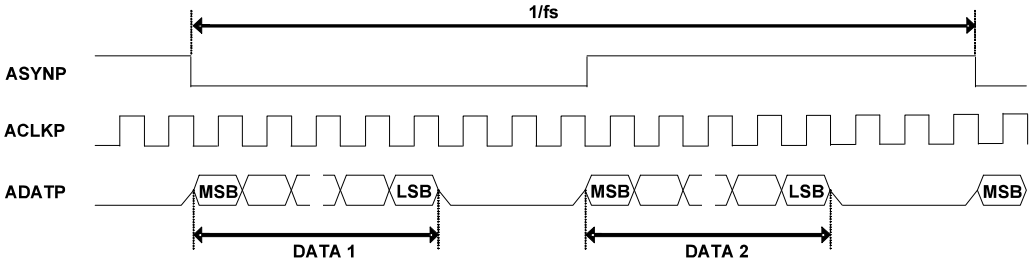


FIGURE 19. RM_SYNC = 0, PB_MASTER = 0, ADATPDLY = 1

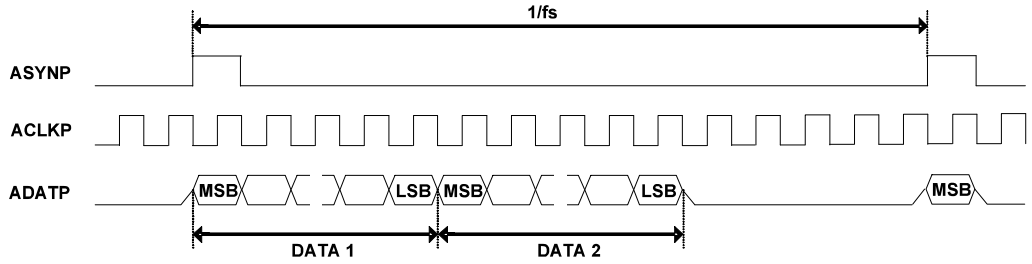


FIGURE 20. RM_SYNC = 1, PB_MASTER = 0, ADATPDLY = 1

ASYNP CHANGES ON THE RISING EDGE OF ACLKP

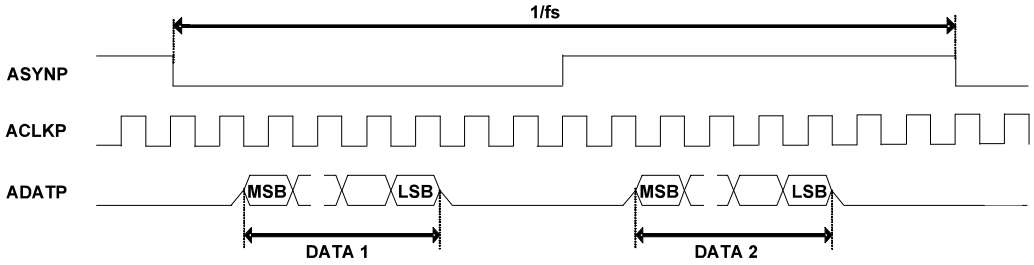


FIGURE 21. RM_SYNC = 0, PB_MASTER = 0, ADATPDLY = 0

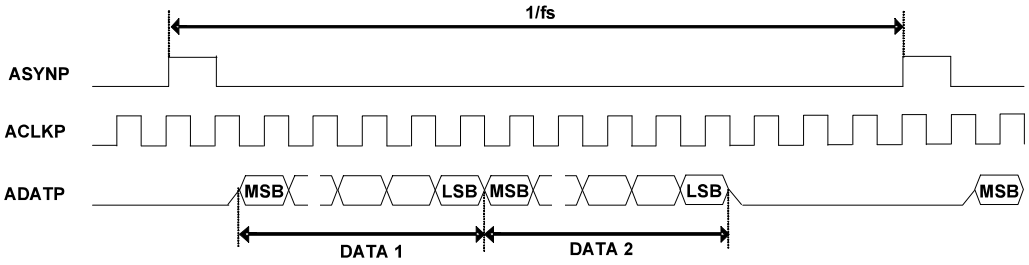


FIGURE 22. RM_SYNC = 1, PB_MASTER = 0, ADATPDLY = 0

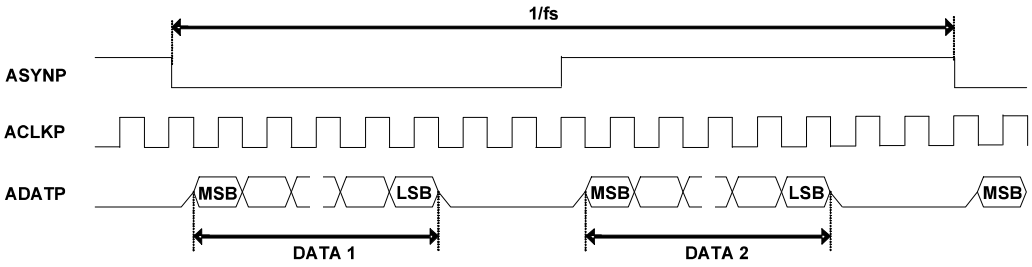


FIGURE 23. RM_SYNC = 0, PB_MASTER = 0, ADATPDLY = 1

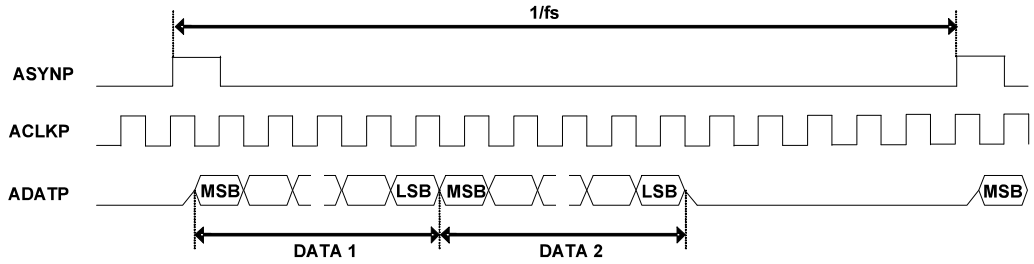


FIGURE 24. RM_SYNC = 1, PB_MASTER = 0, ADATPDLY = 1

Audio Clock Generation

The TW6874 has a built-in audio clock generator. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through the ACKI register based on the following two equations:

$$ACKI = F_{AMCLK} \cdot \frac{2^{23}}{27 \cdot 10^{6}} \cdot (MASCKMD + 1) \quad \text{(EQ. 1)}$$

$$F_{AMCLK}(\text{AMCLK frequency}) = N \cdot f_S \quad \text{(EQ. 2)}$$

$N = 256/320/384$

f_s (sampling frequency) = 8/16/32/44.1/48kHz

AMCLK is used as the audio system clock and the audio ADC clock in master clock mode (ACLKRMASTER register bit is set to 1).

Table 4 provides setting examples of some common audio frequencies with an XTI clock frequency of 27MHz.

TABLE 4. COMMON AUDIO FREQUENCY SETTINGS

AMCLK (MHz)	AFS384	AIN5MD	ACKI [DEC]	ACKI [HEX]
MASCKMD = 1				
256*16kHz	0	0	2545166	26-D6-0E
4.096				
256*8kHz	0	0	1272583	13-6B-07
2.048				
320*16kHz	0	1	3181457	30-8B-91
5.12				
320*8kHz	0	1	1590729	18-45-C9
2.56				
384*16kHz	1	0	3817749	3A-41-15
6.144				
384*8kHz	1	0	1908874	1D-20-8A
3.072				
MASCKMD = 0				
256*48kHz	0	0	3817749	3A-41-15
12.288				
256*44.1kHz	0	0	3507557	35-85-65
11.2896				
256*32kHz	0	0	2545166	26-D6-0E
8.192				
256*16kHz	0	0	1272583	13-6B-07
4.096				
256*8kHz	0	0	636291	09-B5-83
2.048				
320*32kHz	0	1	3181457	30-8B-91
10.24				

TABLE 4. COMMON AUDIO FREQUENCY SETTINGS (Continued)

AMCLK (MHz)	AFS384	AIN5MD	ACKI [DEC]	ACKI [HEX]
320*16kHz	0	1	1590729	18-45-C9
5.12				
320*8kHz	0	1	795364	0C-22-E4
2.56				
384*32kHz	1	0	3817749	3A-41-15
12.288				
384*16	1	0	1908874	1D-20-8A
6.144				
384*8kHz	1	0	954437	0E-90-45
3.072				

Audio Clock Auto Setup

If ACLKRMASTER = 1 (audio clock master mode) and AFAUTO = 1, the TW6874 sets up the ACKI register automatically per the AFMD register value. AFMD takes into account the AFS384/AIN5MD/MASCKMD values when setting ACKI.

TABLE 5. AFMD SETTINGS

AFAUTO	f_S (kHz)	AFMD	MASCKMD
1	8	0	1
1	16	1	1
1	32	2	0
1	44.1	3	0
1	48	4	0
0	ACKI	X	Same as when AFAUTO = 1

Other Information

Ancillary Data

The TW6874 allows SDI ancillary data to be extracted and read via the SPI or I^2C interface. The register map details the registers for configuration and read-back of ancillary data.

Hardware Interrupt

The TW6874 provides the interrupt request function using the IRQ pin. IRQEN enables the interrupt function and the polarity of the IRQ pin is selected by IRQPOL. In addition, individual interrupts must be enabled for each function that is desired to be detected. When the interrupt pin is asserted, each of the functions which have been enabled for interrupt should be read to determine the cause of the interrupt.

Crystal and Clock Oscillator

The TW6874 requires an external 27MHz crystal or oscillator. The crystal connects to the XTI/XTO pins. Alternatively, a 27MHz oscillator drives only the XTI pin. If using the same reference for multiple TW6874s such as for audio cascade mode, then an oscillator is required since it has suitable drive capability. When an oscillator is used, it has to be 1.0V swing because the XTI pin cannot tolerate more than that.

Link Checker

The TW6874 has an integrated PRBS7/23 bit error rate analyzer to serve as the link checker. This checker can be used to optimize operation between transmitter (camera) and the receiver (TW6874) over the coaxial cable interface.

I²C Communication Interface

The TW6874 optionally uses a 2-wire serial bus for communication with its host. I²C is enabled by setting SPIB high. The TW6874 operates as a bus slave. SCL is the Serial Clock line, driven by the host and SDA (full pin name is MOSI_SDA) is the Serial Data line, which can be driven by any device on the bus. SDA is open-drain to allow multiple devices to share the same bus simultaneously. An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) is required for SDA and SCL.

Communication is accomplished in four steps:

1. The host selects the TW6874 it wishes to communicate with.
2. The host writes the first byte of the Configuration Register address it wishes to write to or read from.
3. The host writes the second byte of Configuration Register address it wishes to write to or read from.
4. The host writes to or reads from the selected Configuration Register.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 26). The TW6874 continuously monitors the SDA and SCL lines for the START condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit slave address plus a R/$\overline{W}$ bit, indicating if the next transaction will be a Read (R/$\overline{W}$ = 1) or a Write (R/$\overline{W}$ = 0).

After transmitting the device address and the R/$\overline{W}$ bit, the host must release the SDA line while holding SCL low and wait for an acknowledgment from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDA line low to acknowledge (ACK) the condition (Figure 27). The host will then continue with the next 8-bit transfer. If no device on the bus responds (NACK, where SDA is kept high during the 9th SCL pulse), the host transmits a STOP condition where SDA rises while SCL is high and ends the cycle (Figure 26). Notice that a successful transfer always includes nine SCL pulses.

Once the slave address has been transmitted and acknowledged, one byte of information can be written to or read from the slave. Data on the serial bus must be valid for the entire time SCL is high (Figure 28). Communication with the selected device in the selected direction (read or write) is ended by a STOP command, or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

Configuration Register Write

After receiving the acknowledge bit corresponding to the desired TW6874's slave address byte with R/$\overline{W}$ = 0, the host sends the desired register address where data is to be written. An internal index register points to this address. After receiving the acknowledge bit corresponding to the desired register address byte, the host sends the data byte to be written. The TW6874 loads this to the register pointed by the internal index register. The TW6874 acknowledges the data write and automatically increments the pointer register to point to the next register address. The host can thus write to sequential ascending register addresses. After each transfer, the TW6874 acknowledges the receipt with an acknowledge pulse. To end all transfers to the TW6874 the host issues a STOP condition.

To write to separate or non-sequential register locations, a full I²C START, Device Address (R/$\overline{W}$ = 0), Register Address, Data Write/slave ACK..., STOP sequence must be used for each register location.

Figure 29 shows two views of the steps necessary to write one byte to the Configuration Register.

Configuration Register Read

A TW6874 read cycle has two phases. The first phase is a write to select the desired internal index register. The second phase is the read from the data register. Note that no data is actually written during the first phase.

After receiving the acknowledge bit corresponding to the desired TW6874's slave address byte with R/$\overline{W}$ = 0, the host sends the desired register address from where data is to be read. An internal index register points to this address. After receiving the acknowledge bit corresponding to the desired register address byte, the host sends either a STOP/START or a REPEATED START condition.

The host then sends the same slave address with R/$\overline{W}$ = 1 to indicate a read. The TW6874 transfers the contents of the desired register during eight SCL pulses (controlled by the host). After transferring the byte, the TW6874 releases SDA and the host acknowledges receipt of the data. The TW6874 automatically increments the pointer register to point to the next register address. The host can thus read from sequential ascending register addresses. The host acknowledges receipt of each byte. To end the read, the host does not acknowledge data receipt and then issues a STOP condition.

To read from separate or non-sequential register locations, a full I²C START, Device Address (R/$\overline{W}$ = 0), Register Address, STOP, START, Device Address (R/$\overline{W}$ = 1), Data Read/host ACK..., host NACK, STOP sequence must be used for each register location.

Figure 30 shows two views of the steps necessary to read one byte from the Configuration Register.

I²C Slave Address

In I²C mode, the unused {MISO_ADDR1, CSB_ADDR0} pins are used as input to determine the 7-bit I²C slave address in the following way.

- {MISO_ADDR1, CSB_ADDR0} = 2'b00: Slave Address is 0x68
- {MISO_ADDR1, CSB_ADDR0} = 2'b01: Slave Address is 0x69
- {MISO_ADDR1, CSB_ADDR0} = 2'b10: Slave Address is 0x6A
- {MISO_ADDR1, CSB_ADDR0} = 2'b11: Slave Address is 0x6B

That is, if the 7-bit I²C slave address is 1101000ab (binary), the upper 5 bits of I²C slave address are permanently set to 1101000, while the lower two bits ("a" and "b") are determined by the state of the {MISO_ADDR1, CSB_ADDR0) pins. The two pins allow four TW6874s to be independently controlled while sharing the same I²C bus. The final 8-bit address word transmitted is 1101000abr (binary) where "r" is the R/$\overline{W}$ bit indicating the direction of the next byte(s).

Register Address

Each configuration register is accessed via a 12-bit address. The upper four bits is the page; the lower byte is the address on the page. The upper four bits of the page is always 0 and should be padded as such to make a full byte. The register map lists each register address in a 12-bit format, for example: 0x123. Hence this register address's MSB is 0x01 and its LSB is 0x23.

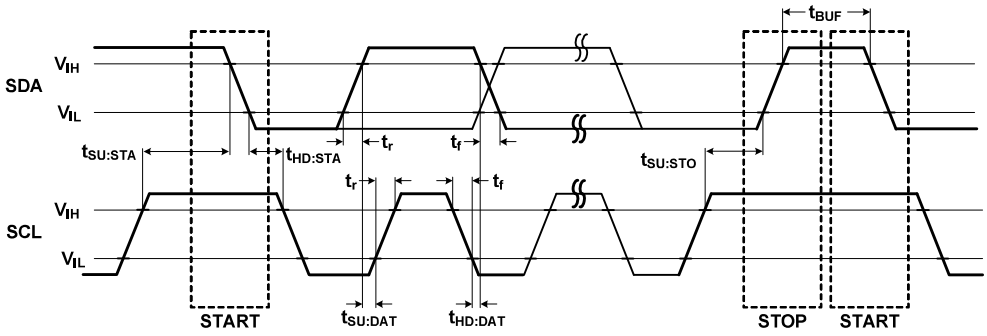


FIGURE 25. I²C TIMING DEFINITIONS

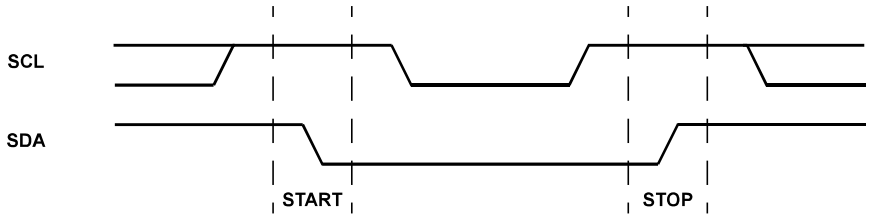


FIGURE 26. VALID START AND STOP CONDITIONS

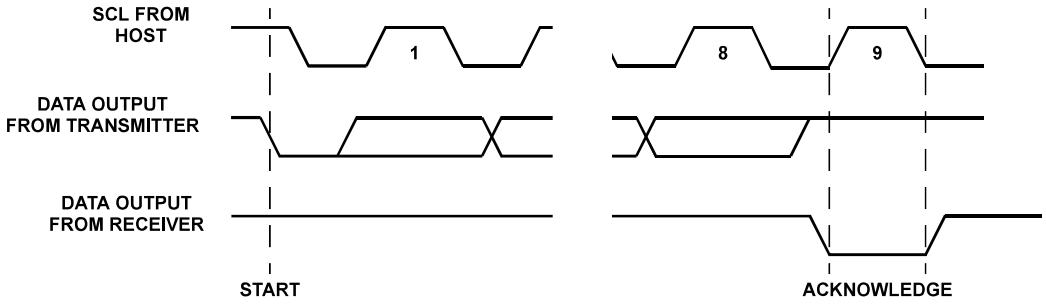


FIGURE 27. ACKNOWLEDGE RESPONSE FROM RECEIVER

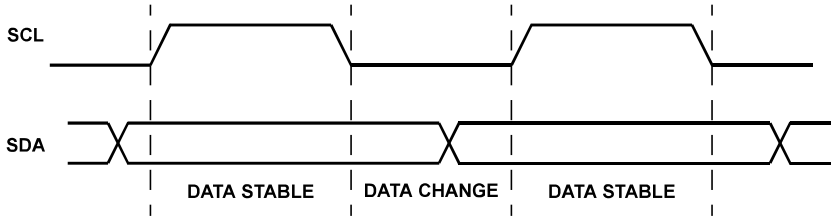
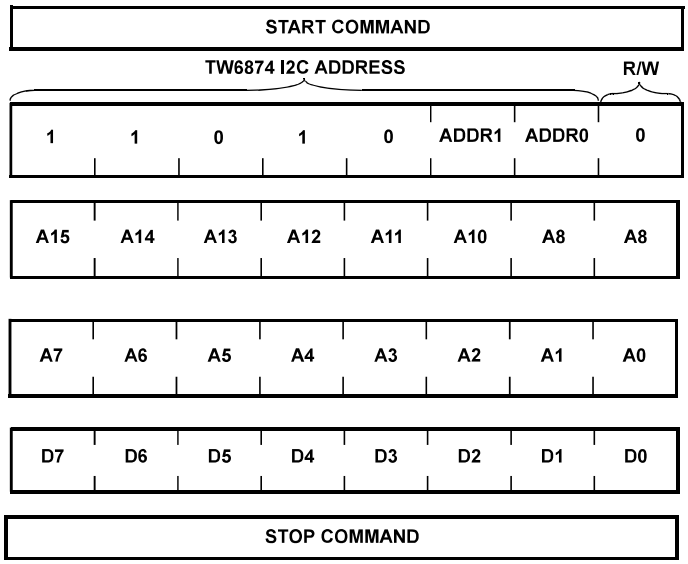


FIGURE 28. VALID DATA CHANGES ON THE SDA BUS



Signals the beginning of an I²C transaction

TW6874 Device Select Address Write

The first 7 bits of the first byte select the TW6874 on the I²C bus at the address determined by the ADDR pins. R/$\overline{W}$ = 0, indicating that the next transaction will be a write.

TW6874 Register Address MSB Write

This is the address MSB of the TW6874's internal configuration

TW6874 Register Address LSB Write

This is the address LSB of the TW6874's internal configuration

TW6874 Register Data Write

This is the data to be written to the selected configuration register.

Signals the Ending of the I²C Transaction

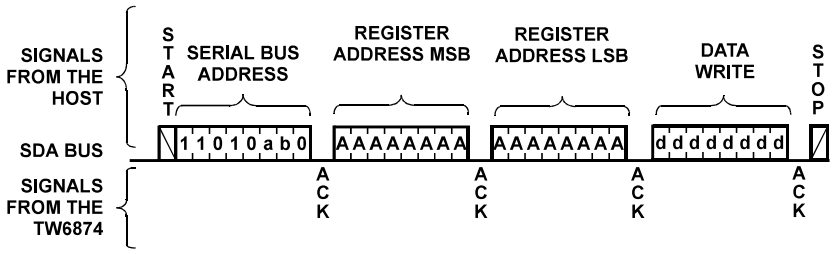
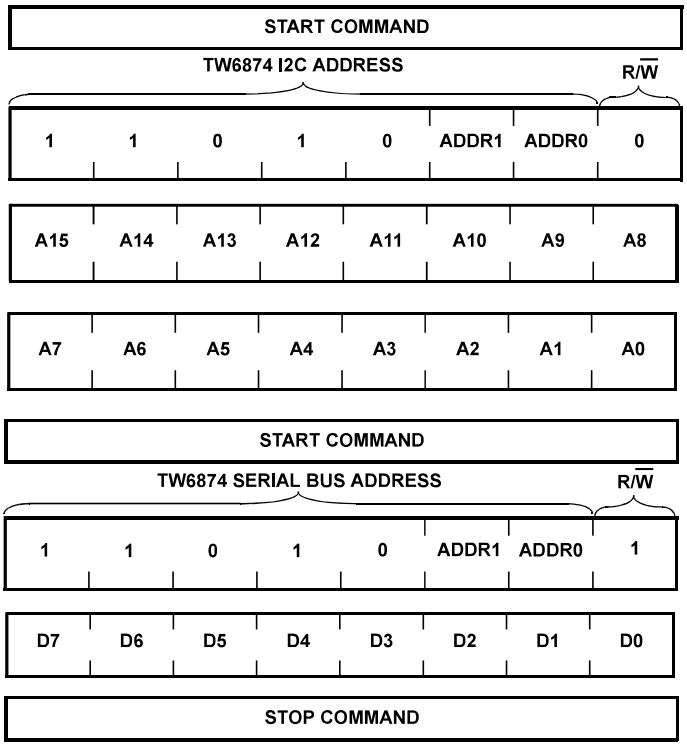


FIGURE 29. CONFIGURATION REGISTER WRITE



Signals the Beginning of an I²C transaction

TW6874 Device Select Address Write

The first 7 bits of the first byte select the TW6874 on the I²C bus at the address determined by the ADDR pins. R/$\overline{W}$ = 0, indicating the

TW6874 Register Address MSB Write

This is the address MSB of the TW6874's internal configuration

TW6874 Register Address LSB Write

This is the address LSB of the TW6874's internal configuration

Ends the Previous Transaction and Starts a New One

TW6874 Device Select Address Write

The first 7 bits of the first byte select the TW6874 on the I²C bus at the address determined by the ADDR pins. R/$\overline{W}$ = 1, indicating next transaction(s) will be a read.

TW6874 Register Data Read(s)

This is the data read from the selected configuration register.

Signals the Ending of the I²C Transaction

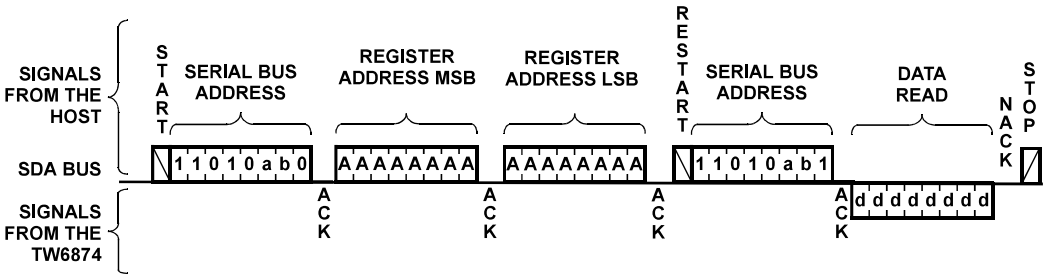


FIGURE 30. CONFIGURATION REGISTER READ

SPI Communication Interface

The TW6874 optionally uses an SPI serial bus for communication with its host. SPI is enabled by setting SPIB low. The TW6874 operates as a bus slave. The SPI serial bus interface consists of 4 pins: SCL, MISO (full pin name is MISO_ADDR1), MOSI (full pin name is MOSI_SDA) and CSB (full pin name is CSB_ADDR0). SCL is the Serial Clock line, driven by the host. MISO is the Master In Slave Out line, driven by the TW6874 to send data to the host. MOSI is the Master Out Slave In line, driven by the host, to send data to the slave. CSB is the Chip-select line, driven low to select the TW6874 for communication.

An SPI transaction consists of two or more 16-bit words. The first word sends the command/address. The second and subsequent words are write or read data. The command/address word is decoded as shown in Table 6.

TABLE 6. SPI COMMAND/ADDRESS FORMAT

15	14:13	12	11:8	7:0
R/$\overline{W}$	0:0	Auto Increment	Address MSB	Address LSB

When the auto increment bit is set low, each address/command word is followed by a single data word. When the auto increment bit it is set to high, the address/command word is followed by consecutive data words as long as the host controller holds the CSB pin low. In the auto increment mode, each 16-bit data word is written to or read from the next 16-bit location in the register space. Each 16-bit word needs to be separated by periods of at least t_{WRITE} for writes and t_{READ} for reads. These wait periods includes the time between address/command word and the first data word.

The serial address/data is sent MSB first from the host controller and registered using the positive edge of SCL in TW6874. The TW6874 sends out the read data at the negative edge of the SCL so that the host controller can register it using the positive edge of SCL. Note that the MSB bit of read data is ready before the first SCL positive edge of the read phase.

Each configuration register is accessed via a 12-bit address. The upper four bits is the page; the lower byte is the address on the page. The register map lists each register address in a 12-bit format, for example: 0x123. Hence this register address's MSB is 0x1 and its LSB is 0x23.

It is important to note that the TW6874's SPI interface operates in 16-bit data mode whereas the I^2C interface operates in 8-bit data mode. The register maps tabulates each register as 8-bit registers in LSB first format. However, reading/writing using SPI always occurs in MSB first format. Hence, reading from register 0x000 returns the byte at 0x001 first, followed by the byte at 0x000. Similarly, reading from register 0x001 returns the byte at 0x002 first, followed by the byte at 0x001. It is advised to read/write 16-bit SPI data only from/to even-numbered registers to prevent confusion.

Figures 31 and 32 show the SPI serial interface Write and Read cycle timing diagrams respectively.

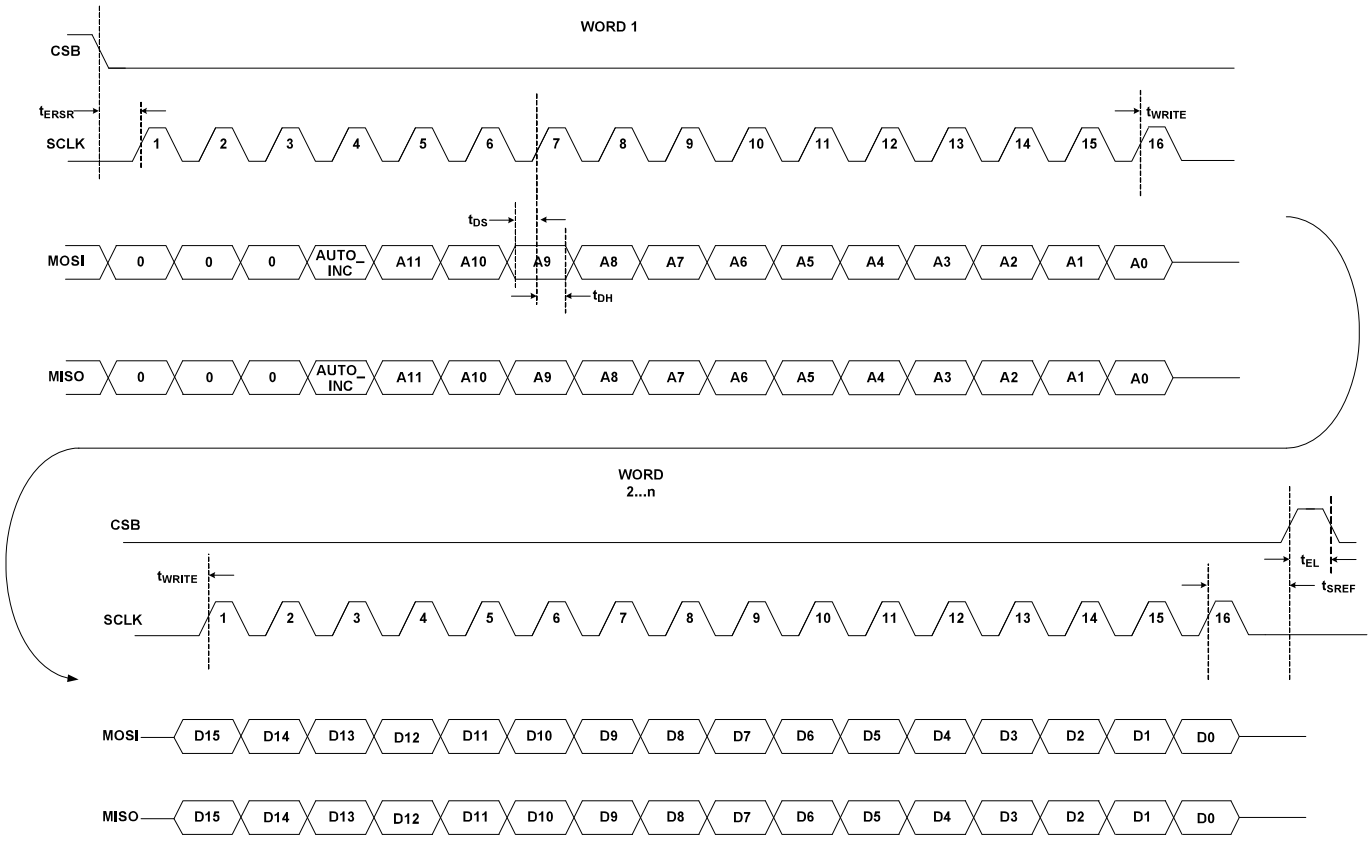


FIGURE 31. SPI SERIAL INTERFACE WRITE CYCLE TIMING DIAGRAM

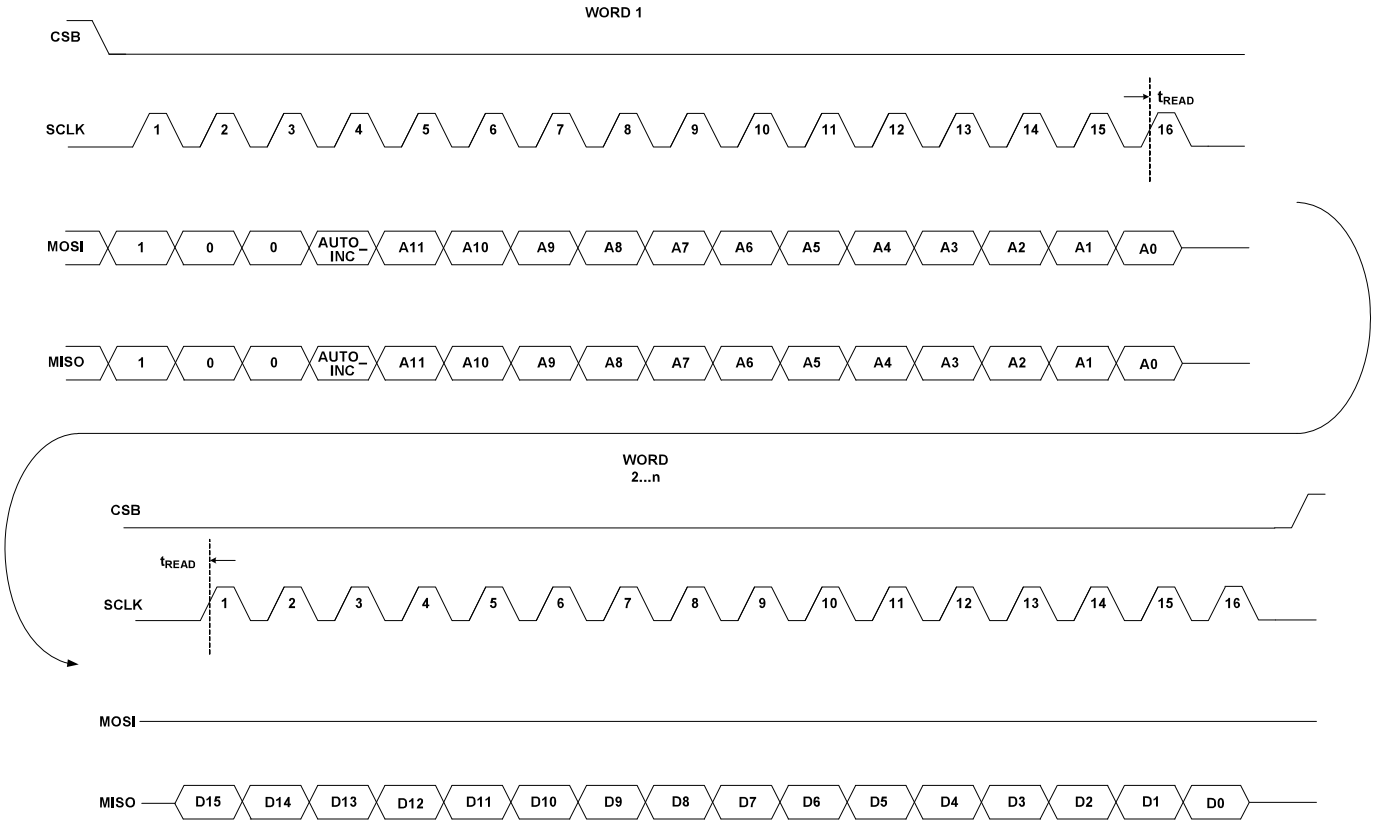


FIGURE 32. SPI SERIAL INTERFACE READ CYCLE TIMING DIAGRAM

Cascade Mode

The SPI bus can be used in cascade mode where multiple TW6874 parts share a common SCL clock and have their own CSB controlled by the host system as shown in Figure 33. The MISO outputs and MOSI inputs can be connected in serial fashion and only the parts with the active CSB pin will be accessed. The MISO output is hardwired to the MOSI input when the transaction is not in the read data phase. This allows parts with active CSB to accept command/address as well as write data simultaneously. In a read transaction, only one CSB should be active to prevent bus collision.

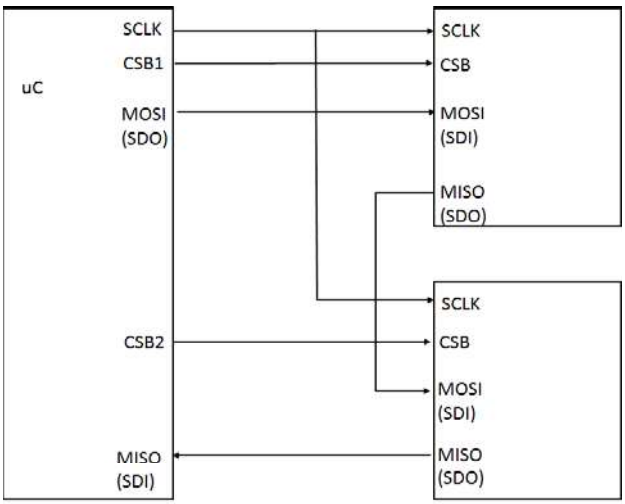


FIGURE 33. INTERFACING TO MULTIPLE SPI SLAVES

Register Map

Status

TABLE 7. SDI1STATUS: SDI CH1 STATUS LSB . . . . . READ-ONLY, ADDR = 0x000

BIT	NAME	BIT DEFINITION	DEFAULT
7	PLL_DIRAC_LOCK1	Dirac PLL locked status (valid only in Dirac mode) 0: Not locked 1: Locked	-
6	T_LOCKED1	Transport format detected by examining the timing of video 0: Not locked 1: Locked; T_FAMILY register gives valid format	-
5	T_SCAN1	Scan Mode 0: Interlaced 1: Progressive	-
4	CRC_ERR1	CRC error detected 0: No error 1: Error	-
3	Reserved	Reserved	-
2	SDI_MODE_LOCKED1	SDI mode auto detection locked status 0: Not locked 1: Locked	-
1:0	SDI_MODE1	SDI mode 00: HD-SDI 01: SD-SDI (includes VC-2 compressed mode) 1x: Reserved	-

TABLE 8. SDI1STATUS: SDI CH1 STATUS MSB . . . . . READ-ONLY, ADDR = 0x001

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	T_RATE1	Frame rate 0000: None 0010: 23.98Hz 0011: 24Hz 0100: 47.95Hz 0101: 25Hz 0110: 29.97Hz 0111: 30Hz 1000: 48Hz 1001: 50Hz 1010: 59.94Hz 1011: 60Hz Unlisted: Undefined	-
3:0	T_FAMILY1	Video format family being detected 0000: ST 274 1920x1080 0001: ST 296 1280x720 0010: ST 2048-2 2048x1080 0011: ST 295 1000: NTSC 720x486 1001: PAL 720x576 1111: Unknown Unlisted: Undefined	-

TABLE 9. SDI2STATUS: SDI CH2 STATUS LSB . . . . . READ-ONLY, ADDR = 0x002

BIT	NAME	BIT DEFINITION	DEFAULT
7	PLL_DIRAC_LOCK2	Dirac PLL locked status (valid only in Dirac mode) 0: Not locked 1: Locked	-
6	T_LOCKED2	Transport format detected by examining the timing of video 0: Not locked 1: Locked; T_FAMILY register gives valid format	-
5	T_SCAN2	Scan Mode 0: Interlaced 1: Progressive	-
4	CRC_ERR2	CRC error detected 0: No error 1: Error	-
3	Reserved	Reserved	-
2	SDI_MODE_LOCKED2	SDI mode auto detection locked status 0: Not locked 1: Locked	-
1:0	SDI_MODE2	SDI mode 00: HD-SDI 01: SD-SDI (includes VC-2 compressed mode) 1x: Reserved	-

TABLE 10. SDI2STATUS: SDI CH2 STATUS MSB . . . . . READ-ONLY, ADDR = 0x003

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	T_RATE2	Frame rate 0000: None 0010: 23.98Hz 0011: 24Hz 0100: 47.95Hz 0101: 25Hz 0110: 29.97Hz 0111: 30Hz 1000: 48Hz 1001: 50Hz 1010: 59.94Hz 1011: 60Hz Unlisted: Undefined	-
3:0	T_FAMILY2	Video format family being detected 0000: ST 274 1920x1080 0001: ST 296 1280x720 0010: ST 2048-2 2048x1080 0011: ST 295 1000: NTSC 720x486 1001: PAL 720x576 1111: Unknown Unlisted: Undefined	-

TABLE 11. SDI3STATUS: SDI CH3 STATUS LSB . . . . . READ-ONLY, ADDR = 0x004

BIT	NAME	BIT DEFINITION	DEFAULT
7	PLL_DIRAC_LOCK3	Dirac PLL locked status (valid only in Dirac mode) 0: Not locked 1: Locked	-
6	T_LOCKED3	Transport format detected by examining the timing of video 0: Not locked 1: Locked; T_FAMILY register gives valid format	-
5	T_SCAN3	Scan Mode 0: Interlaced 1: Progressive	-
4	CRC_ERR3	CRC error detected 0: No error 1: Error	-
3	Reserved	Reserved	-
2	SDI_MODE_LOCKED3	SDI mode auto detection locked status 0: Not locked 1: Locked	-
1:0	SDI_MODE3	SDI mode 00: HD-SDI 01: SD-SDI (includes VC-2 compressed mode) 1x: Reserved	-

TABLE 12. SDI3STATUS: SDI CH3 STATUS MSB . . . . . READ-ONLY, ADDR = 0x005

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	T_RATE3	Frame rate 0000: None 0010: 23.98Hz 0011: 24Hz 0100: 47.95Hz 0101: 25Hz 0110: 29.97Hz 0111: 30Hz 1000: 48Hz 1001: 50Hz 1010: 59.94Hz 1011: 60Hz Unlisted: Undefined	-
3:0	T_FAMILY3	Video format family being detected 0000: ST 274 1920x1080 0001: ST 296 1280x720 0010: ST 2048-2 2048x1080 0011: ST 295 1000: NTSC 720x486 1001: PAL 720x576 1111: Unknown Unlisted: Undefined	-

TABLE 13. SDI4STATUS: SDI CH4 STATUS LSB . . . . . READ-ONLY, ADDR = 0x006

BIT	NAME	BIT DEFINITION	DEFAULT
7	PLL_DIRAC_LOCK4	Dirac PLL locked status (valid only in Dirac mode) 0: Not locked 1: Locked	-
6	T_LOCKED4	Transport format detected by examining the timing of video 0: Not locked 1: Locked; T_FAMILY register gives valid format	-
5	T_SCAN4	Scan Mode 0: Interlaced 1: Progressive	-
4	CRC_ERR4	CRC error detected 0: No error 1: Error	-
3	Reserved	Reserved	-
2	SDI_MODE_LOCKED4	SDI mode auto detection locked status 0: Not locked 1: Locked	-
1:0	SDI_MODE4	SDI mode 00: HD-SDI 01: SD-SDI (includes VC-2 compressed mode) 1x: Reserved	-

TABLE 14. SDI4STATUS: SDI CH4 STATUS MSB . . . . . READ-ONLY, ADDR = 0x007

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	T_RATE4	Frame rate 0000: None 0010: 23.98Hz 0011: 24Hz 0100: 47.95Hz 0101: 25Hz 0110: 29.97Hz 0111: 30Hz 1000: 48Hz 1001: 50Hz 1010: 59.94Hz 1011: 60Hz Unlisted: Undefined	-
3:0	T_FAMILY4	Video format family being detected 0000: ST 274 1920x1080 0001: ST 296 1280x720 0010: ST 2048-2 2048x1080 0011: ST 295 1000: NTSC 720x486 1001: PAL 720x576 1111: Unknown Unlisted: Undefined	-

Source Resolution

TABLE 15. SRC_HSIZE_1L: CH1 SOURCE HOR SIZE LSB . . . . . READ-ONLY, ADDR = 0x010

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_HSIZE_1L	SDI input horizontal size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 16. SRC_HSIZE_1M: CH1 SOURCE HOR SIZE MSB . . . . . READ-ONLY, ADDR = 0x011

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_HSIZE_1M	SDI input horizontal size MSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 17. SRC_HSIZE_2L: CH2 SOURCE HOR SIZE LSB. . . . . READ-ONLY, ADDR = 0x012

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_HSIZE_2L	SDI input horizontal size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 18. SRC_HSIZE_2M: CH2 SOURCE HOR SIZE MSB . . . . . READ-ONLY, ADDR = 0x013

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_HSIZE_2M	SDI input horizontal size MSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 19. SRC_HSIZE_3L: CH3 SOURCE HOR SIZE LSB . . . . . READ-ONLY, ADDR = 0x014

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_HSIZE_3L	SDI input horizontal size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 20. SRC_HSIZE_3M: CH3 SOURCE HOR SIZE MSB . . . . . READ-ONLY, ADDR = 0x015

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_HSIZE_3M	SDI input horizontal size MSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 21. SRC_HSIZE_4L: CH4 SOURCE HOR SIZE LSB . . . . . READ-ONLY, ADDR = 0x016

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_HSIZE_4L	SDI input horizontal size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 22. SRC_HSIZE_4M: CH4 SOURCE HOR SIZE MSB . . . . . READ-ONLY, ADDR = 0x017

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_HSIZE_4M	SDI input horizontal size MSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 23. SRC_VSIZE_1L: CH1 SOURCE VERT SIZE LSB . . . . . READ-ONLY, ADDR = 0x018

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_VSIZE_1L	SDI input vertical size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 24. SRC_VSIZE_1M: CH1 SOURCE VERT SIZE MSB . . . . . READ-ONLY, ADDR = 0x019

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_VSIZE_1M	SDI input horizontal size MSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 25. SRC_VSIZE_2L: CH2 SOURCE VERT SIZE LSB . . . . . READ-ONLY, ADDR = 0x01A

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_VSIZE_2L	SDI input vertical size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 26. SRC_VSIZE_2M: CH2 SOURCE VERT SIZE MSB . . . . . READ-ONLY, ADDR = 0x01B

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_VSIZE_2M	SDI input vertical size MSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 27. SRC_VSIZE_3L: CH3 SOURCE VERT SIZE LSB . . . . . READ-ONLY, ADDR = 0x01C

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_VSIZE_3L	SDI input vertical size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 28. SRC_VSIZE_3M: CH3 SOURCE VERT SIZE MSB . . . . . READ-ONLY, ADDR = 0x01D

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_VSIZE_3M	SDI input vertical size MSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 29. SRC_VSIZE_4L: CH4 SOURCE VERT SIZE LSB . . . . . READ-ONLY, ADDR = 0x01E

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SRC_VSIZE_4L	SDI input vertical size LSB. This size is determined by the detected video format in T_FAMILY.	-

TABLE 30. SRC_VSIZE_4M: CH4 SOURCE VERT SIZE MSB . . . . . READ-ONLY, ADDR = 0x01F

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	-
2:0	SRC_VSIZE_4M	SDI input vertical size MSB. This size is determined by the detected video format in T_FAMILY.	-

Status and SDI Enable

TABLE 31. MISC_STATUS: MISC. STATUS ..... READ-ONLY, ADDR = 0x020

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	-
3:0	Reserved	Reserved	-

TABLE 32. DIV_M_STATUS: DIVM STATUS ..... READ-ONLY, ADDR = 0x021

BIT	NAME	BIT DEFINITION	DEFAULT
7	INVALID_DIVM4	Invalid DIV 1.001 detection for CH4. DIVM4 ignored. Normally this bit is set during SD/DIRAC mode 0: Valid 1: Invalid	-
6	INVALID_DIVM3	Invalid DIV 1.001 detection for CH3. DIVM3 ignored. Normally this bit is set during SD/DIRAC mode 0: Valid 1: Invalid	-
5	INVALID_DIVM2	Invalid DIV 1.001 detection for CH2. DIVM2 ignored. Normally this bit is set during SD/DIRAC mode 0: Valid 1: Invalid	-
4	INVALID_DIVM1	Invalid DIV 1.001 detection for CH1. DIVM1 ignored. Normally this bit is set during SD/DIRAC mode 0: Valid 1: Invalid	-
3	DIVM4	Divided by 1.001 frame rate detection for CH4 (HD mode) 0: No 74.25/1.001 detected 1: 74.25/1.001 detected	-
2	DIVM3	Divided by 1.001 frame rate detection for CH3 (HD mode) 0: No 74.25/1.001 detected 1: 74.25/1.001 detected	-
1	DIVM2	Divided by 1.001 frame rate detection for CH2 (HD mode) 0: No 74.25/1.001 detected 1: 74.25/1.001 detected	-
0	DIVM1	Divided by 1.001 frame rate detection for CH1 (HD mode) 0: No 74.25/1.001 detected 1: 74.25/1.001 detected	-

TABLE 33. T_SCAN_MODE: HD SCAN MODE ..... READ-ONLY, ADDR = 0x031

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	-

TABLE 34. SDI_MODE_EN: SDI MODE ENABLE LSB ..... READ-WRITE, ADDR = 0x032

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	SDI_MODE_EN3	[7]: SD, [6]: HD for CH3 0: Disable 1: Enable	11
5	Reserved	Reserved	1
4:3	SDI_MODE_EN2	[4]: SD, [3]: HD for CH2 0: Disable 1: Enable	11

TABLE 34. SDI_MODE_EN: SDI MODE ENABLE LSB . . . . . READ-WRITE, ADDR = 0x032 (Continued)

BIT	NAME	BIT DEFINITION	DEFAULT
2	Reserved	Reserved	1
1:0	SDI_MODE_EN1	[1]: SD, [0]: HD for CH1 0: Disable 1: Enable	11

TABLE 35. SDI_MASK_EN: SDI MODE ENABLE MSB . . . . . READ-WRITE, ADDR = 0x033

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3	Reserved	Reserved	1
2:1	SDI_MODE_EN4	[2]: SD, [1]: HD for CH4 0: Disable 1: Enable	11
0	Reserved	Reserved	1

Control

TABLE 36. SDI_CTL: SDI CONTROL LSB . . . . . READ-WRITE, ADDR = 0x034

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0xF
3	CHID_EN4	Embed channel ID into BT.1120 sync code for CH4. Setting this bit will put the Channel ID into the XYZ bit[1:0] of SAV/EAV in the BT.656/BT.1120 output. 0: Disabled 1: Enabled	1
2	CHID_EN3	Embed channel ID into BT.1120 sync code for CH3. Setting this bit will put the Channel ID into the XYZ bit[1:0] of SAV/EAV in the BT.656/BT.1120 output. 0: Disabled 1: Enabled	1
1	CHID_EN2	Embed channel ID into BT.1120 sync code for CH2. Setting this bit will put the Channel ID into the XYZ bit[1:0] of SAV/EAV in the BT.656/BT.1120 output. 0: Disabled 1: Enabled	1
0	CHID_EN1	Embed channel ID into BT.1120 sync code for CH1. Setting this bit will put the Channel ID into the XYZ bit[1:0] of SAV/EAV in the BT.656/BT.1120 output. 0: Disabled 1: Enabled	1

TABLE 37. SDI_CTL: SDI CONTROL MSB . . . . . READ-WRITE, ADDR = 0x035

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3:0	Reserved	Reserved	0x0

TABLE 38. CRC_DITHER: CRC AND DITHER CONTROL . . . . . READ-WRITE, ADDR = 0x038

BIT	NAME	BIT DEFINITION	DEFAULT
7	CRC_CLEAR4	Clear CRC counter for CH4 0: No operation 1: Clear	0
6	CRC_CLEAR3	Clear CRC counter for CH3 0: No operation 1: Clear	0
5	CRC_CLEAR2	Clear CRC counter for CH2 0: No operation 1: Clear	0
4	CRC_CLEAR1	Clear CRC counter for CH1 0: No operation 1: Clear	0
3	DITHER_EN4	Enable dithering for CH4 0: Disabled 1: Enabled	0
2	DITHER_EN3	Enable dithering for CH3 0: Disabled 1: Enabled	0
1	DITHER_EN2	Enable dithering for CH2 0: Disabled 1: Enabled	0
0	DITHER_EN1	Enable dithering for CH1 0: Disabled 1: Enabled	0

TABLE 39. CRC_MASK_CTRL: CRC MASK CONTROL . . . . . READ-WRITE, ADDR = 0x039

BIT	NAME	BIT DEFINITION	DEFAULT
7	CRC_CNT4_EN	Enable CRC counter for CH4 0: Stop CRC counter 1: Enable CRC counter	0
6	CRC_CNT3_EN	Enable CRC counter for CH3 0: Stop CRC counter 1: Enable CRC counter	0
5	CRC_CNT2_EN	Enable CRC counter for CH2 0: Stop CRC counter 1: Enable CRC counter	0
4	CRC_CNT1_EN	Enable CRC counter for CH1 0: Stop CRC counter 1: Enable CRC counter	0
3	CRC_MSK4_EN	Mask CRC error for CH4 0: No operation 1: The CRC counters (CRC_CNT4) will be forced to “0”.	0
2	CRC_MSK3_EN	Mask CRC error for CH3 0: No operation 1: The CRC counters (CRC_CNT3) will be forced to “0”.	0
1	CRC_MSK2_EN	Mask CRC error for CH2 0: No operation 1: The CRC counters (CRC_CNT2) will be forced to “0”.	0
0	CRC_MSK1_EN	Mask CRC error for CH1 0: No operation 1: The CRC counters (CRC_CNT1) will be forced to “0”.	0

Reset

TABLE 40. RESETMAIN: MAIN RESET LSB . . . . . READ-WRITE, ADDR = 0x03A

BIT	NAME	BIT DEFINITION	DEFAULT
7	RSTNPORT4	Reset video output port for VD4. This bit is not self-cleared. It needs to be manually set back to 1. Note that the default value is 0 and thus needs to be released after initialization to enable the video output port. 0: Reset 1: Normal operation	1
6	RSTNPORT3	Reset video output port for VD3. This bit is not self-cleared. It needs to be manually set back to 1. Note that the default value is 0 and thus needs to be released after initialization to enable the video output port. 0: Reset 1: Normal operation	1
5	RSTNPORT2	Reset video output port for VD2. This bit is not self-cleared. It needs to be manually set back to 1. Note that the default value is 0 and thus needs to be released after initialization to enable the video output port. 0: Reset 1: Normal operation	1
4	RSTNPORT1	Reset video output port for VD1. This bit is not self-cleared. It needs to be manually set back to 1. Note that the default value is 0 and thus needs to be released after initialization to enable the video output port. 0: Reset 1: Normal operation	1
3	RSTNSDI4	Reset SDI audio AFE and SDI receiver for CH4. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
2	RSTNSDI3	Reset SDI audio AFE and SDI receiver for CH3. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
1	RSTNSDI2	Reset SDI audio AFE and SDI receiver for CH2. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
0	RSTNSDI1	Reset SDI audio AFE and SDI receiver for CH1. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1

TABLE 41. RESETMAIN: MAIN RESET MSB . . . . . READ-WRITE, ADDR = 0x03B

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	Reserved	Reserved	0x00
0	RSTMAIN	Whole device reset (self cleared). When writing to this register, the whole device will reset. No manual reset clear is needed. 0: Normal operation 1: Reset	0

TABLE 42. RESETCORE: CORE RESET LSB . . . . . READ-WRITE, ADDR = 0x03C

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0xF
3	RSTNSDI4	Reset ancillary detection/extraction for CH4. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
2	RSTNSDI3	Reset ancillary detection/extraction for CH3. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
1	RSTNSDI2	Reset ancillary detection/extraction for CH2. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
0	RSTNSDI1	Reset ancillary detection/extraction for CH1. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1

TABLE 43. RESETCORE: CORE RESET MSB . . . . . READ-WRITE, ADDR = 0x03D

BIT	NAME	BIT DEFINITION	DEFAULT
7	RSTNCDR148_4	CDR148 reset for CH4. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
6	RSTNCDR148_3	CDR148 reset for CH3. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
5	RSTNCDR148_2	CDR148 reset for CH2. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
4	RSTNCDR148_1	CDR148 reset for CH1. This bit is not self-cleared. It needs to be manually set back to 1. 0: Reset 1: Normal operation	1
3:0	Reserved	Reserved	0xF

Output Port Configuration

TABLE 44. CRC_CNT1: CH1 CRC ERROR COUNTER. . . . . READ-ONLY, ADDR = 0x040

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	CRC_CNT1	CRC error counter for CH1	0x00

TABLE 45. CRC_CNT2: CH2 CRC ERROR COUNTER. . . . . READ-ONLY, ADDR = 0x041

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	CRC_CNT2	CRC error counter for CH2	0x00

TABLE 46. CRC_CNT3: CH3 CRC ERROR COUNTER. . . . . READ-ONLY, ADDR = 0x042

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	CRC_CNT3	CRC error counter for CH3	0x00

TABLE 47. CRC_CNT4: CH4 CRC ERROR COUNTER . . . . . READ-ONLY, ADDR = 0x043

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	CRC_CNT4	CRC error counter for CH4	0x00

TABLE 48. VP1_CTL: VIDEO PORT 1 CONTROL . . . . . READ-WRITE, ADDR = 0x044

BIT	NAME	BIT DEFINITION	DEFAULT
7	VP1OE	Video port 1 output enable 0: Tri-state 1: Normal output	0
6:3	Reserved	Reserved	0x0
2	VP1ORDER	C or Y component order in HD 8-bit mode 0: C component first 1: Y component first Note: In HD 16-bit mode, Y is on the lower byte and C is on the upper byte. In HD 8-bit mode, both the upper and lower byte carry the same data.	0
1	Reserved	Reserved	0
0	VP1HD8BIT	Select Video port 1 output bus width. Valid for HD 8-bit modes only. 0: 16-bit 1: 8-bit (HD 8-bit mode)	0

TABLE 49. VP2_CTL: VIDEO PORT 2 CONTROL . . . . . READ-WRITE, ADDR = 0x046

BIT	NAME	BIT DEFINITION	DEFAULT
7	VP2OE	Video port 2 output enable 0: Tri-state 1: Normal output	0
6:3	Reserved	Reserved	0x0
2	VP2ORDER	C or Y component order in HD 8-bit mode 0: C component first 1: Y component first Note: In HD 16-bit mode, Y is on the lower byte and C is on the upper byte. In HD 8-bit mode, both the upper and lower byte carry the same data.	0
1	Reserved	Reserved	0
0	VP2HD8BIT	Select Video port 2 output bus width. Valid for HD 8-bit modes only. 0: 16-bit 1: 8-bit (HD 8-bit mode)	0

TABLE 50. VP3_CTL: VIDEO PORT 3 CONTROL . . . . . READ-WRITE, ADDR = 0x048

BIT	NAME	BIT DEFINITION	DEFAULT
7	VP3OE	Video port 3 output enable 0: Tri-state 1: Normal output	0
6:3	Reserved	Reserved	0x0
2	VP3ORDER	C or Y component order in HD 8-bit mode 0: C component first 1: Y component first Note: In HD 16-bit mode, Y is on the lower byte and C is on the upper byte. In HD 8-bit mode, both the upper and lower byte carry the same data.	0
1	Reserved	Reserved	0
0	VP3HD8BIT	Select Video port 3 output bus width. Valid for HD 8-bit modes only. 0: 16-bit 1: 8-bit (HD 8-bit mode)	0

TABLE 51. VP4_CTL: VIDEO PORT 4 CONTROL . . . . . READ-WRITE, ADDR = 0x04A

BIT	NAME	BIT DEFINITION	DEFAULT
7	VP4OE	Video port 4 output enable 0: Tri-state 1: Normal output	0
6:3	Reserved	Reserved	0x0
2	VP4ORDER	C or Y component order in HD 8-bit mode 0: C component first 1: Y component first Note: In HD 16-bit mode, Y is on the lower byte and C is on the upper byte. In HD 8-bit mode, both the upper and lower byte carry the same data.	0
1	Reserved	Reserved	0
0	VP4HD8BIT	Select Video port 4 output bus width. Valid for HD 8-bit modes only. 0: 16-bit 1: 8-bit (HD 8-bit mode)	0

TABLE 52. DIRAC_CLR_UNLOCK: CLEAR DIRAC UNLOCK FLAG. . . . . READ-WRITE, ADDR = 0x04C

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3	DIRAC_CLR_UNLOCK4	Set “1” to clear Dirac unlock flag for CH4 in DIRAC_UNLOCK_FLAG4. This bit is not self-cleared.	0
2	DIRAC_CLR_UNLOCK3	Set “1” to clear Dirac unlock flag for CH3 in DIRAC_UNLOCK_FLAG3. This bit is not self-cleared.	0
1	DIRAC_CLR_UNLOCK2	Set “1” to clear Dirac unlock flag for CH2 in DIRAC_UNLOCK_FLAG2. This bit is not self-cleared.	0
0	DIRAC_CLR_UNLOCK1	Set “1” to clear Dirac unlock flag for CH1 in DIRAC_UNLOCK_FLAG1. This bit is not self-cleared.	0

TABLE 53. DIRAC_UNLOCK_FLAG: DIRAC UNLOCK STATUS . . . . . READ-ONLY, ADDR = 0x04D

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	-
3	DIRAC_UNLOCK_FLAG4	Indicate Dirac lost frame lock for CH4 0: Frame locked 1: Frame unlocked	-
2	DIRAC_UNLOCK_FLAG3	Indicate Dirac lost frame lock for CH3 0: Frame locked 1: Frame unlocked	-
1	DIRAC_UNLOCK_FLAG2	Indicate Dirac lost frame lock for CH2 0: Frame locked 1: Frame unlocked	-
0	DIRAC_UNLOCK_FLAG1	Indicate Dirac lost frame lock for CH1 0: Frame locked 1: Frame unlocked	-

TABLE 54. DIRAC_ERR_CTRL: DIRAC ERROR CONTROL. . . . . READ-WRITE, ADDR = 0x04E

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	Reserved	Reserved	000
4	DIRAC_ERR_RESET_SRC	Auto Dirac error reset source 0: Not selected (No Dirac error detected) 1: Select Dirac unlock as the source	0
3:1	Reserved	Reserved	000
0	DIRAC_ERR_RESET_EN	Enable auto Dirac error reset 0: Disable 1: Enable	0

TABLE 55. DIRACEN: DIRAC ENABLE. . . . . READ-WRITE, ADDR = 0x054

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3	DIRAC_EN4	Enable Dirac for CH4 0: Disabled 1: Enabled	0
2	DIRAC_EN3	Enable Dirac for CH3 0: Disabled 1: Enabled	0
1	DIRAC_EN2	Enable Dirac for CH2 0: Disabled 1: Enabled	0
0	DIRAC_EN1	Enable Dirac for CH1 0: Disabled 1: Enabled	0

TABLE 56. DIRAC VIDEO FORMATS

0: 720p, 60 frames/s 1: 720p, 50 frames/s 2: 1080i, 60 fields/s 3: 1080i. 50 fields/s 4: Reserved 5: Reserved 6: 1080p, 30 frames/s 7: 1080p, 25 frames/s

TABLE 57. DIRACFMT: DIRAC FORMAT LSB . . . . . READ-WRITE, ADDR = 0x055

BIT	NAME	BIT DEFINITION	DEFAULT
7	Reserved	Reserved	0
6:4	DIRAC_FMT2	Dirac format for CH2. See Table 56 for formats.	000
3	Reserved	Reserved	0
2:0	DIRAC_FMT1	Dirac format for CH1. See Table 56 for formats.	000

TABLE 58. DIRACFMT: DIRAC FORMAT MSB. . . . . READ-WRITE, ADDR = 0x056

BIT	NAME	BIT DEFINITION	DEFAULT
7	Reserved	Reserved	1
6:4	DIRAC_FMT4	Dirac format for CH4. See Table 56 for formats.	000
3	Reserved	Reserved	0
2:0	DIRAC_FMT3	Dirac format for CH3. See Table 56 for formats.	000

TABLE 59. PRBS_DIRAC_STATUS: PRBS AND DIRAC STATUS . . . . . READ-ONLY, ADDR = 0x057

BIT	NAME	BIT DEFINITION	DEFAULT
7	PRBS_ERR_RESULT4	PRBS error checking result for CH4 0: Unavailable 1: Available	-
6	PRBS_ERR_RESULT3	PRBS error checking result for CH3 0: Unavailable 1: Available	-
5	PRBS_ERR_RESULT2	PRBS error checking result for CH2 0: Unavailable 1: Available	-
4	PRBS_ERR_RESULT1	PRBS error checking result for CH1 0: Unavailable 1: Available	-
3	DIRAC_HAS_HEADER4	The incoming Dirac stream for CH4 contains proprietary header after EAV 0: Doesn't contain the header 1: Contains the header	-
2	DIRAC_HAS_HEADER3	The incoming Dirac stream for CH3 contains proprietary header after EAV 0: Doesn't contain the header 1: Contains the header	-
1	DIRAC_HAS_HEADER2	The incoming Dirac stream for CH2 contains proprietary header after EAV 0: Doesn't contain the header 1: Contains the header	-
0	DIRAC_HAS_HEADER1	The incoming Dirac stream for CH1 contains proprietary header after EAV 0: Doesn't contain the header 1: Contains the header	-

Link Checker Configuration

TABLE 60. PRBSMODE: PRBS MODE LSB. . . . . READ-WRITE, ADDR = 0x058

BIT	NAME	BIT DEFINITION	DEFAULT
7	PRBS_PAT4	PRBS pattern for CH4 0: PRBS23 1: PRBS7	0
6	PRBS_PAT3	PRBS pattern for CH3 0: PRBS23 1: PRBS7	0
5	PRBS_PAT2	PRBS pattern for CH2 0: PRBS23 1: PRBS7	0
4	PRBS_PAT1	PRBS pattern for CH1 0: PRBS23 1: PRBS7	0
3	PRBS_EN4	PRBS check enable for CH4 0: Disabled 1: Enabled	0
2	PRBS_EN3	PRBS check enable for CH3 0: Disabled 1: Enabled	0
1	PRBS_EN2	PRBS check enable for CH2 0: Disabled 1: Enabled	0
0	PRBS_EN1	PRBS check enable for CH1 0: Disabled 1: Enabled	0

TABLE 61. PRBSMODE: PRBS MODE MSB . . . . . READ-WRITE, ADDR = 0x059

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	PRBS_RATE4	PRBS rate for CH4 00: HD 01: SD 1x: Reserved	00
5:4	PRBS_RATE3	PRBS rate for CH3 00: HD 01: SD 1x: Reserved	00
3:2	PRBS_RATE2	PRBS rate for CH2 00: HD 01: SD 1x: Reserved	00
1:0	PRBS_RATE1	PRBS rate for CH1 00: HD 01: SD 1x: Reserved	00

TABLE 62. PRBSCOUNT1: CH1 PRBS ERROR COUNTER. . . . . READ-ONLY, ADDR = 0x05A

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSCOUNT1	PRBS error count for CH1	0x00

TABLE 63. PRBSCOUNT2: CH2 PRBS ERROR COUNTER. . . . . READ-ONLY, ADDR = 0x05B

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSCOUNT2	PRBS error count for CH2	0x00

TABLE 64. PRBSCOUNT3: CH3 PRBS ERROR COUNTER. . . . . READ-ONLY, ADDR = 0x05C

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSCOUNT3	PRBS error count for CH3	0x00

TABLE 65. PRBSCOUNT4: CH4 PRBS ERROR COUNTER. . . . . READ-ONLY, ADDR = 0x05D

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSCOUNT4	PRBS error count for CH4	0x00

TABLE 66. PRBS_CHECK_REQ: PRBS CHECKING REQUEST. . . . . READ-WRITE, ADDR = 0x05E

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3:0	PRBS_CHECK_REQ	Enable PRBS checking task. When the checking period expired, PRBS_ERR_RESULT is set to 1 to indicate the checking is done. 0: No request 1: Request Enable NOTES: 1. [3] = CH4, [2] = CH3, [1] = CH2, [0] = CH1 2. To issue a new request, first clear this bit then set it to “1”.	0x0

TABLE 67. PRBSWINDOW1: CH1 PRBS WINDOW BYTE 0 . . . . . READ-WRITE, ADDR = 0x060

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW1_0	PRBS window for CH1 during which PRBS testing occurs. This is the LSB of the 32-bit window. PRBSWINDOW1[7:0]	0x00

TABLE 68. PRBSWINDOW1: CH1 PRBS WINDOW BYTE 1 . . . . . READ-WRITE, ADDR = 0x061

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW1_1	PRBS window for CH1 during which PRBS testing occurs. This is the 2nd byte of the 32-bit window. PRBSWINDOW1[15:8]	0x00

TABLE 69. PRBSWINDOW1: CH1 PRBS WINDOW BYTE 2 . . . . . READ-WRITE, ADDR = 0x062

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW1_2	PRBS window for CH1 during which PRBS testing occurs. This is the 3rd byte of the 32-bit window. PRBSWINDOW1[23:16]	0x80

TABLE 70. PRBSWINDOW1: CH1 PRBS WINDOW BYTE 3 . . . . . READ-WRITE, ADDR = 0x063

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW1_3	PRBS window for CH1 during which PRBS testing occurs. This is the MSB of the 32-bit window. PRBSWINDOW1[31:24]	0x00

TABLE 71. PRBSWINDOW2: CH2 PRBS WINDOW BYTE 0 . . . . . READ-WRITE, ADDR = 0x064

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW2_0	PRBS window for CH2 during which PRBS testing occurs. This is the LSB of the 32-bit window. PRBSWINDOW2[7:0]	0x00

TABLE 72. PRBSWINDOW2: CH2 PRBS WINDOW BYTE 1 . . . . . READ-WRITE, ADDR = 0x065

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW2_1	PRBS window for CH2 during which PRBS testing occurs. This is the 2nd byte of the 32-bit window. PRBSWINDOW2[15:8]	0x00

TABLE 73. PRBSWINDOW2: CH2 PRBS WINDOW BYTE 2 . . . . . READ-WRITE, ADDR = 0x066

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW2_2	PRBS window for CH2 during which PRBS testing occurs. This is the 3rd byte of the 32-bit window. PRBSWINDOW2[23:16]	0x80

TABLE 74. PRBSWINDOW2: CH2 PRBS WINDOW BYTE 3 . . . . . READ-WRITE, ADDR = 0x067

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW2_3	PRBS window for CH2 during which PRBS testing occurs. This is the MSB of the 32-bit window. PRBSWINDOW2[31:24]	0x00

TABLE 75. PRBSWINDOW3: CH3 PRBS WINDOW BYTE 0 . . . . . READ-WRITE, ADDR = 0x068

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW3_0	PRBS window for CH3 during which PRBS testing occurs. This is the LSB of the 32-bit window. PRBSWINDOW3[7:0]	0x00

TABLE 76. PRBSWINDOW3: CH3 PRBS WINDOW BYTE 1 . . . . . READ-WRITE, ADDR = 0x069

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW3_1	PRBS window for CH3 during which PRBS testing occurs. This is the 2nd byte of the 32-bit window. PRBSWINDOW3[15:8]	0x00

TABLE 77. PRBSWINDOW3: CH3 PRBS WINDOW BYTE 2 . . . . . READ-WRITE, ADDR = 0x06A

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW3_2	PRBS window for CH3 during which PRBS testing occurs. This is the 3rd byte of the 32-bit window. PRBSWINDOW3[23:16]	0x80

TABLE 78. PRBSWINDOW3: CH3 PRBS WINDOW BYTE 3 . . . . . READ-WRITE, ADDR = 0x06B

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW3_3	PRBS window for CH3 during which PRBS testing occurs. This is the MSB of the 32-bit window. PRBSWINDOW3[31:24]	0x00

TABLE 79. PRBSWINDOW4: CH4 PRBS WINDOW BYTE 0 . . . . . READ-WRITE, ADDR = 0x06C

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW4_0	PRBS window for CH4 during which PRBS testing occurs. This is the LSB of the 32-bit window. PRBSWINDOW4[7:0]	0x00

TABLE 80. PRBSWINDOW4: CH4 PRBS WINDOW BYTE 1 . . . . . READ-WRITE, ADDR = 0x06D

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW4_1	PRBS window for CH4 during which PRBS testing occurs. This is the 2nd byte of the 32-bit window. PRBSWINDOW4[15:8]	0x00

TABLE 81. PRBSWINDOW4: CH4 PRBS WINDOW BYTE 2 . . . . . READ-WRITE, ADDR = 0x06E

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW4_2	PRBS window for CH4 during which PRBS testing occurs. This is the 3rd byte of the 32-bit window. PRBSWINDOW4[23:16]	0x80

TABLE 82. PRBSWINDOW4: CH4 PRBS WINDOW BYTE 3 . . . . . READ-WRITE, ADDR = 0x06F

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PRBSWINDOW4_3	PRBS window for CH4 during which PRBS testing occurs. This is the MSB of the 32-bit window. PRBSWINDOW4[31:24]	0x00

SDI EQ/CDR Control

TABLE 83. SDI_PD: SDI POWER-DOWN ..... READ-WRITE, ADDR = 0x080(CH1)/0x086(CH2)/0x090(CH3)/0x096(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
5	RSTN_CDR	Reset CDR. This bit is HI by default and must be set HI for normal operation. 0: Reset CDR 1: Normal operation	1
4	RSTN_PLL_DIRAC	Reset PLL-DIRAC. This bit is HI by default and must be set LO for Dirac operation. 0: Normal Dirac operation 1: Reset Dirac PLL	1
3	PD_CHANNEL	Power-down channel 0: Normal operation 1: Power-down	0
2	PD_EQ	Power-down EQ 0: Normal operation 1: Power-down	0
1	PD_CDR	Power-down CDR 0: Normal operation 1: Power-down	0
0	PD_PLL_DIRAC	Power-down PLL-DIRAC 0: Normal operation 1: Power-down	0

TABLE 84. RESERVED:. .....READ-WRITE, ADDR = 0x081(CH1)/0x087(CH2)/0x091(CH3)/0x097(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x03

TABLE 85. RESERVED: ..... READ-WRITE, ADDR = 0x082(CH1)/0x088(CH2)/0x092(CH3)/0x098(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x01

TABLE 86. RESERVED: ..... READ-WRITE, ADDR = 0x083(CH1)/0x089(CH2)/0x093(CH3)/0x099(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x0A

TABLE 87. RESERVED: ..... READ-WRITE, ADDR = 0x084(CH1)/0x08A(CH2)/0x094(CH3)/0x09A(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 88. RESERVED: ..... READ-WRITE, ADDR = 0x085(CH1)/0x08B(CH2)/0x095(CH3)/0x09B(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 89. CDR_PI_CTRL1: CH1 CDR PI CONTROL ..... READ-WRITE, ADDR = 0x0A0

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0xB3

TABLE 90. CDR_PI_CTRL2: CH2 CDR PI CONTROL . . . . . READ-WRITE, ADDR = 0x0A1

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0xB3

TABLE 91. CDR_PI_CTRL3: CH3 CDR PI CONTROL . . . . . READ-WRITE, ADDR = 0x0A2

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0xB3

TABLE 92. CDR_PI_CTRL4: CH4 CDR PI CONTROL . . . . . READ-WRITE, ADDR = 0x0A3

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0xB3

TABLE 93. PLL_CTRL: PLL CONTROL LSB. . . . . READ-WRITE, ADDR = 0x0A8

BIT	NAME	BIT DEFINITION	DEFAULT
7	PLL_TEST_BUF_EN	PLL Test buffer 0: Disable 1: Enable	0
6:5	Reserved	Reserved	00
4	PLL_PD	PLL Power-down 0: Normal operation 1: Power-down	0
3:1	Reserved	Reserved	000
0	PLL_RESET	PLL Reset 0: No request 1: Reset	0

TABLE 94. PLL_CTRL: PLL CONTROL MSB . . . . . READ-WRITE, ADDR = 0x0A9

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x01

TABLE 95. BGP_CTRL: BAND GAP CONTROL LSB . . . . . READ-WRITE, ADDR = 0x0AA

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	BAND_GAP_CTRL	Keep this as default.	0x00

TABLE 96. BGP_CTRL: BAND GAP CONTROL MSB . . . . . READ-WRITE, ADDR = 0x0AB

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	0x00
1	ANALOG_TOP_PD	Power-down analog top 0: Normal operation 1: Power-down	0
0	BGP_PD	Power-down Band Gap 0: Normal operation 1: Power-down	0

Video Payload ID

TABLE 97. VPID1: CH1 VIDEO PAYLOAD ID BYTE 0 ..... READ-ONLY, ADDR = 0x0B0

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID1_0	Captured video payload ID for CH1. Only updated if packet does not have checksum error. This is the LSB of the 32-bit word. VPID1[7:0]	0x00

TABLE 98. VPID1: CH1 VIDEO PAYLOAD ID BYTE 1 ..... READ-ONLY, ADDR = 0x0B1

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID1_1	Captured video payload ID for CH1. Only updated if packet does not have checksum error. This is the 2nd byte of the 32-bit word. VPID1[15:8]	0x00

TABLE 99. VPID1: CH1 VIDEO PAYLOAD ID BYTE 2 ..... READ-ONLY, ADDR = 0x0B2

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID1_2	Captured video payload ID for CH1. Only updated if packet does not have checksum error. This is the 3rd byte of the 32-bit word. VPID1[23:16]	0x00

TABLE 100. VPID1: CH1 VIDEO PAYLOAD ID BYTE 3 ..... READ-ONLY, ADDR = 0x0B3

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID1_3	Captured video payload ID for CH1. Only updated if packet does not have checksum error. This is the MSB of the 32-bit word. VPID1[31:24]	0x00

TABLE 101. VPID2: CH2 VIDEO PAYLOAD ID BYTE 0 ..... READ-ONLY, ADDR = 0x0B4

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID2_0	Captured video payload ID for CH2. Only updated if packet does not have checksum error. This is the LSB of the 32-bit word. VPID2[7:0]	0x00

TABLE 102. VPID2: CH2 VIDEO PAYLOAD ID BYTE 1 ..... READ-ONLY, ADDR = 0x0B5

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID2_1	Captured video payload ID for CH2. Only updated if packet does not have checksum error. This is the 2nd byte of the 32-bit word. VPID2[15:8]	0x00

TABLE 103. VPID2: CH2 VIDEO PAYLOAD ID BYTE 2 ..... READ-ONLY, ADDR = 0x0B6

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID2_2	Captured video payload ID for CH2. Only updated if packet does not have checksum error. This is the 3rd byte of the 32-bit word. VPID2[23:16]	0x00

TABLE 104. VPID2: CH2 VIDEO PAYLOAD ID BYTE 3 ..... READ-ONLY, ADDR = 0x0B7

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID2_3	Captured video payload ID for CH2. Only updated if packet does not have checksum error. This is the MSB of the 32-bit word. VPID2[31:24]	0x00

TABLE 105. VPID3: CH3 VIDEO PAYLOAD ID BYTE 0 ..... READ-ONLY, ADDR = 0x0B8

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID3_0	Captured video payload ID for CH3. Only updated if packet does not have checksum error. This is the LSB of the 32-bit word. VPID3[7:0]	0x00

TABLE 106. VPID3: CH3 VIDEO PAYLOAD ID BYTE 1 . . . . . READ-ONLY, ADDR = 0x0B9

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID3_1	Captured video payload ID for CH3. Only updated if packet does not have checksum error. This is the 2nd byte of the 32-bit word. VPID3[15:8]	0x00

TABLE 107. VPID3: CH3 VIDEO PAYLOAD ID BYTE 2 . . . . . READ-ONLY, ADDR = 0x0BA

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID3_2	Captured video payload ID for CH3. Only updated if packet does not have checksum error. This is the 3rd byte of the 32-bit word. VPID3[23:16]	0x00

TABLE 108. VPID3: CH3 VIDEO PAYLOAD ID BYTE 3 . . . . . READ-ONLY, ADDR = 0x0BB

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID3_3	Captured video payload ID for CH3. Only updated if packet does not have checksum error. This is the MSB of the 32-bit word. VPID3[31:24]	0x00

TABLE 109. VPID4: CH4 VIDEO PAYLOAD ID BYTE 0 . . . . . READ-ONLY, ADDR = 0x0BC

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID4_0	Captured video payload ID for CH4. Only updated if packet does not have checksum error. This is the LSB of the 32-bit word. VPID4[7:0]	0x00

TABLE 110. VPID4: CH4 VIDEO PAYLOAD ID BYTE 1 . . . . . READ-ONLY, ADDR = 0x0BD

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID4_1	Captured video payload ID for CH4. Only updated if packet does not have checksum error. This is the 2nd byte of the 32-bit word. VPID4[15:8]	0x00

TABLE 111. VPID4: CH4 VIDEO PAYLOAD ID BYTE 2 . . . . . READ-ONLY, ADDR = 0x0BE

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID4_2	Captured video payload ID for CH4. Only updated if packet does not have checksum error. This is the 3rd byte of the 32-bit word. VPID4[23:16]	0x00

TABLE 112. VPID4: CH4 VIDEO PAYLOAD ID BYTE 3 . . . . . READ-ONLY, ADDR = 0x0BF

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VPID4_3	Captured video payload ID for CH4. Only updated if packet does not have checksum error. This is the MSB of the 32-bit word. VPID4[31:24]	0x00

TABLE 113. RESERVED . . . . . READ-WRITE, ADDR = 0x0C0

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 114. RESERVED . . . . . READ-WRITE, ADDR = 0x0C1

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 115. RESERVED . . . . . READ-WRITE, ADDR = 0x0C2

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 116. RESERVED . . . . . READ-WRITE, ADDR = 0x0C3

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 117. RESERVED . . . . . READ-WRITE, ADDR = 0x0C4

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 118. RESERVED . . . . . READ-WRITE, ADDR = 0x0C5

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 119. RESERVED . . . . . READ-WRITE, ADDR = 0x0C6

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 120. RESERVED . . . . . READ-WRITE, ADDR = 0x0C7

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 121. RESERVED . . . . . READ-WRITE, ADDR = 0x0C8

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 122. RESERVED . . . . . READ-WRITE, ADDR = 0x0C9

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 123. RESERVED . . . . . READ-WRITE, ADDR = 0x0CA

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 124. RESERVED . . . . . READ-WRITE, ADDR = 0x0CB

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 125. RESERVED ..... READ-WRITE, ADDR = 0x0CC

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 126. RESERVED ..... READ-WRITE, ADDR = 0x0CD

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 127. RESERVED ..... READ-WRITE, ADDR = 0x0CE

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 128. RESERVED ..... READ-WRITE, ADDR = 0x0CF

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 129. RESERVED ..... READ-WRITE, ADDR = 0x0D0

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 130. RESERVED ..... READ-WRITE, ADDR = 0x0D1

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 131. RESERVED ..... READ-WRITE, ADDR = 0x0D2

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 132. RESERVED ..... READ-WRITE, ADDR = 0x0D3

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x80

TABLE 133. AUDIO_SRST: AUDIO SOFT RESET ..... READ-WRITE, ADDR = 0x0F6

BIT	NAME	BIT DEFINITION	DEFAULT
7	AUDIO_SRST	Reset whole audio top 0: No request 1: Reset	0
3:0	Reserved	Reserved	0x0

TABLE 134. AUDIO_MISC_CTRL: AUDIO MISC CONTROL . . . . . READ-WRITE, ADDR = 0x0F7

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0xF
3:0	AMUX_CH_SEL	Audio channel select in Audio MUX system. BIT[n] controls CH(n+1), (n = 0~3). When 8-bit/16-bit: 0: Left channel 1: Right channel When 24-bit: 0: Right channel 1: Stereo (Table 141)	0x0

Device Information

TABLE 135. DEVREV: DEVICE REVISION . . . . . READ-ONLY, ADDR = 0x0FE

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	DEVREV	Device revision number.	0xB1

TABLE 136. DEVID: DEVICE ID . . . . . READ-ONLY, ADDR = 0x0FF

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	DEVID	Device ID.	0x74

Analog Audio Processor/Digital Serial Audio Configuration

TABLE 137. AUDIO GAIN SETTINGS

SETTING: GAIN	SETTING: GAIN
0: 0.25	8: 1.00
1: 0.31	9: 1.25
2: 0.38	10: 1.50
3: 0.44	11: 1.75
4: 0.50	12: 2.00
5: 063	13: 2.25
6: 0.75	14: 2.50
7: 0.88	15: 2.75

TABLE 138. AIGAIN: AUDIO GAIN LSB. . . . . READ-WRITE, ADDR = 0x100

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	AIGAIN2	Audio gain for AIN2. See Table 137 for gain settings.	0x8
3:0	AIGAIN1	Audio gain for AIN1. See Table 137 for gain settings.	0x8

TABLE 139. AIGAIN: AUDIO GAIN MSB . . . . . READ-WRITE, ADDR = 0x101

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	AIGAIN4	Audio gain for AIN4. See Table 137 for gain settings.	0x8
3:0	AIGAIN3	Audio gain for AIN3. See Table 137 for gain settings.	0x8

TABLE 140. RM_CTRL: RECORD AND MIX CONTROL . . . . . READ-WRITE, ADDR = 0x102

BIT	NAME	BIT DEFINITION	DEFAULT
7	M_RLSWAP	Defines the sequence of mixing and playback audio on the DATM pin. If RM_SYNC = 0 (I2S format): 0: Mixing audio in position 0; playback audio in position 8 1: Playback audio in position 0; mixing audio in position 8 If RM_SYNC = 1 (DSP format): 0: Mixing audio in position 0; playback audio in position 1 1: Playback audio in position 0; mixing audio in position 1	0
6	RM_SYNC	Defines the serial data format for record and mixing audio on the ACLKR/ASYNR/ADATR/ADATM pins. 0: I2S format 1: DSP format	0
5:4	RM_PBSEL	Selects the output data for the ADATM pin 0: 1st stage 1: 2nd stage 2: 3rd stage 3: 4th stage	00
3:2	R_ADATM	Selects the output mode for the ADATM pin 0: Digital serial data of mixing audio 1: Digital serial data of ADATR format record audio 2: Digital serial data of ADATM format record audio 3: Not defined	00
1:0	R_MULTCH	Define the number of channels for record on the ADATR pin When 8-bit/16-bit: 0: 2 channels 1: 4 channels 2: 8 channels 3: 16 channels When 24-bit: 0: 1 channel R and L 1: 2 channels R and L 2: 4 channels R and L 3: N/A The number of channels is limited as shown in the Sequence of Multichannel Audio Record table on page 23. Each output position is selected by the R_SEQ0/R_SEQ1/.../R_SEQF registers.	00

TABLE 141. ADATR DATA SELECTION

I2S BITS = 0, 1		I2S BITS = 2
SETTING: SELECTION (via R_SEQ0~R_SEQF)		SETTING: SELECTION (via R_SEQ0~R_SEQ7)
0: AIN1 or SDI1_L	8: AIN9	0: SDI1_L
1: AIN2 or SDI2_L	9: AIN10	1: SDI2_L
2: AIN3 or SDI3_L	10: AIN11	2: SDI3_L
3: AIN4 or SDI4_L	11: AIN12	3: SDI4_L
4: AIN5	12: AIN13	4: SDI1_R
5: AIN6	13: AIN14	5: SDI2_R
6: AIN7	14: AIN15	6: SDI3_R
7: AIN8	15: AIN16	7: SDI4_R

TABLE 142. R_SEQ: ADATR RECORD SEQUENCE BYTE 0 . . . . . READ-WRITE, ADDR = 0x103

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQ1	Record sequence on ADATR. See Table 141 for data choices.	0x1
3:0	R_SEQ0	Record sequence on ADATR. See Table 141 for data choices.	0x0

TABLE 143. R_SEQ: ADATR RECORD SEQUENCE BYTE 1 . . . . . READ-WRITE, ADDR = 0x104

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQ3	Record sequence on ADATR. See Table 141 for data choices.	0x3
3:0	R_SEQ2	Record sequence on ADATR. See Table 141 for data choices.	0x2

TABLE 144. R_SEQ: ADATR RECORD SEQUENCE BYTE 2 . . . . . READ-WRITE, ADDR = 0x105

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQ5	Record sequence on ADATR. See Table 141 for data choices.	0x5
3:0	R_SEQ4	Record sequence on ADATR. See Table 141 for data choices.	0x4

TABLE 145. R_SEQ: ADATR RECORD SEQUENCE BYTE 3 . . . . . READ-WRITE, ADDR = 0x106

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQ7	Record sequence on ADATR. See Table 141 for data choices.	0x7
3:0	R_SEQ6	Record sequence on ADATR. See Table 141 for data choices.	0x6

TABLE 146. R_SEQ: ADATR RECORD SEQUENCE BYTE 4 . . . . . READ-WRITE, ADDR = 0x107

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQ9	Record sequence on ADATR. See Table 141 for data choices.	0x9
3:0	R_SEQ8	Record sequence on ADATR. See Table 141 for data choices.	0x8

TABLE 147. R_SEQ: ADATR RECORD SEQUENCE BYTE 5 . . . . . READ-WRITE, ADDR = 0x108

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQB	Record sequence on ADATR. See Table 141 for data choices.	0xB
3:0	R_SEQA	Record sequence on ADATR. See Table 141 for data choices.	0xA

TABLE 148. R_SEQ: ADATR RECORD SEQUENCE BYTE 6 . . . . . READ-WRITE, ADDR = 0x109

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQD	Record sequence on ADATR. See Table 141 for data choices.	0xD
3:0	R_SEQC	Record sequence on ADATR. See Table 141 for data choices.	0xC

TABLE 149. R_SEQ: ADATR RECORD SEQUENCE BYTE 7 . . . . . READ-WRITE, ADDR = 0x10A

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	R_SEQF	Record sequence on ADATR. See Table 141 for data choices.	0xF
3:0	R_SEQE	Record sequence on ADATR. See Table 141 for data choices.	0xE

TABLE 150. MASTER: AUDIO MASTER CONTROL. . . . . READ-WRITE, ADDR = 0x10B

BIT	NAME	BIT DEFINITION	DEFAULT
7	ADAC_EN	Enable DAC 0: Disable 1: Enable	1
6	AADC_EN	Enable ADC 0: Disable 1: Enable	1
5	PB_MASTER	Playback master mode 0: Slave mode (ACLKP/ASYNP are inputs) 1: Master mode (ACLKP/ASYNCP are outputs)	0
4	PB_LRSEL	Select audio channel to be used for playback If PB_SYNC == 0 (I2S format): 0: First left channel 1: First right channel If PB_SYNC == 1 (DSP format): 0: First input 1: Second input	0
3	PB_SYNC	Defines the serial data format for playback audio on the ACLKP/SYNP/ADATP pins. 0: I2S format 1: DSP format	0
2	Reserved	Reserved	0
1	ASYNROEN	ASYNR output mode 0: Output 1: Input	1
0	ACLKRMASTER	ACLKR master/slave mode 0: Slave (input) 1: Master (output)	1

TABLE 151. AFMT: AUDIO OUTPUT FORMAT . . . . . READ-WRITE, ADDR = 0x10C

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	AFMT	Select u-Law/A-Law/PCM/SB output format on ADATR/ADATM pins 0: PCM 1: Signed Bit; if MSB is 1 then PCM data is inverted 2: u-Law 3: A-Law	00
5	MIX_DERATIO	Disable the individual mix ratio for each audio 0: Apply the individual mixing ratio for each audio channel. Each channel applies its mixer gain per MIX_RATIO1/MIX_RATIO2/MIX_RATIO3/ MIX_RATIO4/MIX_RATIO5. 1: Apply MIX_RATIO1 to all channels.	0
4	MIX_MUTEPB	ADATP mute 0: Normal 1: Muted	1
3	MIX_MUTE4	AIN4 mute 0: Normal 1: Muted	0
2	MIX_MUTE3	AIN3 mute 0: Normal 1: Muted	0
1	MIX_MUTE2	AIN2 mute 0: Normal 1: Muted	0
0	MIX_MUTE1	AIN1 mute 0: Normal 1: Muted	0

TABLE 152. MIXRATIO: MIX RATIO BYTE 0 . . . . . READ-WRITE, ADDR = 0x10D

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	MIX_RATIO2	AIN2 mix ratio per MIXRATIOMD. This ratio will not be used if MIX_DERATIO = 1.	0x0
3:0	MIX_RATIO1	AIN1 mix ratio per MIXRATIOMD.	0x0

TABLE 153. MIXRATIO: MIX RATIO BYTE 1 . . . . . READ-WRITE, ADDR = 0x10E

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	MIX_RATIO4	AIN4 mix ratio per MIXRATIOMD. This ratio will not be used if MIX_DERATIO = 1.	0x0
3:0	MIX_RATIO3	AIN3 mix ratio per MIXRATIOMD. This ratio will not be used if MIX_DERATIO = 1.	0x0

TABLE 154. OUTPUT VOLTAGE SWING OR GAIN SETTINGS

SETTING: GAIN/SWING	SETTING: GAIN/SWING
0: -22.5dB/0.11V_{P-P}	8: -10.5dB/0.42V_{P-P}
1: -21.0dB/0.13V_{P-P}	9: -9.0dB/0.50V_{P-P}
2: -19.5dB/0.15V_{P-P}	Ah: -7.5dB/0.59V_{P-P}
3: -18.0dB/0.18V_{P-P}	Bh: -6.0dB/0.70V_{P-P}
4: -16.5dB/0.21V_{P-P}	Ch: -4.5dB/0.83V_{P-P}
5: -15.0dB/0.25V_{P-P}	Dh: -3.0dB/0.98V_{P-P}
6: -13.5dB/0.29V_{P-P}	Eh: -1.5dB/1.17V_{P-P}
7: -12.0dB/0.35V_{P-P}	Fh: 0dB/1.40V_{P-P}

TABLE 155. MIXRATIO: MIX RATIO BYTE 2 . . . . . READ-WRITE, ADDR = 0x10F

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x8
3:0	MIXRATIOPB	ADATP mix ratio. See Table 180 for mix ratio settings.	0x0

TABLE 156. MIXCONTROL: MIX OUTPUT CONTROL . . . . . READ-WRITE, ADDR = 0x110

BIT	NAME	BIT DEFINITION	DEFAULT
7	Reserved	Reserved	0
6	ADCCLKPOL	ADC clock polarity 0: Normal 1: Inverted	0
5	DACCLKPOL	DAC clock polarity 0: Normal 1: Inverted	0
4:0	OUTSEL	Select audio output 0: Select record audio of channel 1 1: Select record audio of channel 2 2: Select record audio of channel 3 3: Select record audio of channel 4 4: Select record audio of channel 5 5: Select record audio of channel 6 6: Select record audio of channel 7 7: Select record audio of channel 8 8: Select record audio of channel 9 9: Select record audio of channel 10 Ah: Select record audio of channel 11 Bh: Select record audio of channel 12 Ch: Select record audio of channel 13 Dh: Select record audio of channel 14 Eh: Select record audio of channel 15 Fh: Select record audio of channel 16 10h: Select ADATP of the first stage device 11h: Select ADATP of the second stage device 12h: Select ADATP of the third stage device 13h: Select ADATP of the last stage device 14h: Select mixed audio 15h: Select record audio of AIN51 16h: Select record audio of AIN52 17h: Select record audio of AIN53 18h: Select record audio of AIN54	0x1F

TABLE 157. RESERVED . . . . . READ-WRITE, ADDR = 0x111

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0xF0

TABLE 158. RESERVED . . . . . READ-WRITE, ADDR = 0x112

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x33

TABLE 159. RESERVED . . . . . READ-WRITE, ADDR = 0x113

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x33

TABLE 160. ACKI: AUDIO CLOCK INCREMENT BYTE 0. . . . . READ-WRITE, ADDR = 0x114

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ACKI0	ACKI clock increment in ACKG block. ACKI[7:0]	0x23

TABLE 161. ACKI: AUDIO CLOCK INCREMENT BYTE 1. . . . . READ-WRITE, ADDR = 0x115

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ACKI1	ACKI clock increment in ACKG block. ACKI[15:8]	0x48

TABLE 162. ACKI: AUDIO CLOCK INCREMENT BYTE 2. . . . . READ-WRITE, ADDR = 0x116

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
5:0	ACKI2	ACKI clock increment in ACKG block. ACKI[21:16]	0x07

TABLE 163. ACKN: AUDIO CLOCK NUMBER BYTE 0 . . . . . READ-WRITE, ADDR = 0x117

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ACKN0	ACKN clock number. ACKN[7:0]	0x00

TABLE 164. ACKN: AUDIO CLOCK NUMBER BYTE 1 . . . . . READ-WRITE, ADDR = 0x118

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ACKN1	ACKN clock number. ACKN[15:8]	0x01

TABLE 165. ACKN: AUDIO CLOCK NUMBER BYTE 2 . . . . . READ-WRITE, ADDR = 0x119

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	0x00
2:0	ACKN2	ACKN clock number. ACKN[18:16]	000

TABLE 166. SDIV: SERIAL CLOCK DIVIDER. . . . . READ-WRITE, ADDR = 0x11A

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
5:0	SDIV	Serial clock divider in ACKG block.	0x00

TABLE 167. LRDIV: LEFT/RIGHT CLOCK DIVIDER. . . . . READ-WRITE, ADDR = 0x11B

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
5:0	LRDIV	Left/Right clock divider in ACKG block.	0x20

TABLE 168. ACCTRL: AUDIO CLOCK CONTROL 0 . . . . . READ-WRITE, ADDR = 0x11C

BIT	NAME	BIT DEFINITION	DEFAULT
7	APZ	Loop control in ACKG block.	1
6:4	APG	Loop control in ACKG block.	100
3	Reserved	Reserved	0
2	ACPL	Open/closed loop in ACKG block 0: Closed 1: Open (recommend for most applications)	1

TABLE 168. ACCTRL: AUDIO CLOCK CONTROL 0 . . . . . READ-WRITE, ADDR = 0x11C (Continued)

BIT	NAME	BIT DEFINITION	DEFAULT
1	SRPH	Audio master clock phase select. 0: Invert master clock 1: Normal master clock	0
0	LRPH	Playback clock phase select. 0: Invert master clock 1: Normal master clock	0

TABLE 169. ADTCT: AUDIO DETECT . . . . . READ-WRITE, ADDR = 0x11D

BIT	NAME	BIT DEFINITION	DEFAULT
7	PBREFEN	Loop control in ACKG block.	0
6:5	ADET_MODE	Loop control in ACKG block.	11
4	ACK36MD	Set this bit to 0 for proper operation.	1
3:0	Reserved	Reserved	0xF

TABLE 170. ACTRL: AUDIO CONTROL . . . . . READ-WRITE, ADDR = 0x11E

BIT	NAME	BIT DEFINITION	DEFAULT
7	AAUTO_MUTE	Audio auto mute 0: No effect 1: When input analog data is less than the ADET_H level, output PCM data will be 0x0000 (0x00). Audio DAC data input is 0x200.	0
6	Reserved	Reserved	0
5	A_DAC_PWDN	Audio DAC power-down 0: Normal operation 1: Power-down	0
4	A_ADC_PWDN	Audio ADC power-down 0: Normal operation 1: Power-down	0
3:0	Reserved	Reserved	0x0

TABLE 171. SERIALCTRL: SERIAL MODE CONTROL. . . . . READ-WRITE, ADDR = 0x11F

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	FIRSTCNUM	First stage device number in the cascade. Set to 3 if 4 devices are cascaded.	0x0
3:2	Reserved	Reserved	00
1	ALINK_CASCADE_EN	Audio cascade mode 0: ALINKI data is 0, ALINKO is tri-state 1: ALINKO is serial output, ALINKI is serial input	0
0	Reserved	Reserved. Always set to 0.	0

TABLE 172. ADACCTRL: AUDIO DAC CONTROL . . . . . READ-WRITE, ADDR = 0x121

BIT	NAME	BIT DEFINITION	DEFAULT
7	DAC_REF	DAC reference voltage source 0: Use VDD/R 1: Use VDD/R and LPF. This rejects more power supply noise.	0
6	DAC_CLK_INVb	DAC clock invert (clock is referenced to the incoming clock) 0: Incoming DAC data is latched by a buffered clock 1: Normal operation. The incoming DAC data is latched by an inverted clock.	0
5	DAC_CMN_REF	DAC common mode voltage reference source 0: Use VDD/R 1: Use VDD/R and LPF. This rejects more power supply noise.	0
4	DAC_TESTEN	Test output driver disable 0: Output driver enabled 1: Output driver disabled	0
3:0	DAC_GAIN	DAC gain. See Table 154 for gain settings.	0x0

TABLE 173. AADCCTRL: AUDIO ADC CONTROL . . . . . READ-WRITE, ADDR = 0x122

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Unused	Unused	0x0
3:2	ADC_CTRL1	Bias current control for channel 4 and 5. Channels 1, 2, 3 are designed with fixed bias current. 0: 20µA 1: 20µA 2: 40µA 3: 59µA	00
1:0	ADC_CTRL2	Bias control for the ADC 0: 10µA 1: 15µA 2: 20µA 3: 25µA	00

TABLE 174. AADCRST: AUDIO ADC RESET . . . . . READ-WRITE, ADDR = 0x124

BIT	NAME	BIT DEFINITION	DEFAULT
7	ADC_MASK	Controls loop in ACKG block	0
6	ARST	Audio soft reset 0: Normal operation 1: Reset audio core	0
5:0	Reserved	Reserved	0x07

TABLE 175. AADCOFFSET: AUDIO ADC OFFSET . . . . . READ-WRITE, ADDR = 0x125

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	ADC4OFFH	Upper two bits of the ADC4 offset register	00
5:4	ADC3OFFH	Upper two bits of the ADC3 offset register	00
3:2	ADC2OFFH	Upper two bits of the ADC2 offset register	00
1:0	ADC1OFFH	Upper two bits of the ADC1 offset register	00

TABLE 176. AADCOFFSET1: AUDIO ADC1 OFFSET. . . . . READ-WRITE, ADDR = 0x126

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADC1OFFL	Lower byte of the ADC1 offset register	0x00

TABLE 177. AADCOFFSET2: AUDIO ADC2 OFFSET . . . . . READ-WRITE, ADDR = 0x127

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADC2OFFL	Lower byte of the ADC2 offset register	0x00

TABLE 178. AADCOFFSET3: AUDIO ADC3 OFFSET. . . . . READ-WRITE, ADDR = 0x128

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADC3OFFL	Lower byte of the ADC3 offset register	0x00

TABLE 179. AADCOFFSET4: AUDIO ADC4 OFFSET. . . . . READ-WRITE, ADDR = 0x129

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADC4OFFL	Lower byte of the ADC4 offset register	0x00

TABLE 180. MIX RATIO SETTINGS IF MIXRATIOMD = 0

MIX_RATIOn: MIX RATIO	MIX_RATIOn: MIX RATIO
0: 0.25	8: 1.00
1: 0.31	9: 1.25
2: 0.38	10: 1.50
3: 0.44	11: 1.75
4: 0.50	12: 2.00
5: 063	13: 2.25
6: 0.75	14: 2.50
7: 0.88	15: 2.75

TABLE 181. AUDIO OUTPUT GAIN SETTINGS IF DAORATIO = 0

DAOGAIN: GAIN	DAOGAIN: GAIN
0: 0.25	8: 1.00
1: 0.31	9: 1.25
2: 0.38	10: 1.50
3: 0.44	11: 1.75
4: 0.50	12: 2.00
5: 063	13: 2.25
6: 0.75	14: 2.50
7: 0.88	15: 2.75

TABLE 182. MIXRATIO: MIX RATIO VALUE. . . . . READ-WRITE, ADDR = 0x12A

BIT	NAME	BIT DEFINITION	DEFAULT
7	MIXRATIOMD	Mix ratio divider control 0: Apply the mix ratio defined by Table 180 1: Use MIX_RATIOn/64	0
6	Reserved	Reserved	0
5	Reserved	Reserved	1
4	DAORATIO	Digital audio output gain control 0: Apply the gain defined by Table 181 1: Use DAOGAIN/64	0
3:0	DAOGAIN	Digital audio output gain per DAORATIO	0x8

TABLE 183. OUTEN: OUTPUT ENABLE BYTE 0 . . . . . READ-WRITE, ADDR = 0x12C

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	Reserved	Reserved	0x00
0	ADATMEN	Enable ADATM output. ADATM outputs through the MPP0 pin. 0: Tri-state 1: Output enable	0

TABLE 184. OUTEN: OUTPUT ENABLE BYTE 1 . . . . . READ-WRITE, ADDR = 0x12D

BIT	NAME	BIT DEFINITION	DEFAULT
7	ALINKOEN	Enable ALINKO output. 0: Output enable based on ALINK_CASCADE_EN 1: Output enable	0
6:0	Reserved	Reserved	0x00

TABLE 185. AUDPTRN: AUDIO TEST PATTERN . . . . . READ-WRITE, ADDR = 0x12E

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	AUDTST4	Audio sine wave test pattern for CH4 00: 0.5kHz 01: 1kHz 10: 2kHz 11: 3kHz	00
5:4	AUDTST3	Audio sine wave test pattern for CH3 00: 0.5kHz 01: 1kHz 10: 2kHz 11: 3kHz	00
3:2	AUDTST2	Audio sine wave test pattern for CH2 00: 0.5kHz 01: 1kHz 10: 2kHz 11: 3kHz	00
1:0	AUDTST1	Audio sine wave test pattern for CH1 00: 0.5kHz 01: 1kHz 10: 2kHz 11: 3kHz	00

TABLE 186. AUDSRCSEL: AUDIO SOURCE SELECT . . . . . READ-WRITE, ADDR = 0x12F

BIT	NAME	BIT DEFINITION	DEFAULT
7	AMPDIV2	Audio sine wave test pattern amplitude divide by 2 0: Do not divide 1: Divide	0
6	AUDSEL5	Audio data select for CH5 0: From ADC 1: From AUDTST5 test pattern	0
5	AUDSEL4	Audio data select for CH4 0: From ADC 1: From AUDTST4 test pattern	0
4	AUDSEL3	Audio data select for CH3 0: From ADC 1: From AUDTST3 test pattern	0
3	AUDSEL2	Audio data select for CH2 0: From ADC 1: From AUDTST2 test pattern	0
2	AUDSEL1	Audio data select for CH5 0: From ADC 1: From AUDTST1 test pattern	0
1:0	AUDTST5	Audio sine wave test pattern for CH5 00: 0.5kHz 01: 1kHz 10: 2kHz 11: 3kHz	00

TABLE 187. AUDCLKCON2: AUDIO CLOCK CONTROL 1 . . . . . READ-WRITE, ADDR = 0x130

BIT	NAME	BIT DEFINITION	DEFAULT
7	I2S_24BIT	ACLKP/ASYNP/ADATP bit width 0: Select per I2S_8BIT 1: Select 24-bit	0
6	I2S_8BIT	ACLKP/ASYNP/ADATP bit width (valid if I2S_24BIT == 0) 0: Input is 16-bit 1: Input is 8-bit	0
5	ACLKRPOL	ACLKR input/output polarity invert 0: Not inverted 1: Inverted	0
4	ACLKPPOL	ACLKP input polarity invert 0: Not inverted 1: Inverted	0
3	AFAUTO	Select auto or manual (ACKI) setup. 0: Manual configuration of ACKI 1: Auto setup of ACKI per AFMD. Effective only if ACLKRMASTER == 1.	1
2:0	AFMD	AFAUTO sampling frequency selection 0: 8kHz 1: 16kHz 2: 32kHz 3: 44.1kHz 4: 48kHz Others: Not used	000

TABLE 188. AUDINCTRL: AUDIO INPUT CONTROL . . . . . READ-WRITE, ADDR = 0x131

BIT	NAME	BIT DEFINITION	DEFAULT
7	I2S8MODE	8-bit I2S record output mode 0: L/R half length separated output 1: One continuous packed output equal to DSP output format	0
6	MASCKMD	Audio clock master ACLKR duty cycle 0: High period is one 36MHz clock period 1: Almost 50% duty cycle. If 1, then ACKI needs to be doubled. Normally used with SDIV = 0.	1
5	PBINSWAP	Playback ADATP input data MSB-LSB swap 0: Not swapped 1: Swapped	0
4	ASYNRDLY	ASYNR input delay 0: No delay 1: Add one 27MHz period delay to ASYNR input	0
3	ASYNPDLY	ASYNP input delay 0: No delay 1: Add one 36MHz period delay to ASYNP input	0
2	ADATPDLY	ADATP input delay 0: No delay 1: Add one 36MHz period delay to ADATP input	0
1:0	INLAWMD	Select u-Law/A-Law/PCM/SB data input format on ADATP pin 0: PCM format 1: Signed Bit; if MSB is 1 then PCM data is inverted 2: u-Law 3: A-Law	00

TABLE 189. AUDCLKCTRL: AUDIO CLOCK CONTROL 2 . . . . . READ-WRITE, ADDR = 0x133

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	0x00
2	AIN51FORM	AIN51/52/53/54 record output format selection. This bit is only effective when A51OUTOFF == 0. When AIN1/2/3/4/51 and AIN6/7/8/9/52 are required to be continuous in the record output, set this bit to 1. 0: If I2S mode (RM_SYNC == 0): L data: <dat0><dat1><dat2><dat3><dat4> <dat5><dat6><dat7><dat51><dat52> R data: <dat8><dat9><datA><datB><datC> <datD><datE><datF><dat53><dat54> If DSP mode (RM_SYNC == 1), all data are continuous: <dat0><dat1><dat2><dat3><dat4> <dat5><dat6><dat7><dat8><dat9> <datA><datB><datC><datD><datE> <datF><dat51><dat52><dat53><dat54> 1: If I2S mode (RM_SYNC == 0): L data: <dat0><dat1><dat2><dat3><dat51> <dat4><dat5><dat6><dat7><dat52> R data: <dat8><dat9><datA><datB><dat53> <datC><datD><datE><datF><dat54> If DSP mode (RM_SYNC == 1), all data are continuous: <dat0><dat1><dat2><dat3><dat51> <dat4><dat5><dat6><dat7><dat52> <dat8><dat9><datA><datB><dat53> <datC><datD><datE><datF><dat54>	0
1	Reserved	Reserved	0
0	Reserved	Reserved	1

TABLE 190. AUDFXCTRL: AUDIO SAMPLING MODE CONTROL . . . . . READ-WRITE, ADDR = 0x134

BIT	NAME	BIT DEFINITION	DEFAULT
7	Reserved	Reserved	0
6	ASYNSERIAL	ALINKO/AINKI bit rate 0: 27MHz. Effective for all sampling frequencies. 1: 13.5MHz. Effective for 8/16kSps modes.	0
5	ACLKR128	ACLKR clock output mode for special 16x8-bit (128-bit total) data interface 0: ACLKR output is normal 1: 128 ACLKR clocks per sample. Effective when I2S_8BIT == 1 (special purpose 8-bit mode).	0
4	ACLKR64	ACLKR clock output mode for special 4-word output interface. Effective for ACLKRMASTER == 1 only. 0: ACLKR is normal 1: 64 ACLKR clocks per sample	0
3	AFS384	Special audio sampling mode. ACLKR runs at: 0: Normal sampling mode. If AIN5MD == 0: 256*f_S 1: 384*f_S	0
2	AIN5MD	Audio input process mode 0: Four channel (AIN1/AIN2/AIN3/AIN4) audio input processing only. If AFS384 == 0: 256*f_S. In this mode, AIN5 is not processed. 1: Five channel (AIN1/AIN2/AIN3/AIN4/AIN5) audio input processing. If AFS384 == 0: 320*f_S.	0
1:0	I2SBITS	Define output data format per one word unit on ADATR/ADATM pin 0: 16-bit one word unit output 1: 8-bit one word unit packed output 2: 24-bit one word unit packed output - applies to SDI audio only 3: Not defined	00

TABLE 191. ANC_AUD: ANCILLARY AUDIO . . . . . READ-WRITE, ADDR = 0x135

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3	ANC_AUD4	Select ancillary or analog audio for CH4 0: Analog audio 1: Truncated 16-bit ancillary audio	0
2	ANC_AUD3	Select ancillary or analog audio for CH3 0: Analog audio 1: Truncated 16-bit ancillary audio	0
1	ANC_AUD2	Select ancillary or analog audio for CH2 0: Analog audio 1: Truncated 16-bit ancillary audio	0
0	ANC_AUD1	Select ancillary or analog audio for CH1 0: Analog audio 1: Truncated 16-bit ancillary audio	0

TABLE 192. PBSEL: PLAYBACK CHANNEL SELECT . . . . . READ-WRITE, ADDR = 0x136

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3:0	PBSEL	Select one of the 16 channels as playback data	0x0

TABLE 193. AADCOFFSET5: AUDIO ADC5 OFFSET LSB. . . . . READ-WRITE, ADDR = 0x138

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	Reserved	Reserved	0x00
1:0	ADC5OFFH	Upper two bits of the ADC5 offset register	00

TABLE 194. AADCOFFSET5: AUDIO ADC5 OFFSET MSB . . . . . READ-WRITE, ADDR = 0x139

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADC5OFFL	Lower byte of the ADC5 offset register	0x00

TABLE 195. ADATM DATA SELECTION

I2SBITS = 0, 1			I2SBITS = 2
SETTING: SELECTION	SETTING: SELECTION	SETTING: SELECTION	SETTING: SELECTION
0: AIN1 or SDI1_L 1: AIN2 or SDI2_L 2: AIN3 or SDI3_L 3: AIN4 or SDI4_L 4: AIN5 5: AIN6 6: AIN7 7: AIN8	8: AIN9 9: AIN10 10: AIN11 11: AIN12 12: AIN13 13: AIN14 14: AIN15 15: AIN16	16: PB1 17: PB2 18: PB3 19: PB4 20: MIX 21: AIN51 22: AIN52 23: AIN53 24: AIN54	0: SDI1_L 1: SDI2_L 2: SDI3_L 3: SDI4_L 4: SDI1_R 5: SDI2_R 6: SDI3_R 7: SDI4_R 8: PB1

TABLE 196. I2SO_RSEL: ADATM RIGHT CHANNEL SELECT . . . . . READ-WRITE, ADDR = 0x13B

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	Reserved	Reserved	000
4:0	I2SO_RSEL	ADATM right channel select. See Table 195 for data choices.	0x15

TABLE 197. I2SO_RSEL: ADATM LEFT CHANNEL SELECT . . . . . READ-WRITE, ADDR = 0x13C

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	Reserved	Reserved	000
4:0	I2SO_LSEL	ADATM left Channel select. See Table 195 for data choices.	0x15

TABLE 198. I2SRECSEL: AIN5 RECORD SELECT . . . . . READ-WRITE, ADDR = 0x13D

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	I2SRECSEL54	0: AIN51, 1: AIN52, 2: AIN53, 3: AIN54	11
5:4	I2SRECSEL53	0: AIN51, 1: AIN52, 2: AIN53, 3: AIN54	10
3:2	I2SRECSEL52	0: AIN51, 1: AIN52, 2: AIN53, 3: AIN54	01
1:0	I2SRECSEL51	0: AIN51, 1: AIN52, 2: AIN53, 3: AIN54	00

TABLE 199. AIN5CTRL: AIN5 CONTROL LSB . . . . . READ-WRITE, ADDR = 0x13E

BIT	NAME	BIT DEFINITION	DEFAULT
7	A5OUTOFF	AIN5 data output on ADATR 0: Output AIN51/AIND52/AIN53/AIN54 record data on ADATR 1: Do not output AIN51/AIND52/AIN53/AIN54 record data on ADATR	1
6	ADATM_I2SOEN	Define ADATM pin output two word data for standard I2S output 0: Mixing data or playback input data are only output on ADATM pin per M_RLSWAP 1: L/R data on ADATM pin is selected by I2SO_RSEL/I2SO_LSEL registers	0
5	AIN5MUTE	AIN5 mute control 0: Normal 1: Mute	1
4:0	Reserved	Reserved	0x03

TABLE 200. AIN5CTRL: AIN5 CONTROL MSB . . . . . READ-WRITE, ADDR = 0x13F

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	AIGAIN5	Audio gain for AIN5. See Table 137 for gain settings.	0x0
3:0	MIX_RATIO5	AIN5 mix ratio per MIXRATIOMD. This ratio will not be used if MIX_DERATIO = 1.	0x0

Interrupt Control

TABLE 201. IRQ_CTRL: IRQ CONTROL. . . . . READ-WRITE, ADDR = 0x300

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	0x00
2	IRQ_TRISTATE	IRQ pin tri-state 0: Enabled 1: Tri-stated	0
1	IRQ_POL	IRQ Polarity 0: High active 1: Low active	0
0	IRQ_EN	Enable interrupt requests through the IRQ pin 0: Disable 1: Enable	0

TABLE 202. RESERVED . . . . . READ-WRITE, ADDR = 0x302

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 203. ANCINTCTRL: ANCILLARY DATA INTERRUPT SOURCE CONTROL . . . . . READ-WRITE, ADDR = 0x305

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3	ANCINT4	Ancillary detection interrupt enable for CH4 0: Disable 1: Enable	0
2	ANCINT3	Ancillary detection interrupt enable for CH3 0: Disable 1: Enable	0
1	ANCINT2	Ancillary detection interrupt enable for CH2 0: Disable 1: Enable	0
0	ANCINT1	Ancillary detection interrupt enable for CH1 0: Disable 1: Enable	0

TABLE 204. I2S_AUDMUX_SEL: I2S AUDIO MUX SOURCE SELECT . . . . . READ-WRITE, ADDR = 0x310

BIT	NAME	BIT DEFINITION	DEFAULT
7	Reserved	Reserved	0
6	I2S_ACLK_POL	I2S output clock polarity reverse 0: Not reversed 1: Reversed	0
5	Reserved	Reserved	1
4:0	I2S_MUX_SEL	I2S MUX input source 01h: Analog audio source 02h: SDI CH1 audio source 04h: SDI CH2 audio source 08h: SDI CH3 audio source x0h: SDI CH4 audio source	0x00

TABLE 205. I2S_AUDOUT_SEL: I2S AUDIO OUT SOURCE SELECT . . . . . READ-WRITE, ADDR = 0x311

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3	I2S_OUT_SEL4	I2S Audio out Select for CH4 0: HD Audio 1: SD Audio	0
2	I2S_OUT_SEL3	I2S Audio out Select for CH3 0: HD Audio 1: SD Audio	0
1	I2S_OUT_SEL2	I2S Audio out Select for CH2 0: HD Audio 1: SD Audio	0
0	I2S_OUT_SEL1	I2S Audio out Select for CH1 0: HD Audio 1: SD Audio	0

Analog EQ Offset Compensation

TABLE 206. RESERVED: ..... READ-WRITE, ADDR = 0x380(CH1)/0x390(CH2)/0x3A0(CH3)/0x3B0(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 207. RESERVED:. ..... .READ-WRITE, ADDR = 0x381(CH1)/0x391(CH2)/0x3A1(CH3)/0x3B1(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 208. RESERVED: ..... READ-WRITE, ADDR = 0x382(CH1)/0x392(CH2)/0x3A2(CH3)/0x3B2(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	0x00

TABLE 209. AGC_CTRL: AUTOMATIC GAIN CONTROL LSB ..... READ-WRITE, ADDR = 0x383(CH1)/0x393(CH2)/0x3A3(CH3)/0x3B3(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	AGC_OVWR_EN	Enable using AGC_OVWR value as offset. The value derived from auto calibration process will be ignored when this bit is “1”. 0: Disable 1: Enable	0
6:0	AGC_OVWR	This value is used as offset value when Overwrite Mode is set. The value is 0 ~ 127.	0x00

TABLE 210. AGC_CTRL: AUTOMATIC GAIN CONTROL MSB..... READ-WRITE, ADDR = 0x384(CH1)/0x394(CH2)/0x3A4(CH3)/0x3B4(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	Reserved	Reserved	0x00
1	AGC_2X_RANGE	Use 2X calibration range (0 ~ 255) 0: Normal range (0 ~ 127) 1: 2X range (0 ~ 255)	0
0	AGC_PD	Power-down the AFC circuit. 0: Normal operation 1: Power-down	0

TABLE 211. AOC_CTRL: AUTOMATIC OFFSET CONTROL LSB ..... READ-WRITE, ADDR = 0x385(CH1)/0x395(CH2)/0x3A5(CH3)/0x3B5(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	AOC_OVWR_EN	Enable using AOC_OVWR value as offset. The value derived from auto calibration process will be ignored when this bit is “1”. 0: Disable 1: Enable	0
6:0	AOC_OVWR	This value is used as offset value when Overwrite Mode is set. The value is 0 ~ 127.	0x00

TABLE 212. AOC_CTRL: AUTOMATIC OFFSET CONTROL MSB. . . . . READ-WRITE, ADDR = 0x386(CH1)/0x396(CH2)/0x3A6(CH3)/0x3B6(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	Reserved	Reserved	0x00
1	AOC_2X_RANGE	Use 2X calibration range (0 ~ 255) 0: Normal range (0 ~ 127) 1: 2X range (0 ~ 255)	0
0	AOC_PD	Power-down the AOC circuit 0: Normal operation 1: Power-down NOTE: AOC has to be in power-down mode during normal operation.	1

TABLE 213. AUTO_AOC_AGC: AUTO AOC/AGC COMMAND . . . . . .READ-WRITE, ADDR = 0x387(CH1)/0x397(CH2)/0x3A7(CH3)/0x3B7(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	Reserved	Reserved	0x00
1	AUTO_AOC	Auto AOC Command Write 1 to this bit will initiate the AOC sweeping, the result will show in AOC status registers. This bit is self-clear.	0
0	AUTO_AGC	Auto AGC Command Write 1 to this bit will initiate the AGC sweeping, the result will show in AGC status registers. This bit is self-clear.	0

TABLE 214. RESERVED: . . . . . .READ-ONLY, ADDR = 0x388(CH1)/0x398(CH2)/0x3A8(CH3)/0x3B8(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	Reserved	Reserved	-

TABLE 215. AGC_STATUS: AGC STATUS LSB. . . . . .READ-ONLY, ADDR = 0x389(CH1)/0x399(CH2)/0x3A9(CH3)/0x3B9(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	AGC_COMP_OUT	AGC Comparator out 0: Offset issued by AGC control < Intrinsic offset 1: Offset issued by AGC control > Intrinsic offset	-
6:0	AGC_OFFSET	The offset value detected by AGC process. This value is 0 ~ 127	-

TABLE 216. AGC_STATUS: AGC STATUS MSB . . . . . .READ-ONLY, ADDR = 0x38A(CH1)/0x39A(CH2)/0x3AA(CH3)/0x3BA(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	Reserved	Reserved	-
1	AGC_CALIB_FAIL	This indicates the auto calibration process fail to detect a valid offset. 0: Not failed 1: Failed	0
0	AGC_CALIB_DONE	This indicates the auto calibration process is done. 0: In process 1: Done	1

TABLE 217. AOC_STATUS: AOC STATUS LSB . . . . . .READ-ONLY, ADDR = 0x38B(CH1)/0x39B(CH2)/0x3AB(CH3)/0x3BB(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	AOC_COMP_OUT	AOC Comparator out 0: Offset issued by AOC control < Intrinsic offset 1: Offset issued by AOC control > Intrinsic offset	-
6:0	AOC_OFFSET	The offset value detected by AOC process. This value is 0 ~ 127	-

TABLE 218. AOC_STATUS: AOC STATUS MSB . . . . . READ-ONLY, ADDR = 0x38C(CH1)/0x39C(CH2)/0x3AC(CH3)/0x3BC(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	Reserved	Reserved	-
1	AOC_CALIB_FAIL	This indicates the auto calibration process fail to detect a valid offset. 0: Not failed 1: Failed	-
0	AOC_CALIB_DONE	This indicates the auto calibration process is done. 0: In process 1: Done	-

SDI Ancillary Audio and Data Processor

TABLE 219. ANCAUDCTRL: ANCILLARY AUDIO CONTROL. . . . . READ-WRITE, ADDR = 0x800(CH1)/0x900(CH2)/0xA00(CH3)/0xB00(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	AUD_RIGHT	Select right or left alignment of 20-bit audio 0: 20-bit audio align left of 24-bit word (recommended) 1: 20-bit audio align right of 24-bit word	0
6	AUD_20	Select 20-bit or 24-bit audio 0: 24-bit audio (for HD SDI audio) 1: 20-bit audio (for SD SDI audio)	0
5:4	AUD_GROUP	Audio group to extract. Refer to SMPTE 272 for audio format/group/channel definitions. 00: Group 1 01: Group 2 10: Group 3 11: Group 4	00
3	AUD_MUTEB	Audio mute for the right channel (channel B) 0: Not muted 1: Muted	0
2	AUD_MUTEA	Audio mute for the left channel (channel A) 0: Not muted 1: Muted	0
1	AUD_FIFO_RST	Audio FIFO reset. Setting this bit resets both channel A and B FIFOs 0: Normal operation 1: Reset	0
0	AUD_EXT_EN	Enable audio data extraction 0: Disabled 1: Enabled	0

TABLE 220. ANCAUDSRC: ANCILLARY AUDIO SOURCE. . . . . READ-WRITE, ADDR = 0x801(CH1)/0x901(CH2)/0xA01(CH3)/0xB01(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
5:4	CHB_SRC	Specify the source channel number out of the four channels in a group to be extracted into audio channel B (right channel)	01
3:2	Reserved	Reserved	00
1:0	CHA_SRC	Specify the source channel number out of the four channels in a group to be extracted into audio channel A (left channel)	00

TABLE 221. ANC_AUD_DELAY: ANCILLARY AUDIO DELAY . . . . . READ-WRITE, ADDR = 0x802(CH1)/0x902(CH2)/0xA02(CH3)/0xB02(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	Reserved	Reserved	000
4:0	AUD_DELAY	Number of audio samples stored in FIFO before starting read out from the FIFO	0x00

TABLE 222. ANC_CTRL: ANCILLARY CONTROL ..... READ-WRITE, ADDR = 0x804(CH1)/0x904(CH2)/0xA04(CH3)/0xB04(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
5	HD_ANC_C2	Enable chroma (DS2) ancillary data extraction. This bit should be set in order for extracted data to be written in to the C2 FIFO. 0: Disabled 1: Enabled	0
4	HD_ANC_Y1	Enable luma (DS1) ancillary data extraction. This bit should be set in order for extracted data to be written in to the Y1 FIFO. 0: Disabled 1: Enabled	0
3:2	Reserved	Reserved	00
1	ANC_FIFO_RST	Ancillary FIFO reset. The data FIFOs are written whenever data packets are extracted. Once extracted, an interrupt is asserted. The host processor should read the data from the FIFOs and then assert this bit to bring the write counter back to 0 and make the Y1 and C2 FIFOs ready to receive new extracted data in the next frame. 0: Disabled 1: Enabled	0
0	ANC_EXT_EN	Enable ancillary data extraction. Set this bit in order to start extracting any ancillary data. 0: Disabled 1: Enabled	0

TABLE 223. ANC_TYPE1: ANCILLARY TYPE 1 LSB ..... READ-WRITE, ADDR = 0x806(CH1)/0x906(CH2)/0xA06(CH3)/0xB06(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE1L	Type 1 DID to extract. 0x00 means extract all. ANC_TYPE1[7:0]	0x00

TABLE 224. ANC_TYPE1: ANCILLARY TYPE 1 MSB .....READ-WRITE, ADDR = 0x807(CH1)/0x907(CH2)/0xA07(CH3)/0xB07(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE1M	Type 1 SDID to extract. ANC_TYPE1[15:8]	0x00

TABLE 225. ANC_TYPE2: ANCILLARY TYPE 2 LSB ..... READ-WRITE, ADDR = 0x808(CH1)/0x908(CH2)/0xA08(CH3)/0xB08(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE2L	Type 2 DID to extract. ANC_TYPE2[7:0]	0x00

TABLE 226. ANC_TYPE2: ANCILLARY TYPE 2 MSB..... READ-WRITE, ADDR = 0x809(CH1)/0x909(CH2)/0xA09(CH3)/0xB09(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE2M	Type 2 SDID to extract. ANC_TYPE2[15:8]	0x00

TABLE 227. ANC_TYPE3: ANCILLARY TYPE 3 LSB..... READ-WRITE, ADDR = 0x80A(CH1)/0x90A(CH2)/0xA0A(CH3)/0xB0A(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE3L	Type 3 DID to extract. ANC_TYPE3[7:0]	0x00

TABLE 228. ANC_TYPE3: ANCILLARY TYPE 3 MSB..... READ-WRITE, ADDR = 0x80B(CH1)/0x90B(CH2)/0xA0B(CH3)/0xB0B(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE3M	Type 3 SDID to extract. ANC_TYPE3[15:8]	0x00

TABLE 229. ANC_TYPE4: ANCILLARY TYPE 4 LSB ..... READ-WRITE, ADDR = 0x80C(CH1)/0x90C(CH2)/0xA0C(CH3)/0xB0C(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE4L	Type 4 DID to extract. ANC_TYPE4[7:0]	0x00

TABLE 230. ANC_TYPE4: ANCILLARY TYPE 4 MSB..... READ-WRITE, ADDR = 0x80D(CH1)/0x90D(CH2)/0xA0D(CH3)/0xB0D(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE4M	Type 4 SDID to extract. ANC_TYPE4[15:8]	0x00

TABLE 231. ANC_TYPE5: ANCILLARY TYPE 5 LSB ..... READ-WRITE, ADDR = 0x80E(CH1)/0x90E(CH2)/0xA0E(CH3)/0xB0E(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE5L	Type 5 DID to extract. ANC_TYPE5[7:0]	0x00

TABLE 232. ANC_TYPE5: ANCILLARY TYPE 5 MSB..... READ-WRITE, ADDR = 0x80F(CH1)/0x90F(CH2)/0xA0F(CH3)/0xB0F(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_TYPE5M	Type 5 SDID to extract. ANC_TYPE5[15:8]	0x00

TABLE 233. ANC_LINE1: ANCILLARY LINE 1 LSB ..... READ-WRITE, ADDR = 0x810(CH1)/0x910(CH2)/0xA10(CH3)/0xB10(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_LINE1L	Line 1 to extract ancillary data. ANC_LINE1[7:0]	0x00

TABLE 234. ANC_LINE1: ANCILLARY LINE 1 MSB..... READ-WRITE, ADDR = 0x811(CH1)/0x911(CH2)/0xA11(CH3)/0xB11(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	0x00
2:0	ANC_LINE1M	Line 1 to extract ancillary data. ANC_LINE1[10:8]	000

TABLE 235. ANC_LINE2: ANCILLARY LINE 2 LSB ..... READ-WRITE, ADDR = 0x812(CH1)/0x912(CH2)/0xA12(CH3)/0xB12(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_LINE2L	Line 2 to extract ancillary data. ANC_LINE2[7:0]	0x00

TABLE 236. ANC_LINE2: ANCILLARY LINE 2 MSB..... READ-WRITE, ADDR = 0x813(CH1)/0x913(CH2)/0xA13(CH3)/0xB13(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	Reserved	Reserved	0x00
2:0	ANC_LINE2M	Line 2 to extract ancillary data. ANC_LINE2[10:8]	000

TABLE 237. ANC_DETEN: ANCILLARY DETECTION ENABLE . . . . . READ-WRITE, ADDR = 0x820(CH1)/0x920(CH2)/0xA20(CH3)/0xB20(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	ANC_DATA_C_DET_EN	Interrupt enable for ancillary data packet upper 10-bit detection 0: Disabled 1: Enabled	0
6	ANC_DATA_Y_DET_EN	Interrupt enable for ancillary data packet lower 10-bit detection 0: Disabled 1: Enabled	0
5	AUD_UFLOW_DET_EN	Interrupt enable for audio FIFO underflow detection 0: Disabled 1: Enabled	0
4	AUD_OFLOW_DET_EN	Interrupt enable for audio FIFO overflow detection 0: Disabled 1: Enabled	0
3	ANC_DET_EN	Interrupt enable for ancillary data detection 0: Disabled 1: Enabled	0
2	AUD_AUX_DET_EN	Interrupt enable for audio auxiliary data detection 0: Disabled 1: Enabled	0
1	AUD_CTRL_DET_EN	Interrupt enable for audio control data detection 0: Disabled 1: Enabled	0
0	AUD_DATA_DET_EN	Interrupt enable for audio data detection 0: Disabled 1: Enabled	0

TABLE 238. ANC_DET: ANCILLARY DETECTION . . . . . READ-ONLY, ADDR = 0x821(CH1)/0x921(CH2)/0xA21(CH3)/0xB21(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	ANC_DATA_C_DET	Ancillary data upper packet 10-bit detection 0: Not detected 1: Detected	0
6	ANC_DATA_Y_DET	Ancillary data lower packet 10-bit detection 0: Not detected 1: Detected	0
5	AUD_UFLOW_DET	Audio FIFO underflow detection 0: Not detected 1: Detected	0
4	AUD_OFLOW_DET	Audio FIFO overflow detection 0: Not detected 1: Detected	0
3	ANC_DET	Ancillary data detection 0: Not detected 1: Detected	0
2	AUD_AUX_DET	Audio auxiliary data detection 0: Not detected 1: Detected	0
1	AUD_CTRL_DET	Audio control data detection 0: Not detected 1: Detected	0
0	AUD_DATA_DET	Audio data detection 0: Not detected 1: Detected	0

TABLE 239. ANCAUDFRM12: ANC AUDIO FRAME 12 LSB . . . . . READ-ONLY, ADDR = 0x824(CH1)/0x924(CH2)/0xA24(CH3)/0xB24(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AF_12L	Audio frame number for channels 1 and 2. AF12[7:0]	0x00

TABLE 240. ANCAUDFRM12: ANC AUDIO FRAME 12 MSB. . . . . READ-ONLY, ADDR = 0x825(CH1)/0x925(CH2)/0xA25(CH3)/0xB25(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
0	AF_12M	Audio frame number for channels 1 and 2. AF12[8]	0

TABLE 241. ANCAUDFRM34: ANC AUDIO FRAME 34 LSB . . . . . READ-ONLY, ADDR = 0x826(CH1)/0x926(CH2)/0xA26(CH3)/0xB26(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AF_34L	Audio frame number for channels 3 and 4. AF34[7:0]	0x00

TABLE 242. ANCAUDFRM34: ANC AUDIO FRAME 34 MSB. . . . . READ-ONLY, ADDR = 0x827(CH1)/0x927(CH2)/0xA27(CH3)/0xB27(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	Reserved	Reserved	00
0	AF_34M	Audio frame number for channels 3 and 4. AF34[8]	0

TABLE 243. ANCAUDRATE: ANCILLARY AUDIO RATE . . . . . READ-ONLY, ADDR = 0x828(CH1)/0x928(CH2)/0xA28(CH3)/0xB28(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	ARATE_34	Rate code for channels 3 and 4 0: 48kHz 1: 44.1kHz 2: 32kHz 3-6: Reserved 7: Undefined (free-running)	-
4	ASYN_34	Synchronous 3 and 4 0: Channels 3 and 4 are running synchronously 1: Channels 3 and 4 are running asynchronously	-
3:1	ARATE_12	Rate code for channels 1 and 2 0: 48kHz 1: 44.1kHz 2: 32kHz 3-6: Reserved 7: Undefined (free-running)	-
0	ASYN_12	Synchronous 1 and 2 0: Channels 1 and 2 are running synchronously 1: Channels 1 and 2 are running asynchronously	-

TABLE 244. ANCAUDACT: ANCILLARY ACTIVE AUDIO CHANNELS . . . . . .READ-ONLY, ADDR = 0x829(CH1)/0x929(CH2)/0xA29(CH3)/0xB29(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	-
3	AACT_4	Channel 4 0: Inactive 1: Active	-
2	AACT_3	Channel 3 0: Inactive 1: Active	-
1	AACT_2	Channel 2 0: Inactive 1: Active	-
0	AACT_1	Channel 1 0: Inactive 1: Active	-

TABLE 245. ANCAUDDELA0: ANCILLARY AUDIO DELAY A0 . . . . . .READ-ONLY, ADDR = 0x82A(CH1)/0x92A(CH2)/0xA2A(CH3)/0xB2A(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	ADELA0	A1DELA[6:0] If DELA E bit is 1: DELA represents the audio channel 1 accumulated audio processing delay relative to video, measured in audio sample intervals. If DELA E bit is 0: DELA represents the audio channel 1 and 2 accumulated audio processing delay relative to video, measure in audio sample intervals.	0x00
0	ADELAE	E bit of DELA. Indicates whether DELA is valid audio delay data. 0: Not valid 1: Valid	0

TABLE 246. ANCAUDDELA1: ANCILLARY AUDIO DELAY A1 . . . . . .READ-ONLY, ADDR = 0x82B(CH1)/0x92B(CH2)/0xA2B(CH3)/0xB2B(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELA1	A1DELA[15:8]	0x00

TABLE 247. ANCAUDDELA2: ANCILLARY AUDIO DELAY A2 . . . . . .READ-ONLY, ADDR = 0x82C(CH1)/0x92C(CH2)/0xA2C(CH3)/0xB2C(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELA2	A1DELA[24:17]	0x00

TABLE 248. ANCAUDDELB0: ANCILLARY AUDIO DELAY B0 . . . . . READ-ONLY, ADDR = 0x82D(CH1)/0x92D(CH2)/0xA2D(CH3)/0xB2D(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	ADELB0	A1DELB[6:0] If DELB E bit is 1: DELB represents the audio channel 3 accumulated audio processing delay relative to video, measured in audio sample intervals. If DELB E bit is 0: DELB represents the audio channel 3 and 4 accumulated audio processing delay relative to video, measure in audio sample intervals.	0x00
0	ADELBE	E bit of DELB. Indicates whether DELB is valid audio delay data. 0: Not valid 1: Valid	0

TABLE 249. ANCAUDDELB1: ANCILLARY AUDIO DELAY B1 . . . . . READ-ONLY, ADDR = 0x82E(CH1)/0x92E(CH2)/0xA2E(CH3)/0xB2E(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELB1	A1DELB[15:8]	0x00

TABLE 250. ANCAUDDELB2: ANCILLARY AUDIO DELAY B2 . . . . . READ-ONLY, ADDR = 0x82F(CH1)/0x92F(CH2)/0xA2F(CH3)/0xB2F(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELB2	A1DELB[23:16]	0x00

TABLE 251. ANCAUDDELC0: ANCILLARY AUDIO DELAY C0 . . . . . READ-ONLY, ADDR = 0x830(CH1)/0x930(CH2)/0xA30(CH3)/0xB30(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	ADELC0	A1DELC[6:0] If DELC E bit is 1: DELC represents the audio channel 2 accumulated audio processing delay relative to video, measured in audio sample intervals. If DELC E bit is 0: DELC is not valid audio processing delay data.	0x00
0	ADELCE	E bit of DELC. Indicates whether DELC is valid audio delay data. 0: Not valid 1: Valid	0

TABLE 252. ANCAUDDELC1: ANCILLARY AUDIO DELAY C1 . . . . . READ-ONLY, ADDR = 0x831(CH1)/0x931(CH2)/0xA31(CH3)/0xB31(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELC1	A1DELC[15:8]	0x00

TABLE 253. ANCAUDDELC2: ANCILLARY AUDIO DELAY C2 . . . . . READ-ONLY, ADDR = 0x832(CH1)/0x932(CH2)/0xA32(CH3)/0xB32(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELC2	A1DELC[24:17]	0x00

TABLE 254. ANCAUDDELD0: ANCILLARY AUDIO DELAY D0 . . . . . READ-ONLY, ADDR = 0x833(CH1)/0x933(CH2)/0xA33(CH3)/0xB33(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	ADELD0	A1DELD[6:0] If DELD E bit is 1: DELD represents the audio channel 4 accumulated audio processing delay relative to video, measured in audio sample intervals. If DELD E bit is 0: DELD is not valid audio processing delay data.	0x00
0	ADELDE	E bit of DELD. Indicates whether DELD is valid audio delay data. 0: Not valid 1: Valid	0

TABLE 255. ANCAUDDELD1: ANCILLARY AUDIO DELAY D1 . . . . . READ-ONLY, ADDR = 0x834(CH1)/0x934(CH2)/0xA34(CH3)/0xB34(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELD1	A1DELD[15:8]	0x00

TABLE 256. ANCAUDDELD2: ANCILLARY AUDIO DELAY D2 . . . . . READ-ONLY, ADDR = 0x835(CH1)/0x935(CH2)/0xA35(CH3)/0xB35(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADELD2	A1DELD[24:17]	0x00

TABLE 257. ANC_Y1DID: ANCILLARY Y1 DID . . . . . READ-ONLY, ADDR = 0x838(CH1)/0x938(CH2)/0xA38(CH3)/0xB38(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_Y1DID	DID for ancillary data package in FIFO for luma (DS1)	0x00

TABLE 258. ANC_Y1SDID: ANCILLARY Y1 SDID . . . . . READ-ONLY, ADDR = 0x839(CH1)/0x939(CH2)/0xA39(CH3)/0xB39(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_Y1SDID	SDID for ancillary data package in FIFO for luma (DS1)	0x00

TABLE 259. ANC_Y1DC: ANCILLARY Y1 DC . . . . . READ-ONLY, ADDR = 0x83A(CH1)/0x93A(CH2)/0xA3A(CH3)/0xB3A(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_Y1DC	Data count (DC) for ancillary data package in FIFO for luma (DS1)	0x00

TABLE 260. ANC_C2DID: ANCILLARY C2 DID. . . . . READ-ONLY, ADDR = 0x83C(CH1)/0x93C(CH2)/0xA3C(CH3)/0xB3C(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_C2DID	DID for ancillary data package in FIFO for chroma (DS2)	0x00

TABLE 261. ANC_C2SDID: ANCILLARY C2 SDID . . . . . READ-ONLY, ADDR = 0x83D(CH1)/0x93D(CH2)/0xA3D(CH3)/0xB3D(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_C2SDID	DID for ancillary data package in FIFO for chroma (DS2)	0x00

TABLE 262. ANC_C2DC: ANCILLARY C2 DC . . . . . READ-ONLY, ADDR = 0x83E(CH1)/0x93E(CH2)/0xA3E(CH3)/0xB3E(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_C2DC	Data count (DC) for ancillary data package in FIFO for chroma (DS2)	0x00

TABLE 263. ANCAUD_MAS_CTRL: ANCILLARY AUDIO MASTER CONTROL. . . READ-WRITE, ADDR = 0x840(CH1)/0x940(CH2)/0xA40(CH3)/0xB40(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	Reserved	Reserved	0x00
1	ANCAUD_ASYNROEN	Define input/output mode on the ASYNR pin when the single channel Ancillary audio output mode is selected. 0: Output (recommended for the single SDI ANC audio) 1: Input	1
0	ANCAUD_ ACLKRMASTER	Define input/output mode on the ACLKR pin and set up audio system processing when the single channel Ancillary audio output mode is selected. 0: ACLKR pin is input. External 256 x f_S or 320 x f_S or 384 x f_S clock should be connected to ACLKR pin by AIN5MD/AFS384 setting. 1: ACLKR pin is output. Internal ACKG generates audio system clock. (recommended for the single SDI ANC audio)	0

TABLE 264. ANCAUD_CLK_CTRL: ANCILLARY AUDIO CLOCK CONTROL. . . . . READ-WRITE, ADDR = 0x84B(CH1)/0x94B(CH2)/0xA4B(CH3)/0xB4B(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	Reserved	Reserved	0x0
3	ANCAUD_AFAUTO	ACKI[21:0] control automatic setup with ANCAUD_AFMD registers. This mode is only effective when ANCAUD_ACLKRMASTER = 1. 0: ACKI[21:0] registers set up ACKI control. 1: ACKI control is automatically set up by ANCAUD_AFMD register value.	1
2:0	ANCAUD_AFMD	AFAUTO control mode 000: 8kHz setting (default) 001: 16kHz setting 010: 32kHz setting 011: 44.1kHz setting 100: 48kHz setting (recommended for the single SDI ANC audio)	000

TABLE 265. ANCAUD_I2S_CTRL: ANCILLARY AUDIO I2S CONTROL . . . . . READ-WRITE, ADDR = 0x84C(CH1)/0x94C(CH2)/0xA4C(CH3)/0xB4C(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7	Reserved	Reserved	0
6	ANCAUD_MASCKMD	Audio clock master ACLKR output wave format 0: High period is one 36MHz clock period (recommended for the single SDI ANC audio) 1: Almost duty 50-50% clock output on ACLKR pin. NOTE: If this mode is selected, two times bigger number value need to be set up ACKI registers. If ANCAUD_AFAUTO = 1, ACKI control is automatically set up even if ANCAUD_MASCKMD = 1, SDIV = 00h is used with this function normally.	1
5:0	Reserved	Reserved	0x00

TABLE 266. ANCAUD_FSMODE: ANCILLARY AUDIO f_S MODE CONTROL . . . . . READ-WRITE, ADDR = 0x84D(CH1)/0x94D(CH2)/0xA4D(CH3)/0xB4D(CH4)

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	Reserved	Reserved	000
4	ANCAUD_ACLKR64	ACLKR clock output mode for special 4 word output interface. ANCAUD_ACLKRMASTER = 1 mode only. 0: ACLKR output is normal 1: The number of ACLKR clock per f_S is 64. (recommended for the single SDI ANC audio)	1
3:0	Reserved	Reserved	0x0

TABLE 267. ANC_ACCESS: ANCILLARY RAW DATA ACCESS LSB
. . . . . READ-ONLY, ADDR = 0xC00+2n(CH1)/0xE00+2n(CH2)/0x1000+2n(CH3)/0x1200+2n(CH4), (n = 0 ~ 255)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_DATA_Y	Y raw data 8-bit buffer values up to 256 bytes NOTE: In SPI mode, the data is 16-bit, so the data can be accessed by even number of address.	-

TABLE 268. ANC_ACCESS: ANCILLARY RAW DATA ACCESS MSB
. . . . . READ-ONLY, ADDR = 0xC00+(2n+1)(CH1)/0xE00+(2n+1)(CH2)/0x1000+(2n+1)(CH3)/0x1200+(2n+1)(CH4), (n = 0~255)

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANC_DATA_C	C raw data 8-bit buffer values up to 256 bytes	-

Layout Guidelines

Specific printed circuit board (PCB) layout guidelines should be followed for optimal TW6874 performance. Special care should be given to the to the following subsections in order of layout priority:

- SDI routing
- Power supply routing
- Parallel video routing
- Power supply bypassing

These are each addressed in the following sections.

SDI Routing

The SDI pins receive high speed (up to Gbps) data over long cable reaches. These signals will be heavily filtered due to the cable effects. Special care is required in designing the PCB interface for these pins, otherwise poor return loss and suboptimal cable reach will occur.

Typically, the SDIP input consists of: BNC connector, return loss network (75Ω resistor in parallel with an 15nH inductor), 75Ω termination resistor to ground and 4.7µF AC-coupling capacitor to the SDIP pin. The SDIN input consists of just a 37.4Ω termination resistor to ground and 4.7µF AC-coupling capacitor to the SDIN pin. It is recommended to use 1% for the 75/37.4Ω resistors on the SDI input circuit.

Since the termination networks are 75Ω, the PCB trace characteristic impedance must also be 75Ω single-ended. These traces should be on the top layer and not transition to any other layer, which would cause impedance discontinuities. The adjacent reference (ground) plane should be a solid, continuous copper plane.

A PCB stackup/spacing should be chosen such that the trace width to give 75Ω is approximately as wide as the component landing pads in order to minimize impedance discontinuities. In this regard, the physically smallest components should be used. Imperial code 0402 (metric code 1005) size is recommended.

The AC-coupling capacitors (C62 and C63 in Figure 34) should be placed as close as possible to the TW6874's SDIP/N pins. The termination resistors (R46 and R47) should be adjacent to these caps. The return loss network (L7 and R48) should be adjacent to the termination resistor.

A high quality BNC connector should be chosen. Typically edge launch BNC connectors, such as the Samtec BNC7T-J-P-XX-ST-EM1, give better frequency response than right angle or vertical connectors. To optimize return loss, the total trace length from BNC connector to SDIP should be as short as possible.

To minimize crosstalk, each of the four SDI inputs should be isolated by a ground fill as shown in Figure 35. Ground pour can be used on each layer. Use multiple vias to tie the grounds together.

It is advised to follow the reference layout to meet these criteria. Figures 34 and 35 show the reference schematic and layout meeting these requirements. The PCB stackup used in this design is:

- Layer 1: TW6874 + SDI signal + GND fill
- Layer 2: GND fill
- Layer 3: Analog Power (1.0V/1.8V) + GND fill
- Layer 4: Signal + GND fill
- Layer 5: Digital Power (1.0V/3.3V) + GND fill
- Layer 6: Signal + GND fill

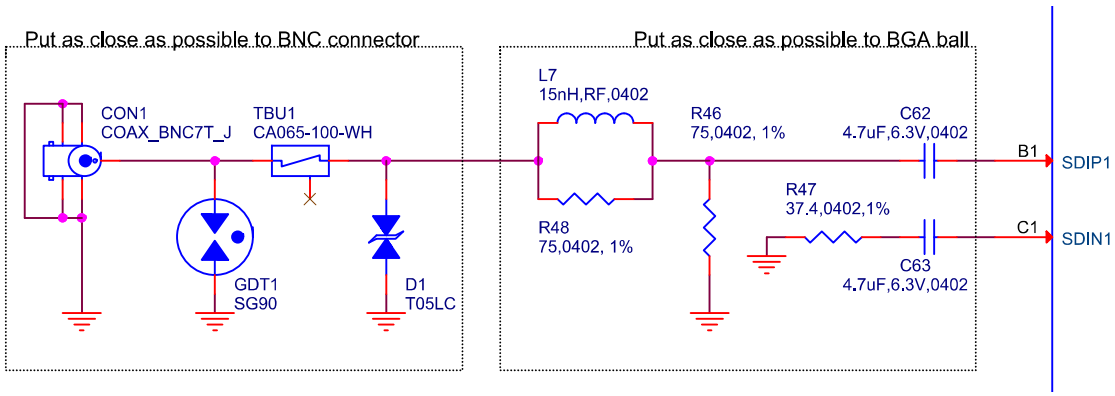


FIGURE 34. SDIP/SDIN INPUT SCHEMATIC

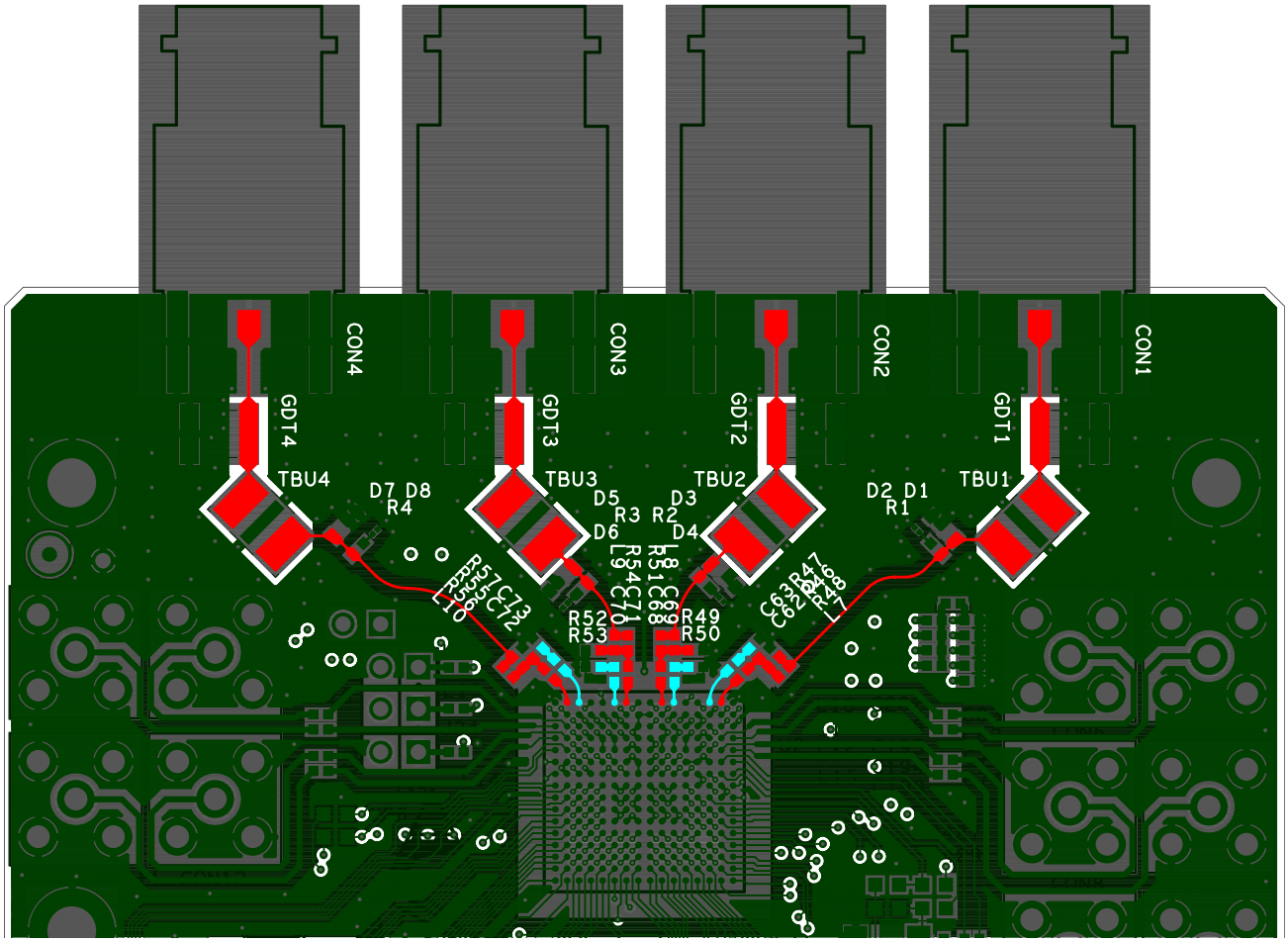


FIGURE 35. SDI1-4 LAYOUT LAYER 1

Digital Video Routing

The parallel video output pins toggle at 27MHz for SD video (8-bit data + clock), 74.25MHz for HD video (16-bit data + clock) or 148.5MHz for HD video (8-bit + clock). The traces connected to these pins must be matched in length for all data bits plus clock.

The LVCMOS traces are typically routed as 50Ω single-ended, but it is not critical. The traces are also allowed to transition between layers for ease of routing. A 33Ω series termination should be placed near each of the driver pins. Series termination prevents overshoot and ringing, leading to improved EMI performance.

Power Supply Routing

The TW6874 uses 21 analog supply domains (11 1.0V pins and 10 1.8V pins) and two digital supply domains (13 DVDD_3V3 1.8V to 3.3V pins and 13 DVDD_1V0 1.0V pins). Switching regulators that generate a 3.3V and 1.0V rail for the digital domains can be used. However, LDOs that generate 1.0V and 1.8V for analog are required.

For the analog 1.8V regulator, AVDD_REG1/2/3/4, AVDD_PLL18 and AVDD_BG must be isolated from all other supplies by a ferrite bead on each pin. Furthermore, these six pins must have a 1nF bypass capacitor in addition to a 0.1µF capacitor. The other four 1.8V analog supply pins can be grouped by one ferrite bead.

For the analog 1.0V regulator, AVDD_CDR1/2/3/4, AVDD_PLL10, AVDD_XTAL and AVDD_GUARD must be isolated from all other supplies by a ferrite bead on each pin. Furthermore, these seven pins must have a 1nF bypass capacitor in addition to a 0.1µF capacitor. The other four 1.0V analog supply pins can be grouped by one ferrite bead.

For DVDD_1V0 and DVDD_3V3, a single ferrite bead can be used from each power regulator to all pins in each domain.

Ideally, a low impedance plane will route to each pin, but a wide trace can also be used. Also, analog ground plane and digital ground plane shall be separated, only to be jointed at a location far away from the device, for example, next to the power supply module.

Power Supply Bypassing

It is important that the various supplies be well bypassed over a wide range of frequencies, from below the typical loop bandwidth of the PLL to approaching the signal bit rate of the serial data. A combination of different values of capacitors from 1000pF to 5µF or more with low ESR characteristics is generally required.

Each power supply plane should be adjacent to a ground plane in order to create a large capacitance with little to no inductance. This will minimize ground bounce and improve power supply bypassing.

The dielectric thickness separating these layers should be as thin as possible. Board houses are able to create spacings of as small as 3 mils with today's technology. A material with a large dielectric constant helps to effect a large capacitance.

BULK CAPACITORS

These physically large, high value capacitors need to be chosen carefully, with special care regarding their ESR. Very good results can be obtained with multilayer ceramic capacitors, available from many suppliers and generally in small outlines, which provide good bypass capabilities down to a few mΩ at 1MHz to 2MHz. Other capacitor technologies may also be suitable but "classic" electrolytic capacitors frequently have ESR values of above 1Ω, that nullify any decoupling effect above the 1kHz to 10kHz frequency range.

Ferrite beads may be used to isolate sensitive voltage rails from the other voltage rails and to prevent noisy voltage rails from affecting the power supply bus. If a ferrite bead is used on a voltage rail, another bulk capacitor should be used in a pi-filter configuration on that voltage rail in order to provide instantaneous charge for that rail.

LOCAL BYPASS CAPACITORS

A physically small, low value capacitor should bypass each IC supply pin to ground. Capacitors of 0.1µF offer low impedance in the 10MHz to 20MHz region and 1000pF capacitors in the 100MHz to 200MHz region. Minimize trace length and vias to minimize inductance and maximize noise rejection.

Figure 36 demonstrates a common but non-ideal PCB layout and its equivalent circuit. The additional trace inductance between the bypass capacitor and the power supply/IC reduces its effectiveness. Figure 37 demonstrates a better layout. In this case there is still series trace inductance (it is impossible to completely eliminate it), but now it is being put to good use as part of a T-filter, attenuating supply noise before it gets to the IC and reducing the amount of IC-generated noise that gets injected into the supply. Figures 38 and 39 show the same effect when the bypass capacitor must be placed on the opposite side of the PCB from the IC.

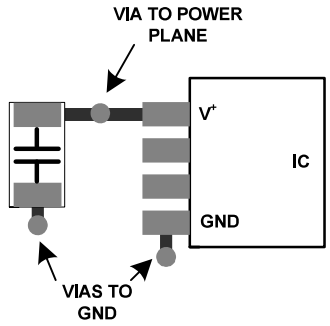


FIGURE 36. SUB-OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT — CAPACITOR AND IC ON SAME PCB LAYER

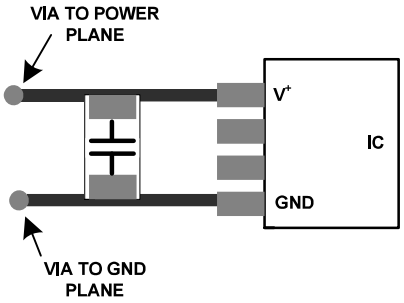


FIGURE 37. OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT — CAPACITOR AND IC ON SAME PCB LAYER

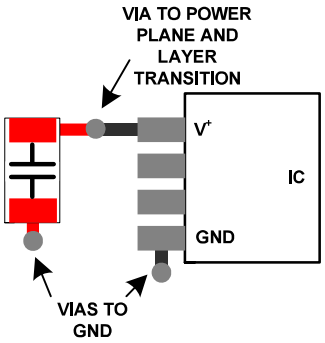


FIGURE 38. SUB-OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT — CAPACITOR AND IC ON OPPOSITE PCB LAYERS

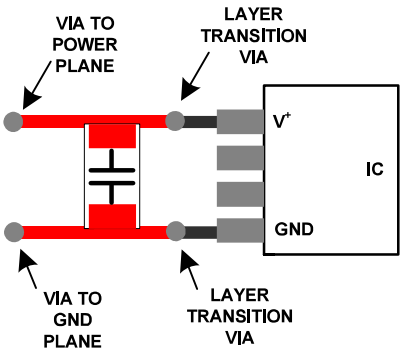


FIGURE 39. OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT — CAPACITOR AND IC ON OPPOSITE PCB LAYERS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
March 25, 2015	FN8430.1	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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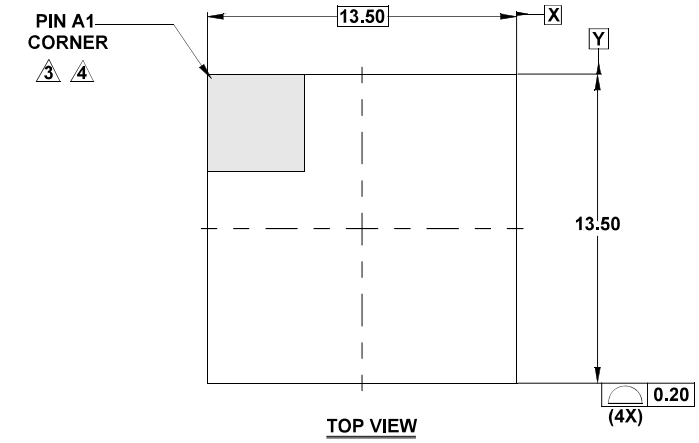
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

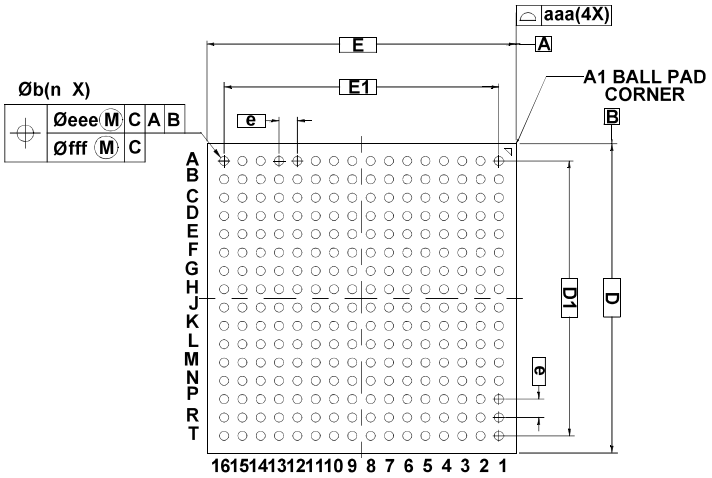
V256.13.5x13.5

256 LOW PROFILE, FINE PITCH PLASTIC BALL GRID ARRAY PACKAGE (LFBGA)

Rev 0, 3/13

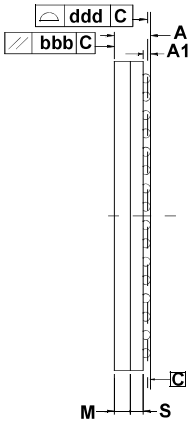


TOP VIEW

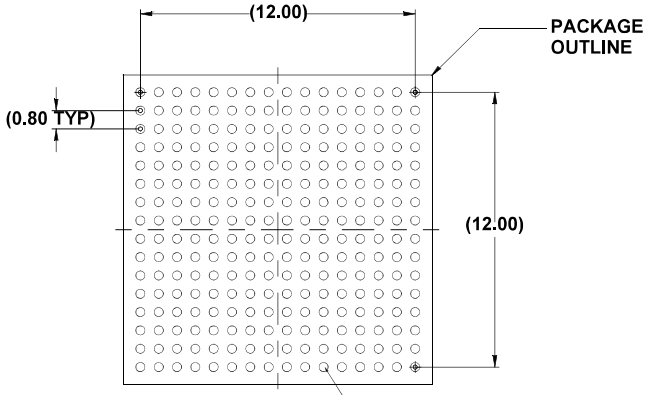


BOTTOM VIEW

		SYMBOL	COMMON DIMENSIONS		
			MIN	NOM	MAX
Package			LFBGA		
Body Size	X	E		13.50	
	Y	D		13.50	
Ball Pitch		e		0.800	
Total Thickness		A	-	-	1.700
Mold Thickness		M		0.700 Ref.	
Substrate Thickness		S		0.560 Ref.	
Ball Diameter				0.400	
Stand Off		A1	0.270	-	0.370
Ball Width		b	0.380	-	0.480
Package Edge Tolerance		aaa		0.150	
Mold Parallelism		bbb		0.200	
Coplanarity		ddd		0.120	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.080	
Ball Count		n		256	
Edge Ball Center to Center	X	E1		12.000	
	Y	D1		12.000	



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN

NON SOLDER MASK DEFINED
PAD 0.38 NOM/0.40mm
DIAMETER MAX.