SN74ABT3614
64 × 36 × 2 CLOCKED BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY WITH BUS MATCHING AND BYTE SWAPPING

SCBS126H – JUNE 1992 – REVISED APRIL 2000

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox-Bypass Register for Each FIFO**
- **Dynamic Port-B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte-Order Swapping on Port B**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**

- **$\overline{\text{EFA}}$, $\overline{\text{FFA}}$, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **$\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Package Options Include 120-Pin Thin Quad Flat (PCB) and 132-Pin Quad Flat (PQ) Packages**

description

The SN74ABT3614 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read-access times as fast as 10 ns. Two independent 64 × 36 dual-port SRAM FIFOs in this device buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags, almost full ($\overline{\text{AF}}$) and almost empty ($\overline{\text{AE}}$) to indicate when a selected number of words is stored in memory. FIFO data on port B can be input and output in 36-bit, 18-bit, and 9-bit formats, with a choice of big- or little-endian configurations. Three modes of byte-order swapping are possible with any bus-size selection. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port.

The SN74ABT3614 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses controlled by a synchronous interface.

The full flag and almost-full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag and almost-empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

The SN74ABT3614 is characterized for operation from 0°C to 70°C.

For more information on this device family, see the following application reports:

- *FIFO Mailbox-Bypass Registers: Using Bypass Registers to Initialize DMA Control* (literature number SCAA007)

- *Advanced Bus-Matching/Byte-Swapping Features for Internetworking FIFO Applications* (literature number SCAA014)

- *Parity-Generate and Parity-Check Features for High-Bandwidth-Computing FIFO Applications* (literature number SCAA015)

- *Internetworking the SN74ABT3614* (literature number SCAA015)

- *Metastability Performance of Clocked FIFOs* (literature number SCZA004)

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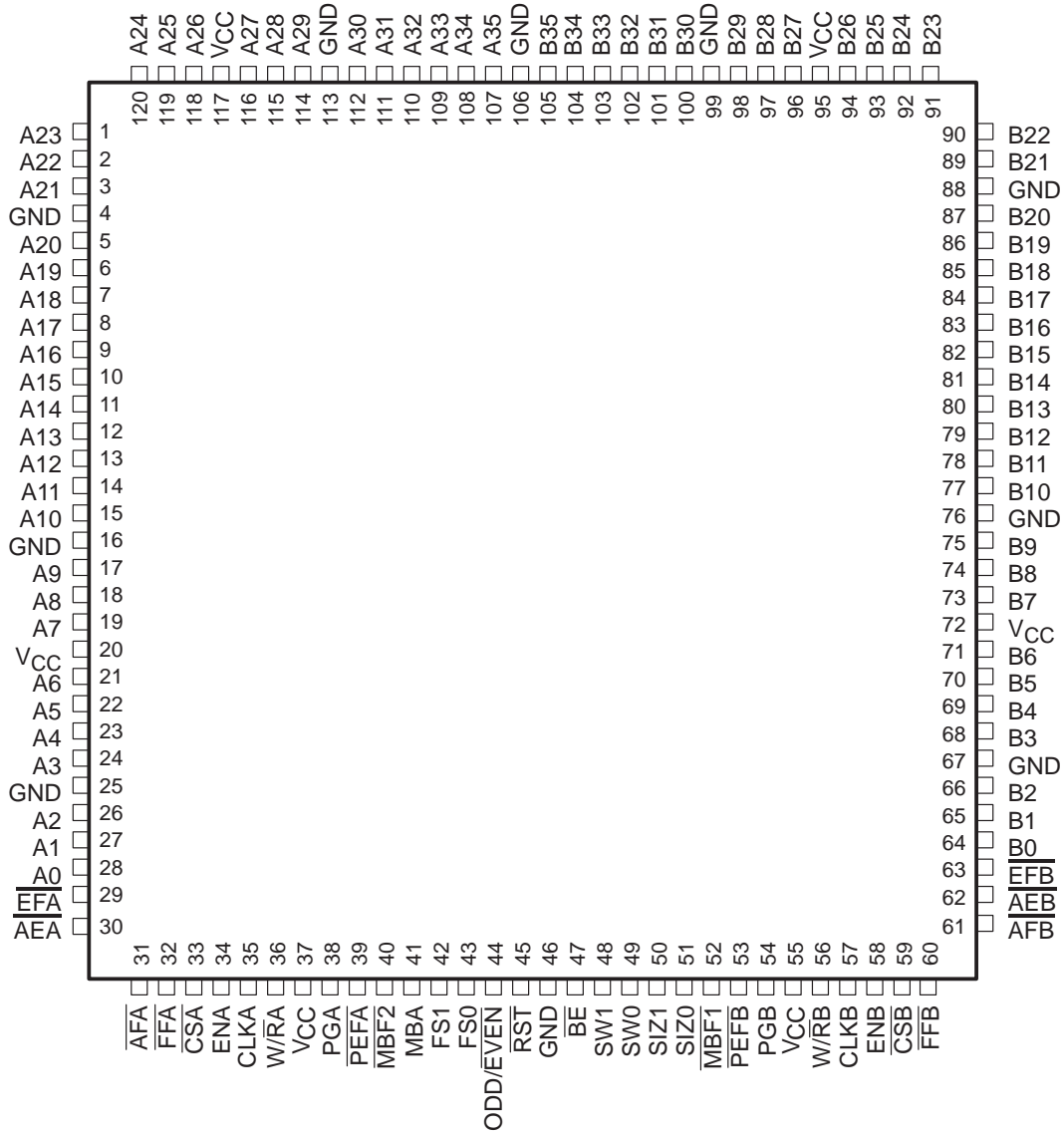
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TEXAS INSTRUMENTS

SN74ABT3614

64 × 36 × 2 CLOCKED BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY WITH BUS MATCHING AND BYTE SWAPPING

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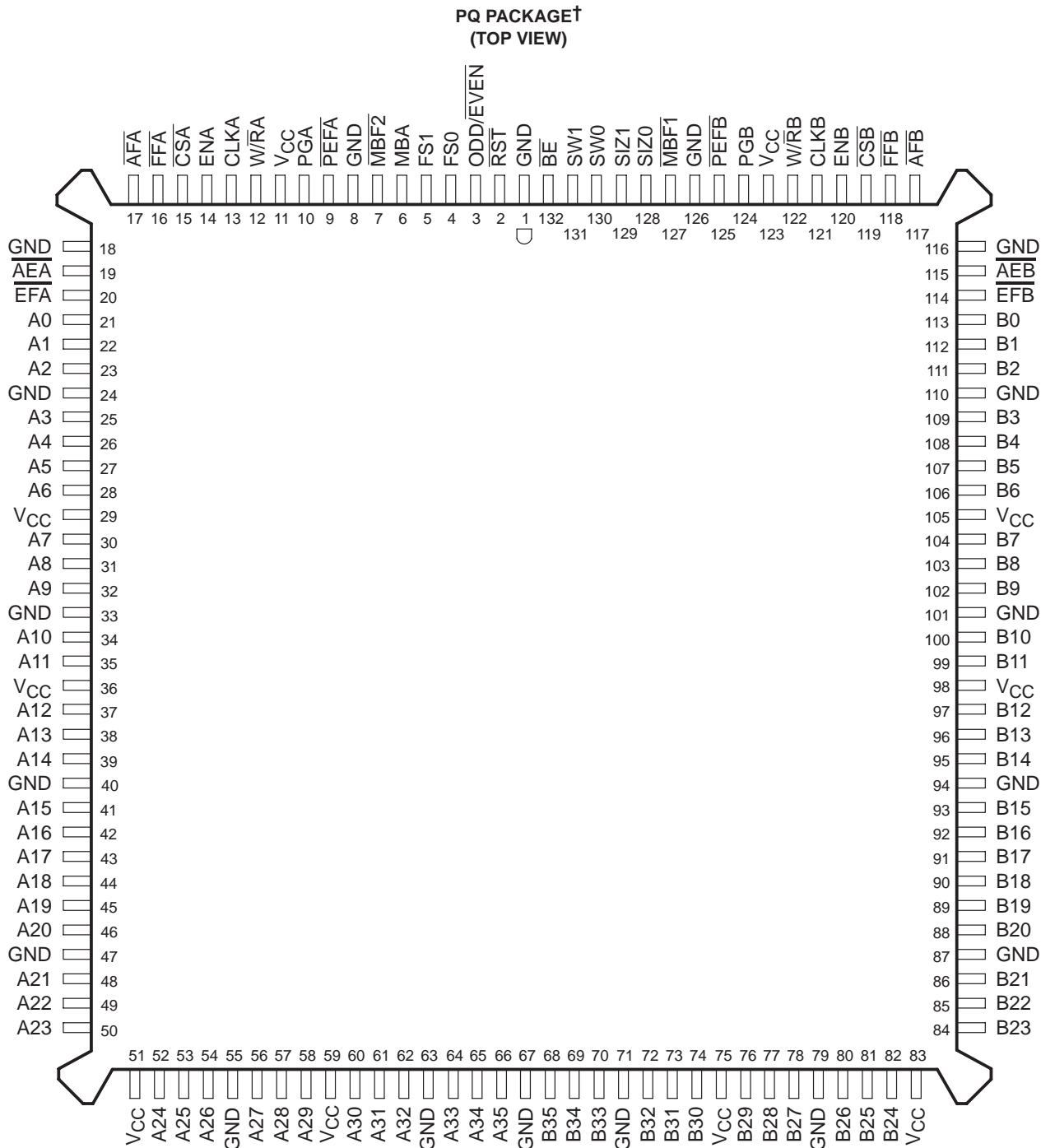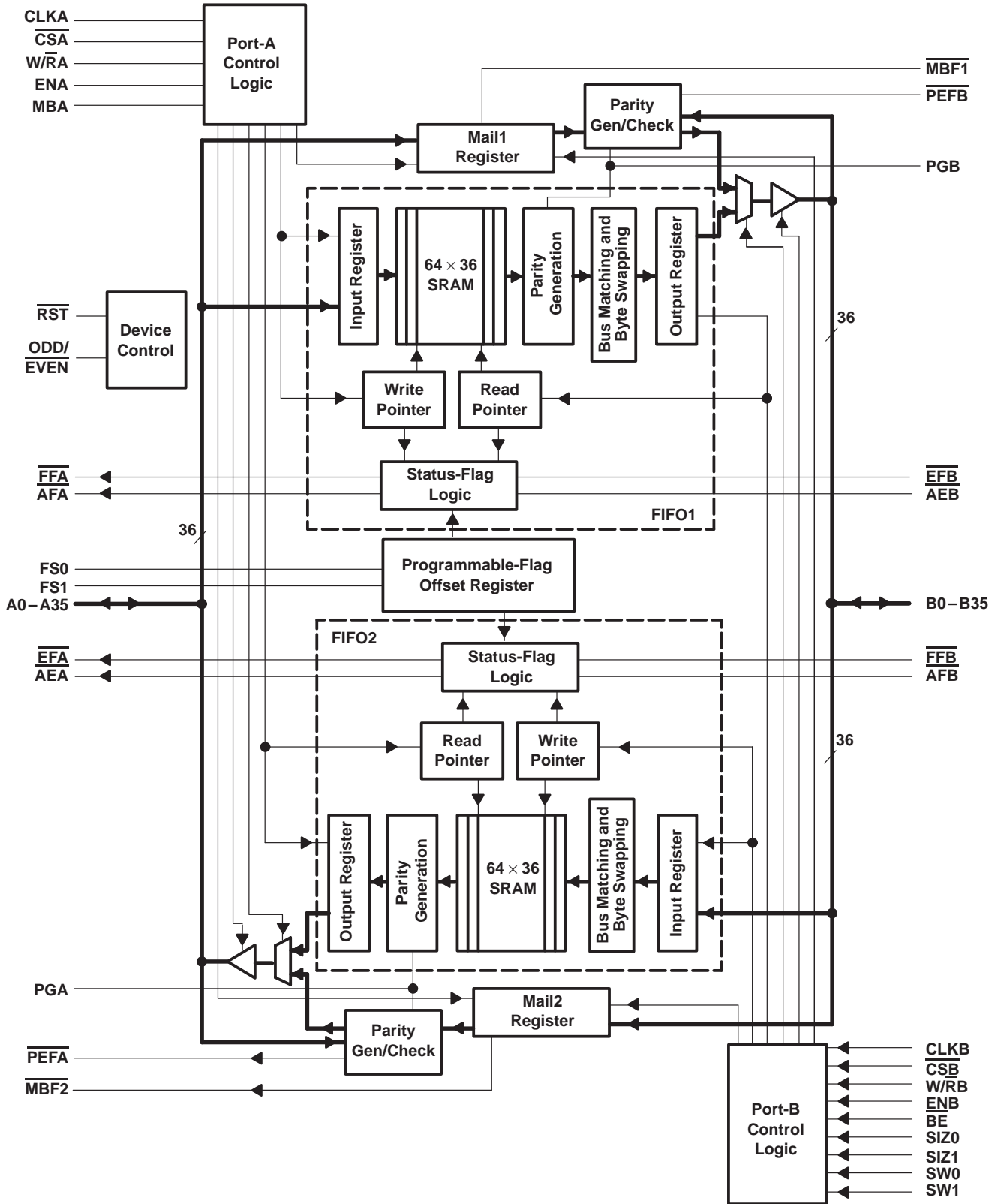
PCB PACKAGE
(TOP VIEW)

Top pins (120 to 91): A24, A25, A26, VCC, A27, A28, A29, GND, A30, A31, A32, A33, A34, A35, GND, B35, B34, B33, B32, B31, B30, GND, B29, B28, B27, VCC, B26, B25, B24, B23

Left pins (1 to 30):
Pin	Signal
1	A23
2	A22
3	A21
4	GND
5	A20
6	A19
7	A18
8	A17
9	A16
10	A15
11	A14
12	A13
13	A12
14	A11
15	A10
16	GND
17	A9
18	A8
19	A7
20	V_{CC}
21	A6
22	A5
23	A4
24	A3
25	GND
26	A2
27	A1
28	A0
29	$\overline{EFA}$
30	AEA

Right pins (90 to 61):
Pin	Signal
90	B22
89	B21
88	GND
87	B20
86	B19
85	B18
84	B17
83	B16
82	B15
81	B14
80	B13
79	B12
78	B11
77	B10
76	GND
75	B9
74	B8
73	B7
72	V_{CC}
71	B6
70	B5
69	B4
68	B3
67	GND
66	B2
65	B1
64	B0
63	$\overline{EFB}$
62	$\overline{AEB}$
61	AFB

Bottom pins (31 to 60): $\overline{AFA}$, FFA, $\overline{CSA}$, ENA, CLKA, W/$\overline{RA}$, VCC, PGA, $\overline{PEFA}$, $\overline{MBF2}$, MBA, FS1, FS0, ODD/$\overline{EVEN}$, $\overline{RST}$, GND, $\overline{BE}$, SW1, SW0, SIZ1, SIZ0, $\overline{MBF1}$, $\overline{PEFB}$, PGB, VCC, W/$\overline{RB}$, CLKB, ENB, $\overline{CSB}$, FFB

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PQ PACKAGE†
(TOP VIEW)

Top pins (left to right, pins 17 down to 1, then 132 down to 117):

Pin	Signal
17	$\overline{AFA}$
16	$\overline{FFA}$
15	$\overline{CSA}$
14	$\overline{ENA}$
13	CLKA
12	W/$\overline{RA}$
11	V_{CC}
10	PGA
9	$\overline{PEFA}$
8	GND
7	$\overline{MBF2}$
6	MBA
5	FS1
4	FS0
3	ODD/$\overline{EVEN}$
2	$\overline{RST}$
1	GND
132	$\overline{BE}$
131	SW1
130	SW0
129	SIZ1
128	SIZ0
127	$\overline{MBF1}$
126	GND
125	$\overline{PEFB}$
124	PGB
123	V_{CC}
122	W/$\overline{RB}$
121	CLKB
120	$\overline{ENB}$
119	$\overline{CSB}$
118	$\overline{FFB}$
117	$\overline{AFB}$

Left side pins (top to bottom):

Pin	Signal
18	GND
19	$\overline{AEA}$
20	EFA
21	A0
22	A1
23	A2
24	GND
25	A3
26	A4
27	A5
28	A6
29	V_{CC}
30	A7
31	A8
32	A9
33	GND
34	A10
35	A11
36	V_{CC}
37	A12
38	A13
39	A14
40	GND
41	A15
42	A16
43	A17
44	A18
45	A19
46	A20
47	GND
48	A21
49	A22
50	A23

Right side pins (top to bottom):

Pin	Signal
116	GND
115	$\overline{AEB}$
114	EFB
113	B0
112	B1
111	B2
110	GND
109	B3
108	B4
107	B5
106	B6
105	V_{CC}
104	B7
103	B8
102	B9
101	GND
100	B10
99	B11
98	V_{CC}
97	B12
96	B13
95	B14
94	GND
93	B15
92	B16
91	B17
90	B18
89	B19
88	B20
87	GND
86	B21
85	B22
84	B23

Bottom pins (left to right, pins 51 to 83):

Pin	Signal
51	V_{CC}
52	A24
53	A25
54	A26
55	GND
56	A27
57	A28
58	A29
59	V_{CC}
60	A30
61	A31
62	A32
63	GND
64	A33
65	A34
66	A35
67	GND
68	B35
69	B34
70	B33
71	GND
72	B32
73	B31
74	B30
75	V_{CC}
76	B29
77	B28
78	B27
79	GND
80	B26
81	B25
82	B24
83	V_{CC}

NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

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functional block diagram

CLKA
CSA
W/RA
ENA
MBA

Port-A Control Logic

MBF1
PEFB

Mail1 Register

Parity Gen/Check

PGB

Input Register

64 × 36 SRAM

Parity Generation

Bus Matching and Byte Swapping

Output Register

36

RST

ODD/EVEN

Device Control

Write Pointer

Read Pointer

FFA
AFA

Status-Flag Logic

FIFO1

EFB
AEB

36

FS0
FS1
A0 – A35

Programmable-Flag Offset Register

B0 – B35

FIFO2

EFA
AEA

Status-Flag Logic

FFB
AFB

Read Pointer

Write Pointer

36

Output Register

Parity Generation

64 × 36 SRAM

Bus Matching and Byte Swapping

Input Register

PGA

Mail2 Register

Parity Gen/Check

PEFA

MBF2

Port-B Control Logic

CLKB
CSB
W/RB
ENB
BE
SIZ0
SIZ1
SW0
SW1

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Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AEA}$	O (port A)	Port-A almost-empty flag. Programmable flag synchronized to CLKA. $\overline{AEA}$ is low when the number of 36-bit words in FIFO2 is less than or equal to the value in offset register X.
$\overline{AEB}$	O (port B)	Port-B almost-empty flag. Programmable flag synchronized to CLKB. $\overline{AEB}$ is low when the number of 36-bit words in FIFO1 is less than or equal to the value in offset register X.
$\overline{AFA}$	O (port A)	Port-A almost-full flag. Programmable flag synchronized to CLKA. $\overline{AFA}$ is low when the number of 36-bit empty locations in FIFO1 is less than or equal to the value in offset register X.
$\overline{AFB}$	O (port B)	Port-B almost-full flag. Programmable flag synchronized to CLKB. $\overline{AFB}$ is low when the number of 36-bit empty locations in FIFO2 is less than or equal to the value in offset register X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
$\overline{BE}$	I	Big-endian select. Selects the bytes on port B used during byte or word data transfer. A low on $\overline{BE}$ selects the most-significant bytes on B0–B35 for use, and a high selects the least-significant bytes.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data-port-sizing operations are also synchronous to the low-to-high transition of CLKB. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
$\overline{EFA}$	O (port A)	Port-A empty flag. $\overline{EFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{EFA}$ is low, FIFO2 is empty and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is high. $\overline{EFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	O (port B)	Port-B empty flag. $\overline{EFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EFB}$ is low, FIFO1 is empty and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is high. $\overline{EFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{FFA}$	O (port A)	Port-A full flag. $\overline{FFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FFA}$ is low, FIFO1 is full and writes to its memory are disabled. $\overline{FFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
$\overline{FFB}$	O (port B)	Port-B full flag. $\overline{FFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{FFB}$ is low, FIFO2 is full and writes to its memory are disabled. $\overline{FFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after reset.
FS1, FS0	I	Flag offset selects. The low-to-high transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the $\overline{AE}$ flag and $\overline{AF}$ flag offset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and both SIZ1 and SIZ0 are high. $\overline{MBF1}$ is set high when the device is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high when the device is reset.

TEXAS INSTRUMENTS

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
ODD/$\overline{\text{EVEN}}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{\text{EVEN}}$ is high and even parity is checked when ODD/$\overline{\text{EVEN}}$ is low. ODD/$\overline{\text{EVEN}}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{\text{PEFA}}$	O (port A)	Port-A parity-error flag. When any byte applied to terminals A0–A35 fails parity, $\overline{\text{PEFA}}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most-significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA; therefore, if a mail2 read with parity generation is set up by having W/$\overline{\text{RA}}$ low, MBA high, and PGA high, the $\overline{\text{PEFA}}$ flag is forced high, regardless of the state of the A0–A35 inputs.
$\overline{\text{PEFB}}$	O (port B)	Port-B parity-error flag. When any valid byte applied to terminals B0–B35 fails parity, $\overline{\text{PEFB}}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most-significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB; therefore, if a mail1 read with parity generation is set up by having W/$\overline{\text{RB}}$ low, SIZ1 and SIZ0 high, and PGB high, the $\overline{\text{PEFB}}$ flag is forced high, regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most-significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most-significant bit of each byte.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. This sets the $\overline{\text{AFA}}$, $\overline{\text{AFB}}$, $\overline{\text{MBF1}}$, and $\overline{\text{MBF2}}$ flags high and the $\overline{\text{EFA}}$, $\overline{\text{EFB}}$, $\overline{\text{AEA}}$, $\overline{\text{AEB}}$, $\overline{\text{FFA}}$, and $\overline{\text{FFB}}$ flags low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of the FS1 and FS0 inputs to select $\overline{\text{AF}}$ flag and $\overline{\text{AE}}$ flag offset.
SIZ0, SIZ1	I (port B)	Port-B bus-size selects. The low-to-high transition of CLKB latches the states of SIZ0, SIZ1, and $\overline{\text{BE}}$, and the following low-to-high transition of CLKB implements the latched states as a port-B bus size. Port-B bus sizes can be long word, word, or byte. A high on both SIZ0 and SIZ1 accesses the mailbox registers for a port-B 36-bit write or read.
SW0, SW1	I (port B)	Port-B byte-swap selects. At the beginning of each long word transfer, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/$\overline{\text{RA}}$	I	Port-A write/read select. W/$\overline{\text{RA}}$ high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
W/$\overline{\text{RB}}$	I	Port-B write/read select. W/$\overline{\text{RB}}$ high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{\text{RB}}$ is high.

detailed description

reset

The SN74ABT3614 is reset by taking the reset ($\overline{\text{RST}}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags ($\overline{\text{FFA}}$, $\overline{\text{FFB}}$) low, the empty flags ($\overline{\text{EFA}}$, $\overline{\text{EFB}}$) low, the almost-empty flags ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) low, and the almost-full flags ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) high. A reset also forces the mailbox flags ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) high. After a reset, $\overline{\text{FFA}}$ is set high after two low-to-high transitions of CLKA and $\overline{\text{FFB}}$ is set high after two low-to-high transitions of CLKB. The device must be reset after power up before data is written to its memory.

A low-to-high transition on $\overline{\text{RST}}$ loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

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reset (continued)

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	$\overline{\text{AF}}$ AND $\overline{\text{AE}}$ FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{R}}$A). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{R}}$A is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{R}}$A are low. Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is high, ENA is high, MBA is low, and $\overline{\text{FFA}}$ is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is low, ENA is high, MBA is low, and $\overline{\text{EFA}}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{R}}$A	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select (W/$\overline{\text{R}}$B). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ or W/$\overline{\text{R}}$B is high. The B0–B35 outputs are active when both $\overline{\text{CSB}}$ and W/$\overline{\text{R}}$B are low. Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{R}}$B is high, ENB is high, $\overline{\text{FFB}}$ is high, and either SIZ0 or SIZ1 is low. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{R}}$B is low, ENB is high, $\overline{\text{EFB}}$ is high, and either SIZ0 or SIZ1 is low (see Table 3).

The setup- and hold-time constraints to the port clocks for the port-chip selects ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) and write/read selects (W/$\overline{\text{R}}$A, W/$\overline{\text{R}}$B) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port-chip select and write/read select can change states during the setup- and hold-time window of the cycle.

FIFO writer/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{\text{CSB}}$	W/$\overline{\text{RB}}$	ENB	SIZ1, SIZ0	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	One, both low	↑	In high-impedance state	FIFO2 write
L	H	H	Both high	↑	In high-impedance state	Mail2 write
L	L	L	One, both low	X	Active, FIFO1 output register	None
L	L	H	One, both low	↑	Active, FIFO1 output register	FIFO1 read
L	L	L	Both high	X	Active, mail1 register	None
L	L	H	Both high	↑	Active, mail1 register	Mail1 read (set $\overline{\text{MBF1}}$ high)

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another. $\overline{\text{EFA}}$, $\overline{\text{AEA}}$, $\overline{\text{FFA}}$, and $\overline{\text{AFA}}$ are synchronized to CLKA. $\overline{\text{EFB}}$, $\overline{\text{AEB}}$, $\overline{\text{FFB}}$, and $\overline{\text{AFB}}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF 36-BIT WORDS IN FIFO1†	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{\text{EFB}}$	$\overline{\text{AEB}}$	$\overline{\text{AFA}}$	$\overline{\text{FFA}}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 − (X + 1)]	H	H	H	H
(64 − X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the $\overline{\text{AE}}$ flag and $\overline{\text{AF}}$ flag offset register.

Table 5. FIFO2 Flag Operation

NUMBER OF 36-BIT WORDS IN FIFO2†	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	$\overline{\text{EFA}}$	$\overline{\text{AEA}}$	$\overline{\text{AFB}}$	$\overline{\text{FFB}}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 − (X + 1)]	H	H	H	H
(64 − X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the $\overline{\text{AE}}$ flag and $\overline{\text{AF}}$ flag offset register.

empty flags ($\overline{\text{EFA}}$, $\overline{\text{EFB}}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array. When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored. When reading FIFO1 with a byte or word size on port B, $\overline{\text{EFB}}$ is set low when the fourth byte or second word of the last long word is read.

The FIFO read pointer is incremented each time a new word is clocked to the output register. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty-flag synchronizing clock; therefore, an empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The FIFO empty flag is set high by the second low-to-high transition of the synchronizing clock and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on an empty-flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1}, or greater, after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 13 and 14).

full flags ($\overline{\text{FFA}}$, $\overline{\text{FFB}}$)

The FIFO full flag is synchronized to the port clock that writes data to its array. When the full flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full-flag synchronizing clock. A full flag is low if less than two cycles of the full-flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the full-flag synchronizing clock after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on a full-flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1}, or greater, after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 15 and 16).

almost-empty flags ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$)

The FIFO almost-empty flag is synchronized to the port clock that reads data from its array. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). An $\overline{\text{AE}}$ flag is low when the FIFO contains X or fewer long words in memory and is high when the FIFO contains (X + 1) or more long words.

Two low-to-high transitions of the $\overline{\text{AE}}$-flag synchronizing clock are required after a FIFO write for the $\overline{\text{AE}}$ flag to reflect the new level of fill; therefore, the $\overline{\text{AE}}$ flag of a FIFO containing (X + 1) or more long words remains low if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An $\overline{\text{AE}}$ flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an $\overline{\text{AE}}$ flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2}, or greater, after the write that fills the FIFO to (X + 1) long words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 17 and 18).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). An almost-full flag is low when the FIFO contains (64 – X) or more long words in memory and is high when the FIFO contains [64 – (X + 1)] or fewer long words.

Two low-to-high transitions of the $\overline{AF}$-flag synchronizing clock are required after a FIFO read for the $\overline{AF}$ flag to reflect the new level of fill; therefore, the $\overline{AF}$ flag of a FIFO containing [64 – (X + 1)] or fewer words remains low if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of long words in memory to [64 – (X + 1)]. An $\overline{AF}$ flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO read that reduces the number of long words in memory to [64 – (X + 1)]. A low-to-high transition of an $\overline{AF}$-flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2}, or greater, after the read that reduces the number of long words in memory to [64 – (X + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 19 and 20).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data-transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA, and MBA is high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and both SIZ0 and SIZ1 are high. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When the port-A data outputs (A0–A35) are active, the data on the bus comes from the FIFO2 output register when MBA is low and from the mail2 register when MBA is high. When the port-B data outputs (B0–B35) are active, the data on the bus comes from the FIFO1 output register when either one or both SIZ1 and SIZ0 are low and from the mail2 register when both SIZ1 and SIZ0 are high. The mail1 register flag ($\overline{MBF1}$) is set high by a rising CLKB edge when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and both SIZ1 and SIZ0 are high. The mail2 register flag ($\overline{MBF2}$) is set high by a rising CLKA edge when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is high. The data in the mail register remains intact after it is read and changes only when new data is written to the register.

dynamic bus sizing

The port-B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from FIFO1 or written to FIFO2. Word- and byte-size bus selections can utilize the most-significant bytes of the bus (big endian) or least-significant bytes of the bus (little endian). Port-B bus size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port-B bus-size select (SIZ0, SIZ1) inputs and the big-endian select ($\overline{BE}$) input are stored on each CLKB low-to-high transition. The stored port-B bus-size selection is implemented by the next rising edge on CLKB according to Figure 1.

Only 36-bit long-word data is written to or read from the two FIFO memories on the SN74ABT3614. Bus-matching operations are done after data is read from the FIFO1 RAM and before data is written to the FIFO2 RAM. Port-B bus sizing does not apply to mail-register operations.

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dynamic bus sizing (continued)

BYTE ORDER ON PORT A:

| A35 | A27 | A26 | A18 | A17 | A9 | A8 | A0 |

| A | B | C | D | Write to FIFO1/Read From FIFO2 |

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

$\overline{BE}$	SIZ1	SIZ0
X	L	L

| A | B | C | D | Read From FIFO1/Write to FIFO2 |

(a) LONG WORD SIZE

$\overline{BE}$	SIZ1	SIZ0
L	L	H

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| A | B | | | 1st: Read From FIFO1/Write to FIFO2 |

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| C | D | | | 2nd: Read From FIFO1/Write to FIFO2 |

(b) WORD SIZE – BIG ENDIAN

$\overline{BE}$	SIZ1	SIZ0
H	L	H

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| | | C | D | 1st: Read From FIFO1/Write to FIFO2 |

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| | | A | B | 2nd: Read From FIFO1/Write to FIFO2 |

(c) WORD SIZE – LITTLE ENDIAN

$\overline{BE}$	SIZ1	SIZ0
L	H	L

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| A | | | | 1st: Read From FIFO1/Write to FIFO2 |

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| B | | | | 2nd: Read From FIFO1/Write to FIFO2 |

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| C | | | | 3rd: Read From FIFO1/Write to FIFO2 |

| B35 | B27 | B26 | B18 | B17 | B9 | B8 | B0 |

| D | | | | 4th: Read From FIFO1/Write to FIFO2 |

(d) BYTE SIZE – BIG ENDIAN

Figure 1. Dynamic Bus Sizing

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dynamic bus sizing (continued)

$\overline{BE}$	SIZ1	SIZ0
H	H	L

B35	B27	B26	B18	B17	B9	B8 B0

D   **1st: Read From FIFO1/Write to FIFO2**

C   **2nd: Read From FIFO1/Write to FIFO2**

B   **3rd: Read From FIFO1/Write to FIFO2**

A   **4th: Read From FIFO1/Write to FIFO2**

(e) BYTE SIZE − LITTLE ENDIAN

Figure 1. Dynamic Bus Sizing (continued)

bus-matching FIFO1 reads

Data is read from the FIFO1 RAM in 36-bit long-word increments. If a long-word bus size is implemented, the entire long word immediately shifts to the FIFO1 output register. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO1 output register with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO1 reads with the same bus-size implementation output the rest of the long word to the FIFO1 output register in the order shown by Figure 1.

Each FIFO1 read with a new bus-size implementation automatically unloads data from the FIFO1 RAM to its output register and auxiliary registers. Therefore, implementing a new port-B bus size and performing a FIFO1 read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread long-word data.

When reading data from FIFO1 in byte or word format, the unused B0−B35 outputs remain inactive but static with the unused FIFO1 output register bits holding the last data value to decrease power consumption.

bus-matching FIFO2 writes

Data is written to the FIFO2 RAM in 36-bit long-word increments. FIFO2 writes with a long-word bus size immediately store each long word in FIFO2 RAM. Data written to FIFO2 with a byte or word bus size stores the initial bytes or words in auxiliary registers. The CLKB rising edge that writes the fourth byte or the second word of long word to FIFO2 also stores the entire long word in FIFO2 RAM. The bytes are arranged in the manner shown in Figure 1.

Each FIFO2 write with a new bus-size implementation resets the state machine that controls the data flow from the auxiliary registers to the FIFO2 RAM. Therefore, implementing a new bus size and performing a FIFO2 write before bytes or words stored in the auxiliary registers have been loaded to FIFO2 RAM results in a loss of data.

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port-B mail-register access

In addition to selecting port-B bus sizes for FIFO reads and writes, the port-B bus size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are high, the mail1 register is accessed for a port-B long-word read and the mail2 register is accessed for a port-B long-word write. The mail register is accessed immediately. Any bus-sizing operation that is underway is unaffected by the mail-register access. After the mail-register access is complete, the previous FIFO access can resume in the next CLKB cycle. The logic diagram in Figure 2 shows that the previous bus-size selection is preserved when the mail registers are accessed from port B. A port-B bus size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{BE}$_Q.
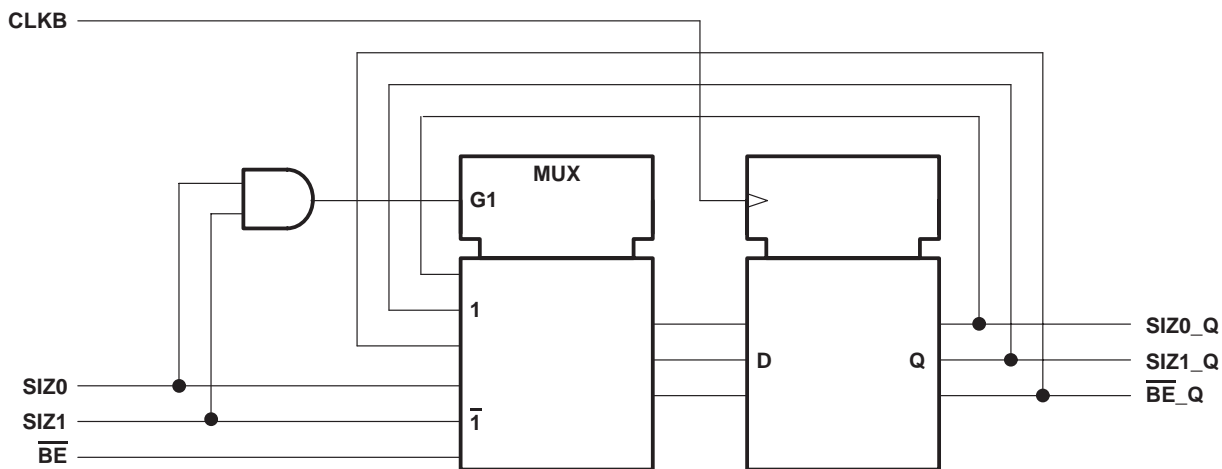
Figure 2. Logic Diagram for SIZ0, SIZ1, and $\overline{BE}$ Register

byte swapping

The byte-order arrangement of data read from FIFO1 or data written to FIFO2 can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail-register data. Four modes of byte-order swapping (including no swap) can be done with any data-port-size selection. The order of the bytes is rearranged within the long word, but the bit order within the bytes remains constant.

Byte arrangement is chosen by the port-B swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from FIFO1 or writes a new long word to FIFO2. The byte order chosen on the first byte or first word of a new long-word read from FIFO1 or written to FIFO2 is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent writes or reads. Figure 3 is an example of the byte-order swapping available for long words. Performing a byte swap and bus size simultaneously for a FIFO1 read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 1. Simultaneous bus-sizing and byte-swapping operations for FIFO2 writes load the data according to Figure 1, then swap the bytes as shown in Figure 3 when the long word is loaded to FIFO2 RAM.

byte swapping (continued)

SW1	SW0
L	L

(a) NO SWAP

SW1	SW0
L	H

(b) BYTE SWAP

SW1	SW0
H	L

(c) WORD SWAP

SW1	SW0
H	H

(d) BYTE-WORD SWAP
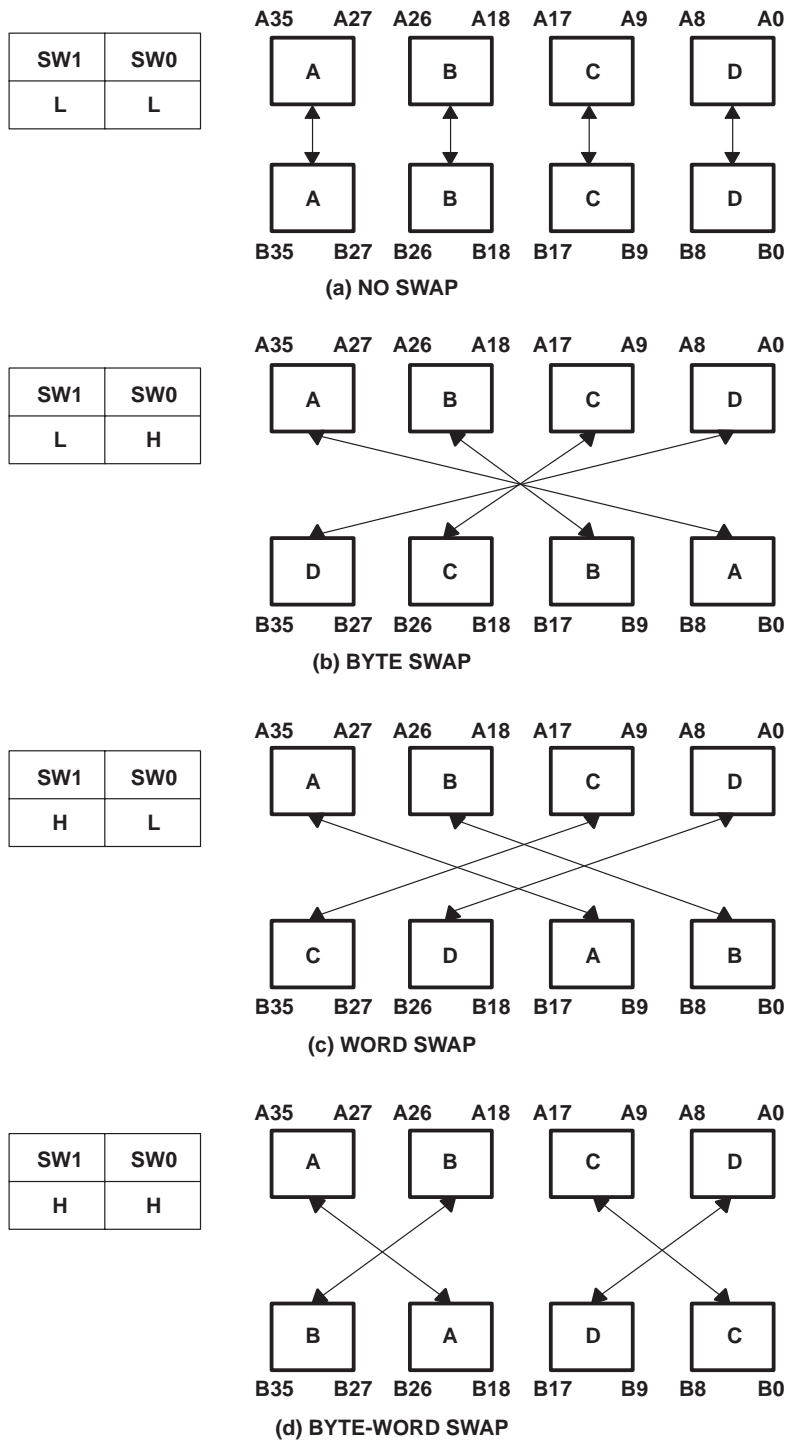
Figure 3. Byte Swapping (Long-Word Size Example)

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parity checking

The port-A data inputs (A0−A35) and port-B data inputs (B0−B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port-A data bus is reported by a low level on the port-A parity error flag ($\overline{PEFA}$). A parity failure on one or more bytes of the port-B data inputs that are valid for the bus-size implementation is reported by a low level on the port-B parity-error flag ($\overline{PEFB}$). Odd- or even-parity checking can be selected, and the parity-error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more valid bytes of a port is reported by a low level on the corresponding port-parity-error flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port-A bytes are arranged as A0−A8, A9−A17, A18−A26, and A27−A35. Port-B bytes are arranged as B0−B8, B9−B17, B18−B26, and B27−B35, and its valid bytes are those used in a port-B bus-size implementation. When odd/even parity is selected, a port parity-error flag ($\overline{PEFA}$, $\overline{PEFB}$) is low if any valid byte on the port has an odd/even number of low levels applied to the bits.

The four parity trees used to check the A0−A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{CSA}$ low, ENA high, W/$\overline{RA}$ low, MBA high, and PGA high, the port-A parity-error flag ($\overline{PEFA}$) is held high, regardless of the levels applied to the A0−A35 inputs. Likewise, the parity trees used to check the B0−B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{CSB}$ low, ENB high, and W/$\overline{RB}$ low, both SIZ0 and SIZ1 high, and PGB high, the port-B parity-error flag ($\overline{PEFB}$) is held high, regardless of the levels applied to the B0−B35 inputs.

parity generation

A high level on the port-A parity-generate select (PGA) or port-B parity-generate select (PGB) enables the SN74ABT3614 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0−A8, A9−A17, A18−A26, and A27−A35, with the most-significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0−B8, B9−B17, B18−B26, and B27−B35, with the most-significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte, regardless of the state of the parity-generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most-significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. The port-A parity-generate select (PGA) and odd/even parity select (ODD/$\overline{EVEN}$) have setup- and hold-time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{EVEN}$ have setup- and hold-time constraints to the port-B clock (CLKB). These timing constraints apply only for a rising clock edge used to read a new long word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0−B35) to check parity. The circuit used to generate parity for the mail2 data is shared by the port-A bus (A0−A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port chip select ($\overline{CSA}$, $\overline{CSB}$) is low, enable (ENA, ENB) is high, write/read select (W/$\overline{RA}$, W/$\overline{RB}$) input is low, the mail register is selected (MBA is high for port A; both SIZ0 and SIZ1 are high for port B), and port parity-generate select (PGA, PGB) is high. Generating parity for mail register data does not change the contents of the register.
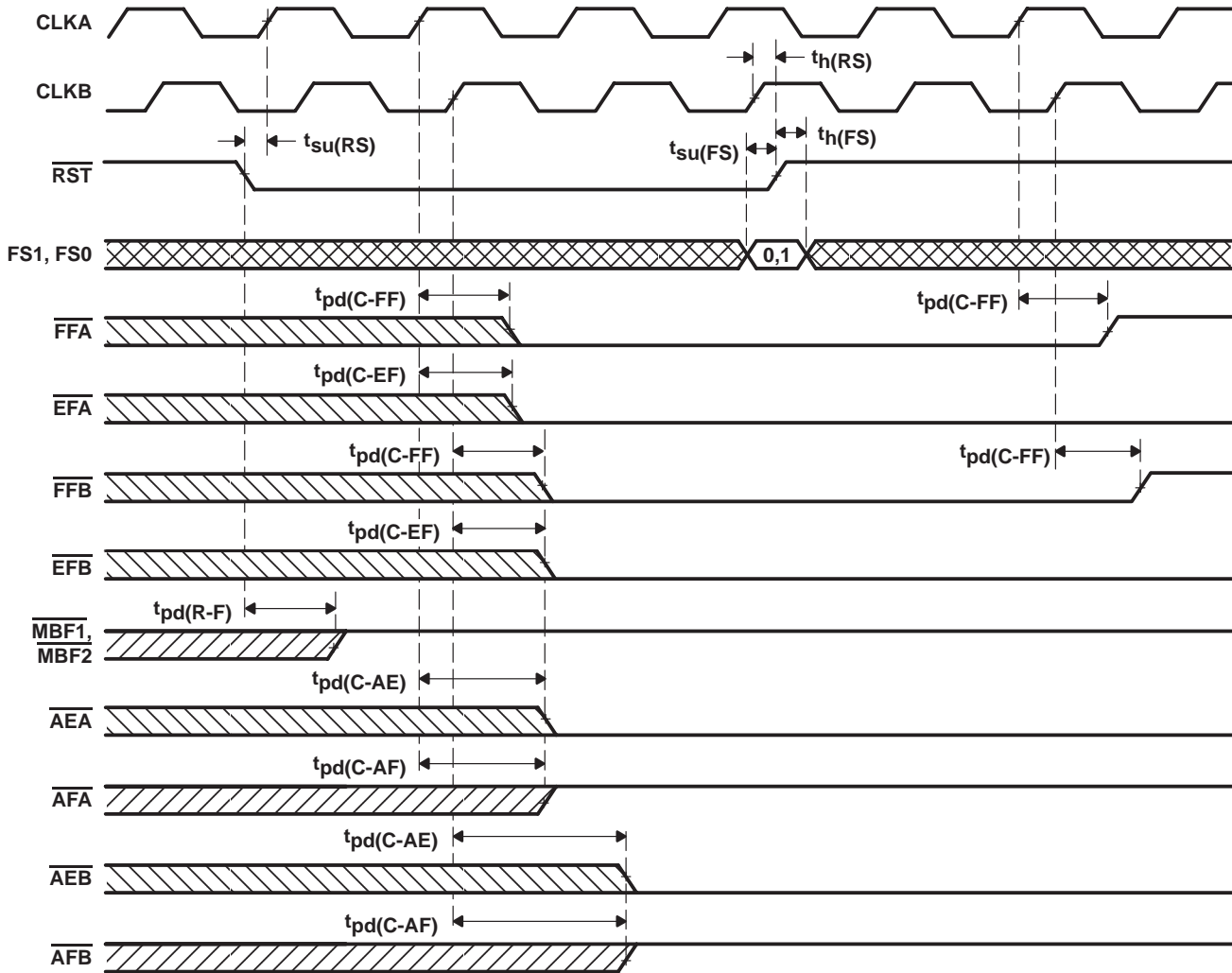
Figure 4. Device Reset Loading the X Register With the Value of Eight
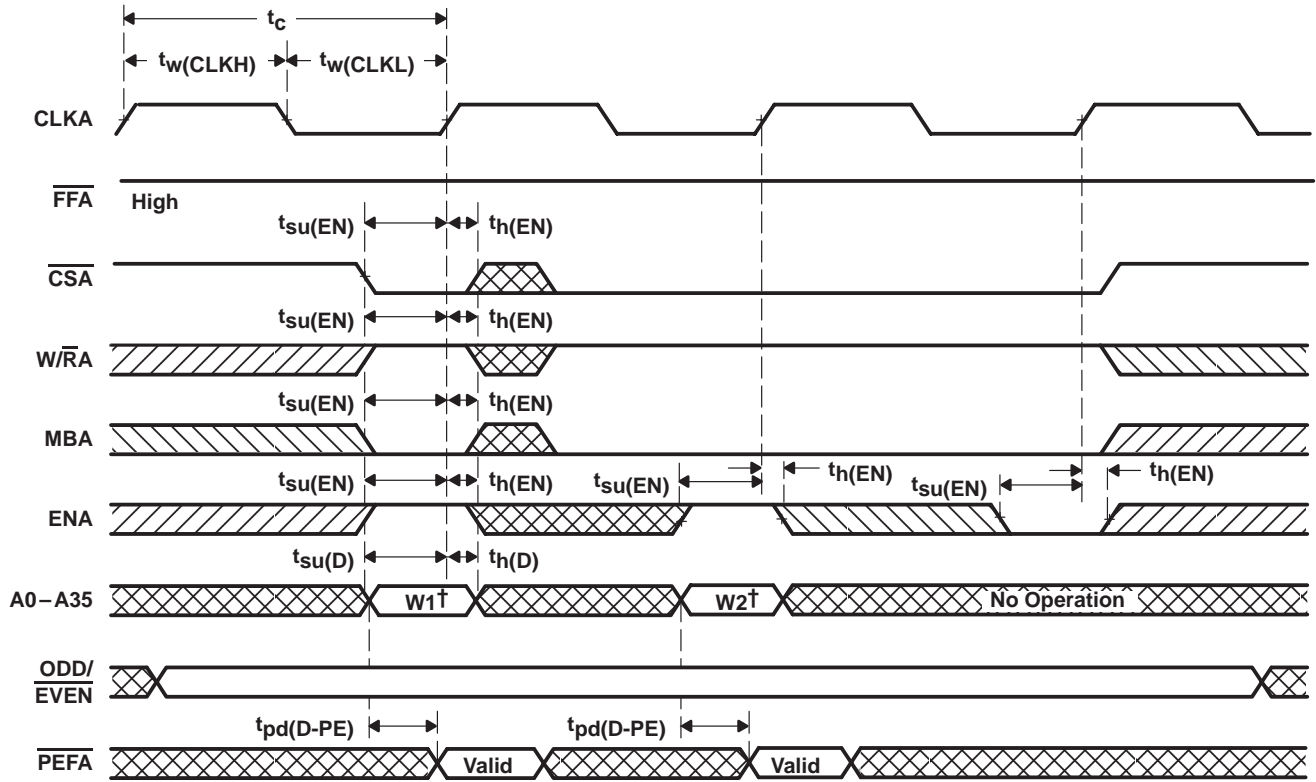
† Written to FIFO1

Figure 5. Port-A Write-Cycle Timing for FIFO1
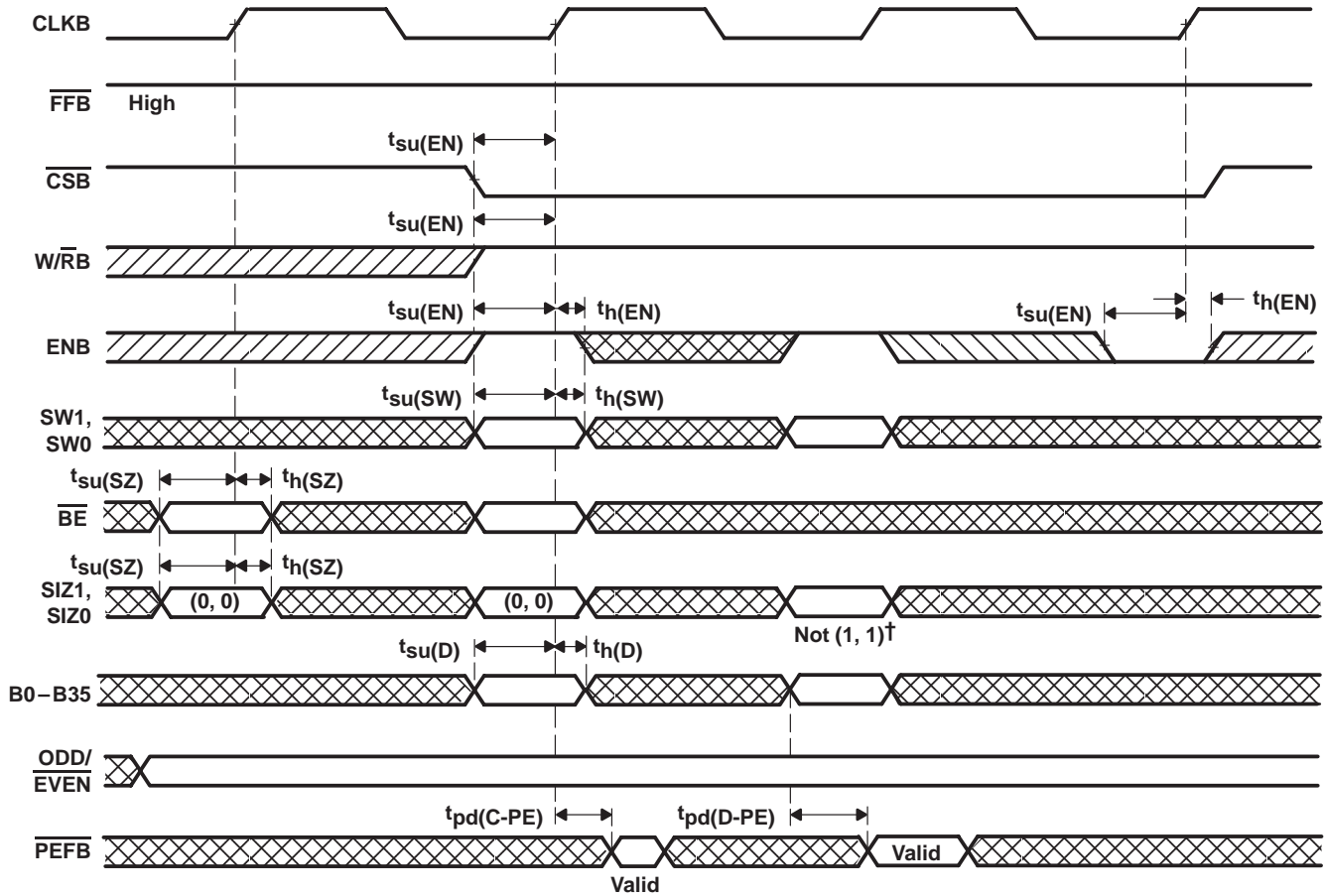
† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

DATA SWAP TABLE FOR LONG-WORD WRITES TO FIFO2

SWAP MODE		DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
SW1	SW0	B35−B27	B26−B18	B17−B9	B8−B0	A35−A27	A26−A18	A17−A9	A8−A0
L	L	A	B	C	D	A	B	C	D
L	H	D	C	B	A	A	B	C	D
H	L	C	D	A	B	A	B	C	D
H	H	B	A	D	C	A	B	C	D

Figure 6. Port-B Long-Word Write-Cycle Timing for FIFO2
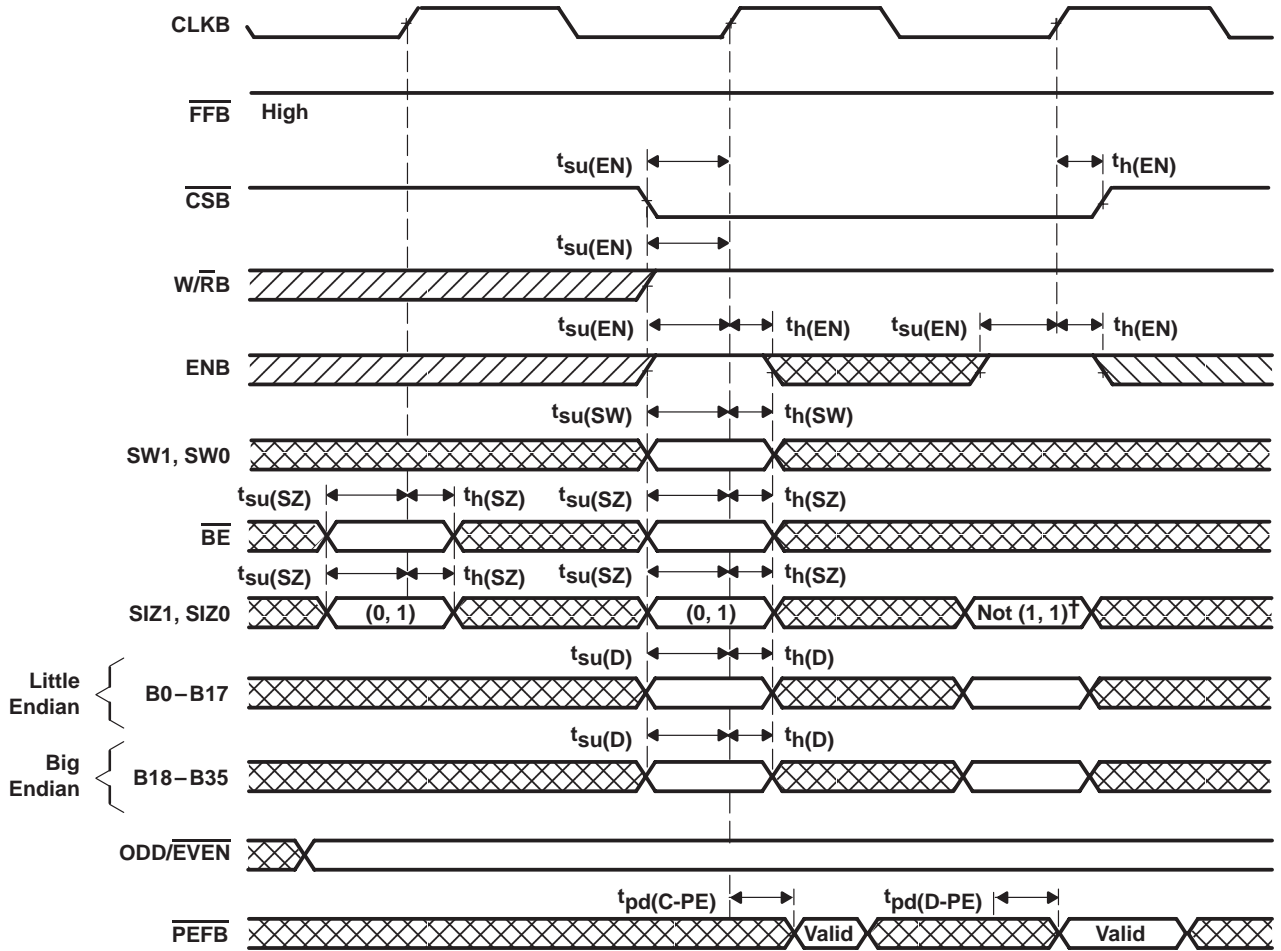
† SIZ0 = H and SIZ1 = H writes data to the mail2 register.
NOTE A: PEFB indicates parity error for the following bytes: B35 – B27 and B26 – B18 for big-endian bus, and B17 – B9 and B8 – B0 for little-endian bus.

DATA SWAP TABLE FOR WORD WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
			BIG ENDIAN		LITTLE ENDIAN					
SW1	SW0		B35 – B27	B26 – B18	B17 – B9	B8 – B0	A35 – A27	A26 – A18	A17 – A9	A8 – A0
L	L	1	A	B	C	D	A	B	C	D
		2	C	D	A	B				
L	H	1	D	C	B	A	A	B	C	D
		2	B	A	D	C				
H	L	1	C	D	A	B	A	B	C	D
		2	A	B	C	D				
H	H	1	B	A	D	C	A	B	C	D
		2	D	C	B	A				

Figure 7. Port-B Word Write-Cycle Timing for FIFO2
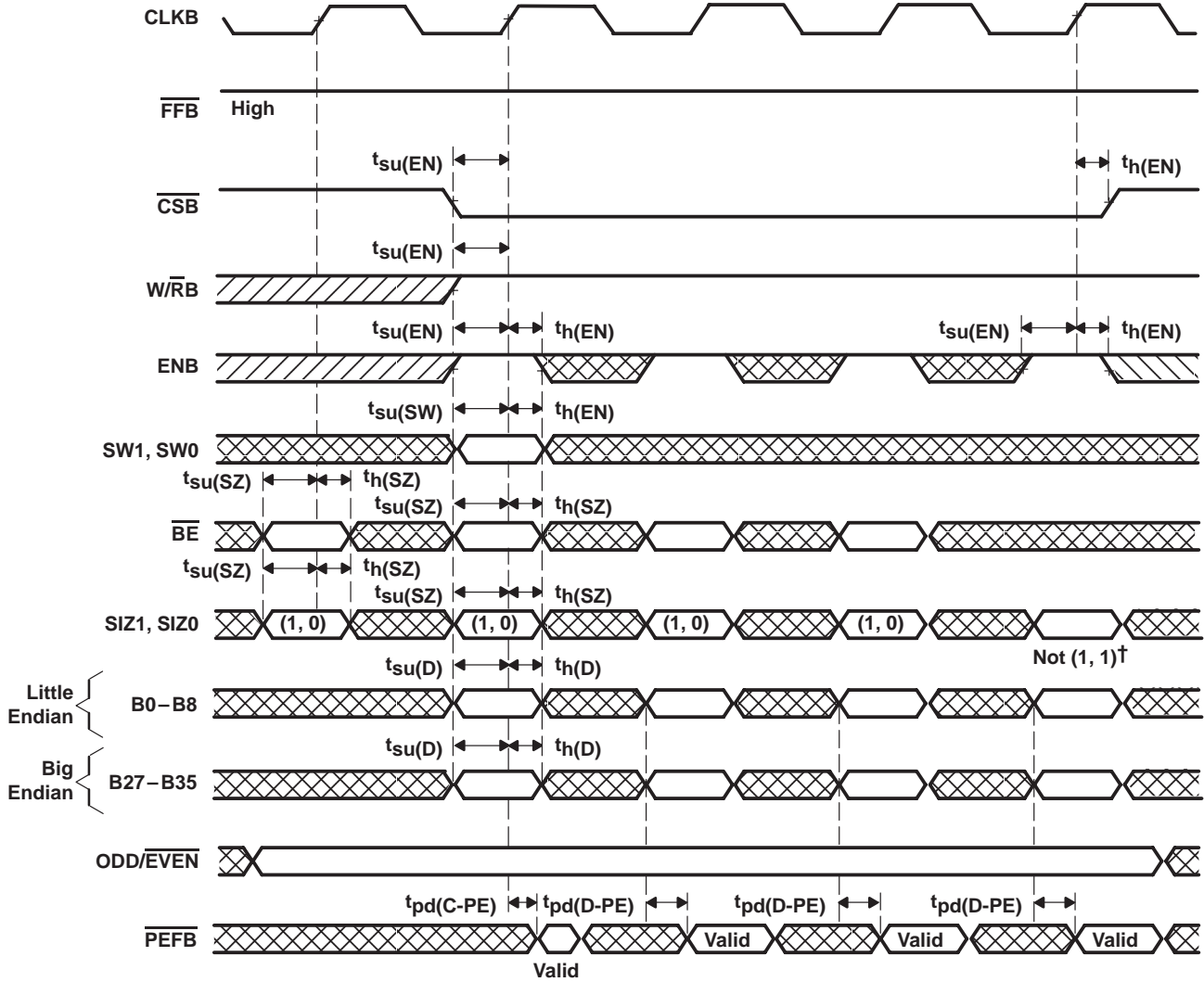
$\dagger$ SIZ0 = H and SIZ1 = H writes data to the mail2 register.

NOTE A: $\overline{PEFB}$ indicates parity error for the following bytes: B35–B27 for big-endian bus and B17–B9 for little-endian bus.

Figure 8. Port-B Byte Write-Cycle Timing for FIFO2

DATA SWAP TABLE FOR BYTE WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
			BIG ENDIAN	LITTLE ENDIAN				
SW1	SW0		B35−B27	B8−B0	A35−A27	A26−A18	A17−A9	A8−A0
L	L	1 2 3 4	A B C D	D C B A	A	B	C	D
L	H	1 2 3 4	D C B A	A B C D	A	B	C	D
H	L	1 2 3 4	C D A B	B A D C	A	B	C	D
H	H	1 2 3 4	B A D C	C D A B	A	B	C	D

Figure 8. Port-B Byte Write-Cycle Timing for FIFO2 (Continued)
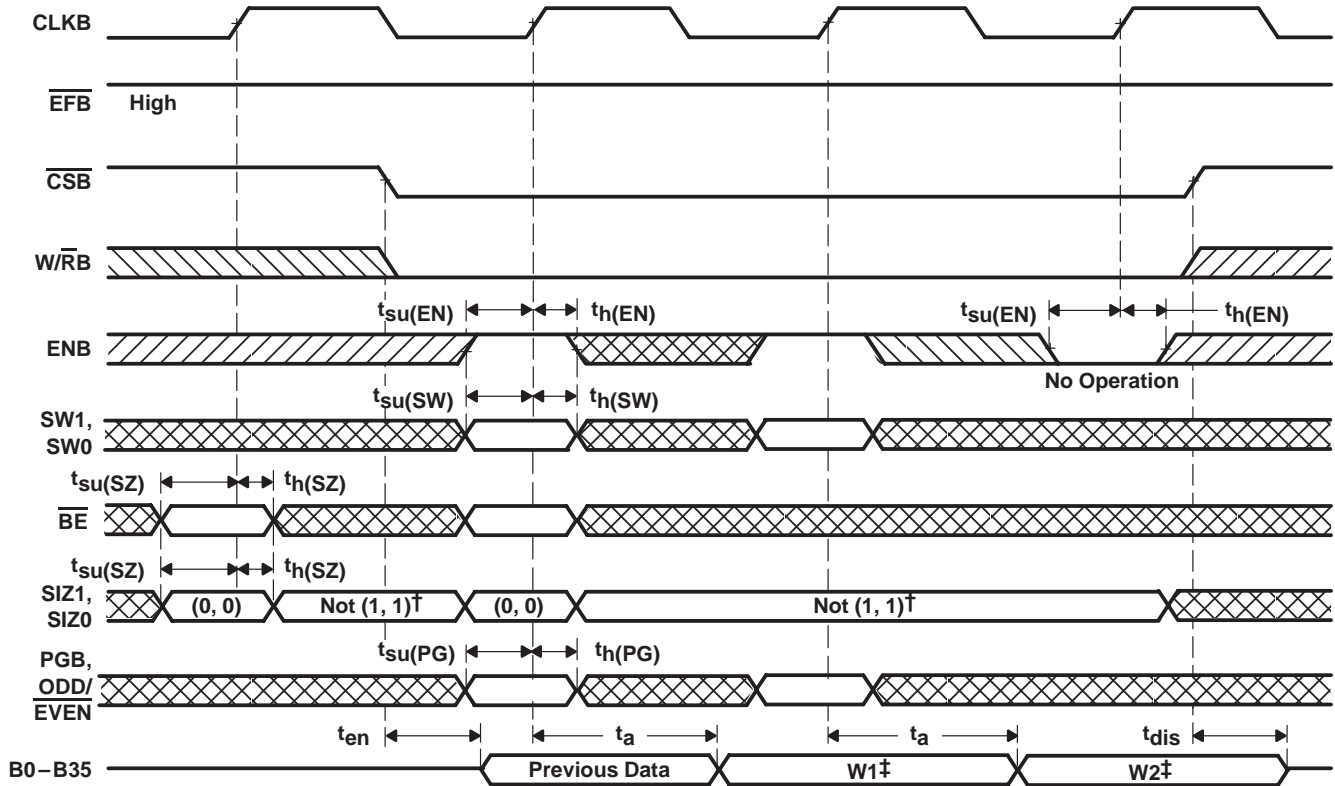
† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Data read from FIFO1

DATA SWAP TABLE FOR LONG-WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		DATA READ FROM FIFO1			
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0	B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 9. Port-B Long-Word Read-Cycle Timing for FIFO1

Timing diagram signals: CLKB, $\overline{\text{EFB}}$ (High), $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, ENB ($t_{su(EN)}$, $t_{h(EN)}$, No Operation), SW1, SW0 ($t_{su(SW)}$, $t_{h(SW)}$), $\overline{\text{BE}}$ ($t_{su(SZ)}$, $t_{h(SZ)}$), SIZ1, SIZ0 ((0, 1), Not (1, 1)†, (0, 1), Not (1, 1)†, $t_{su(SZ)}$, $t_{h(SZ)}$), PGB, ODD/$\overline{\text{EVEN}}$ ($t_{su(PG)}$, $t_{h(PG)}$)

Little Endian‡ B0–B17 (t_{en}, t_a, t_a, t_{dis}): Previous Data, Read 1, Read 2

Big Endian‡ B18–B35 (t_a, t_a, t_{dis}): Previous Data, Read 1, Read 2
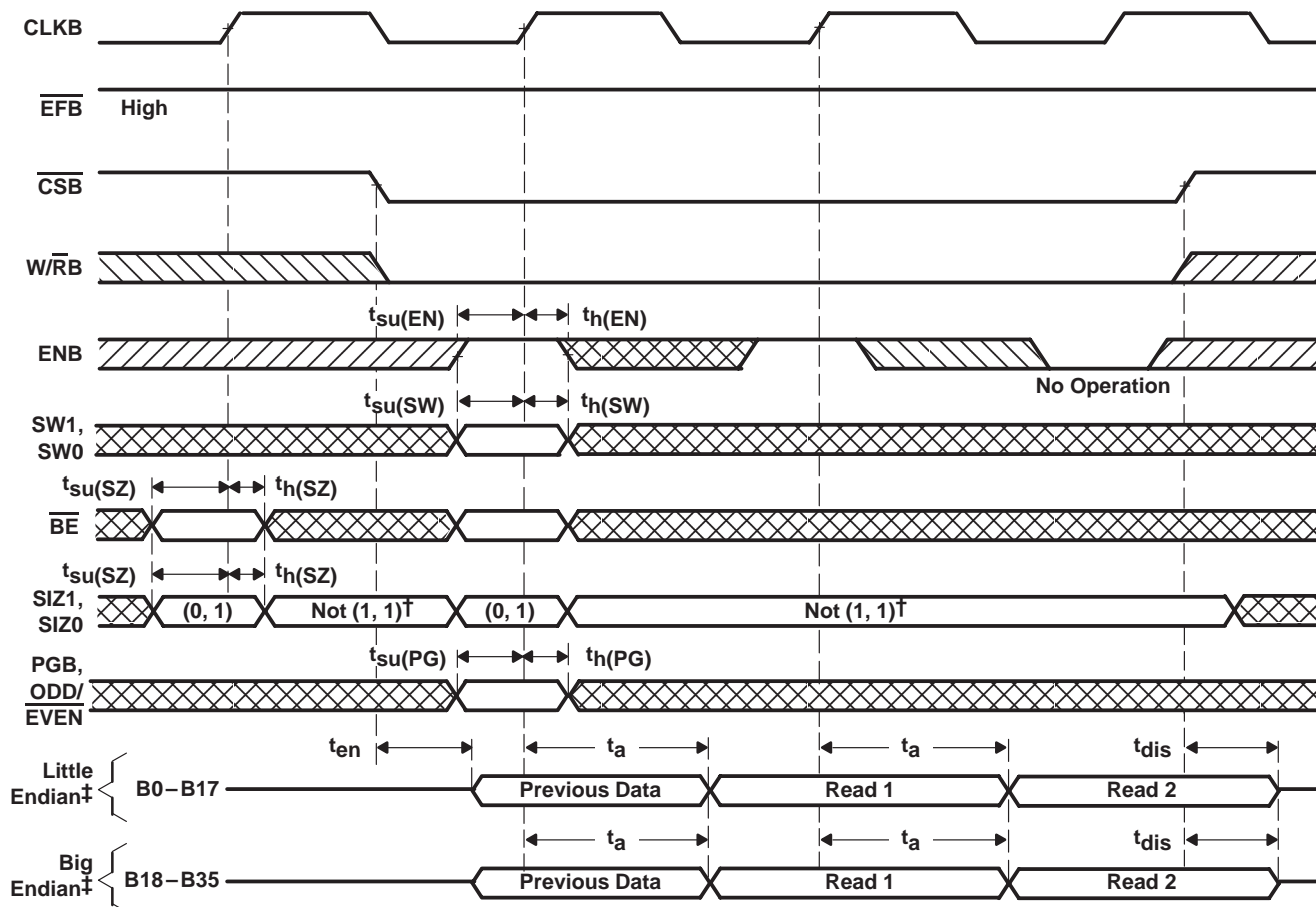
† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Unused word B0–B17 or B18–B35 holds the last FIFO1-output-register data for word-size reads.

DATA SWAP TABLE FOR WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1			
							BIG ENDIAN		LITTLE ENDIAN	
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	1	A	B	C	D
						2	C	D	A	B
A	B	C	D	L	H	1	D	C	B	A
						2	B	A	D	C
A	B	C	D	H	L	1	C	D	A	B
						2	A	B	C	D
A	B	C	D	H	H	1	B	A	D	C
						2	D	C	B	A

Figure 10. Port-B Word Read-Cycle Timing for FIFO1

Figure 11. Port-B Byte Read-Cycle Timing for FIFO1
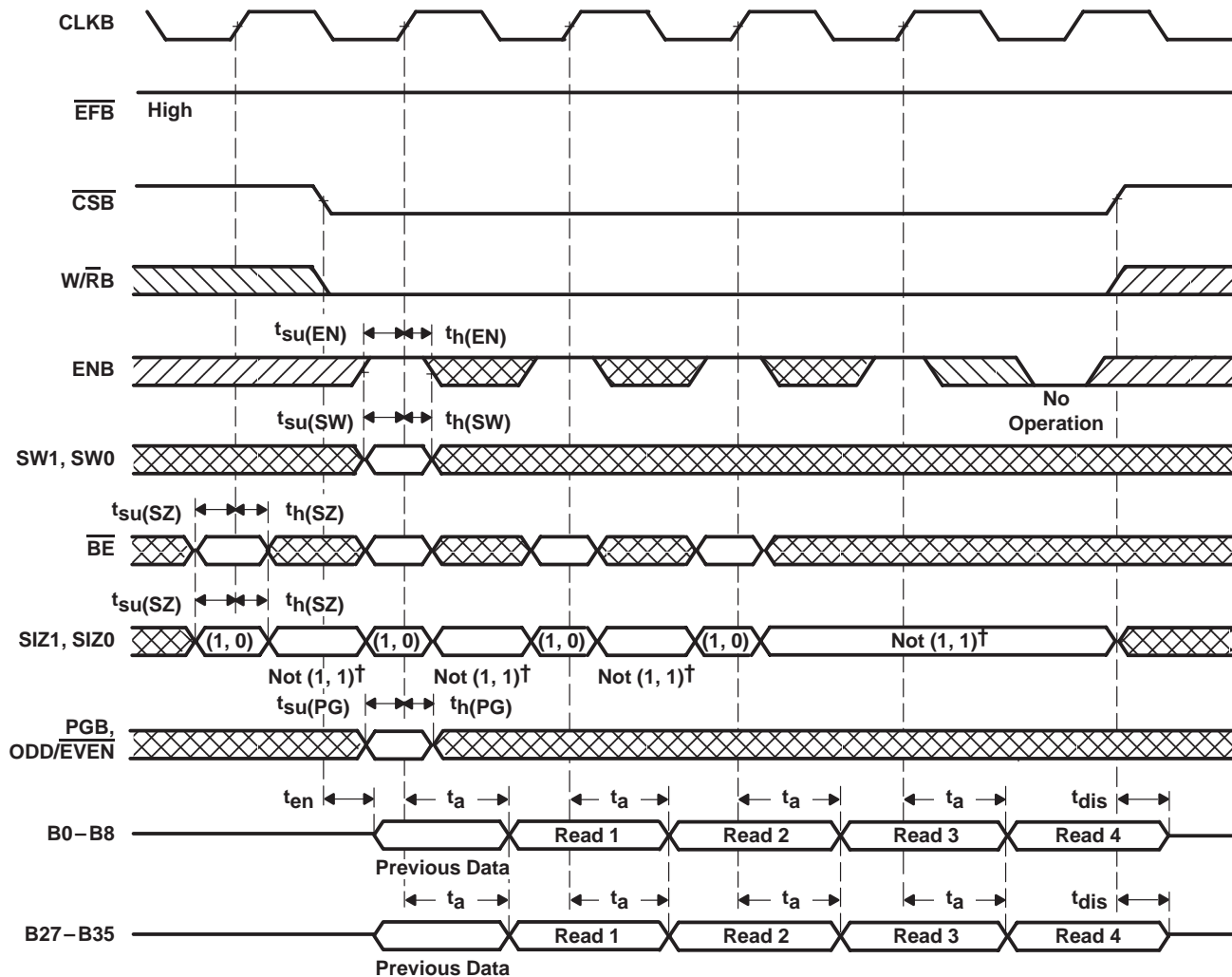
† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.

NOTE A: Unused bytes hold the last FIFO1-output-register data for byte-size reads.

DATA SWAP TABLE FOR BYTE READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1	
							BIG ENDIAN	LITTLE ENDIAN
A35−A27	A26−A18	A17−A9	A8−A0	SW1	SW0		B35−B27	B8−B0
A	B	C	D	L	L	1 2 3 4	A B C D	D C B A
A	B	C	D	L	H	1 2 3 4	D C B A	A B C D
A	B	C	D	H	L	1 2 3 4	C D A B	B A D C
A	B	C	D	H	H	1 2 3 4	B A D C	C D A B

Figure 11. Port-B Byte Read-Cycle Timing for FIFO1 (continued)

† Read from FIFO2
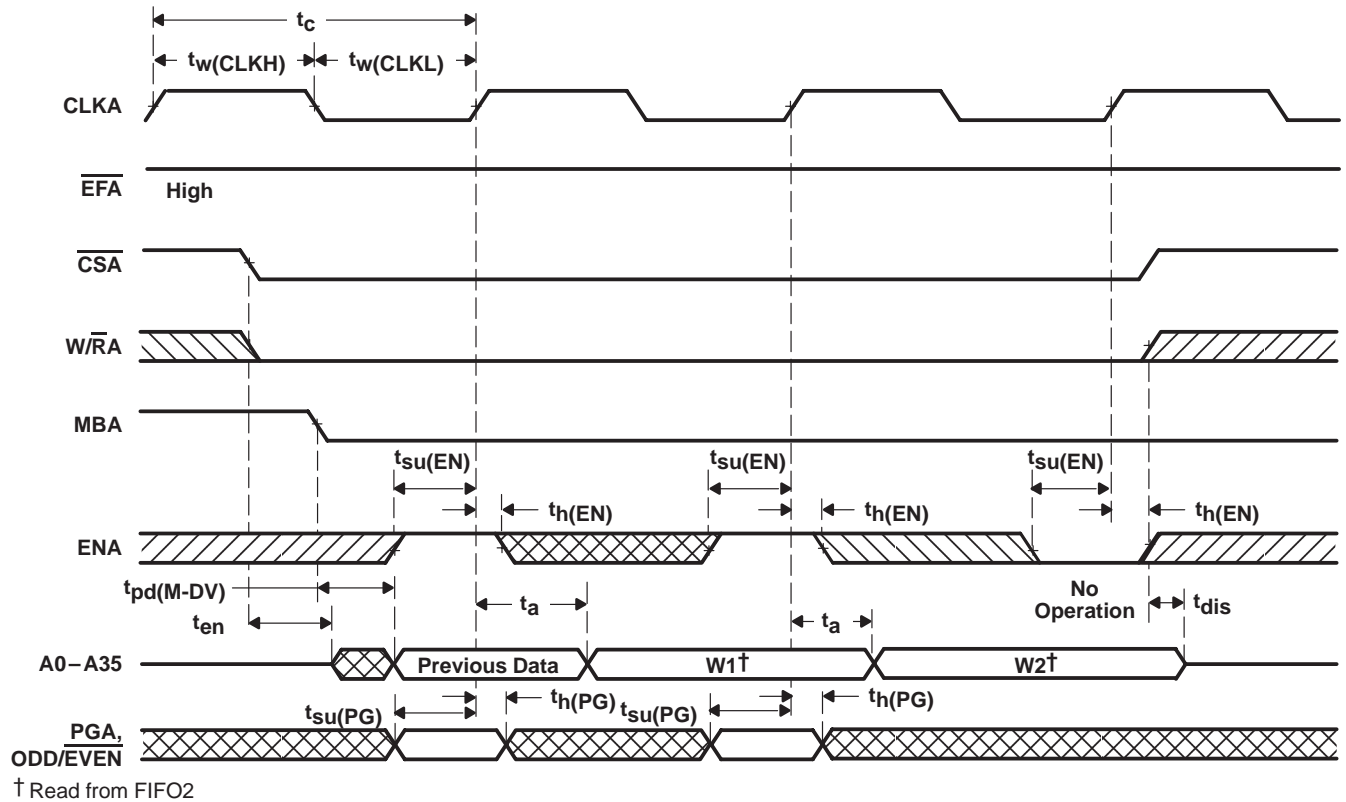
Figure 12. Port-A Read-Cycle Timing for FIFO2
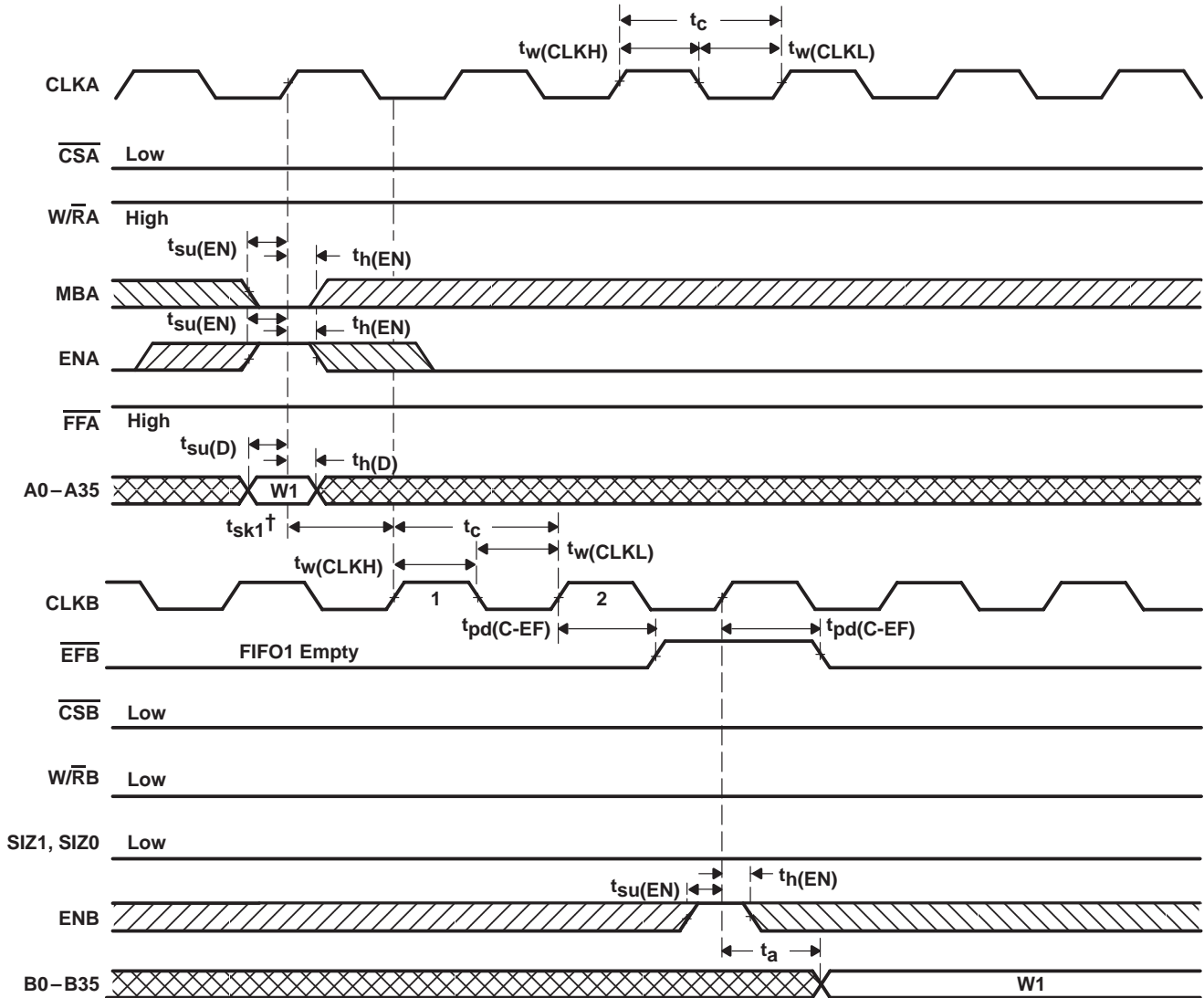
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of $\overline{EFB}$ high may occur one CLKB cycle later than shown.

NOTE A: Port-B size of the long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{EFB}$ is set low by the last word or byte read from FIFO1, respectively.

Figure 13. $\overline{EFB}$-Flag Timing and First Data Read When FIFO1 Is Empty
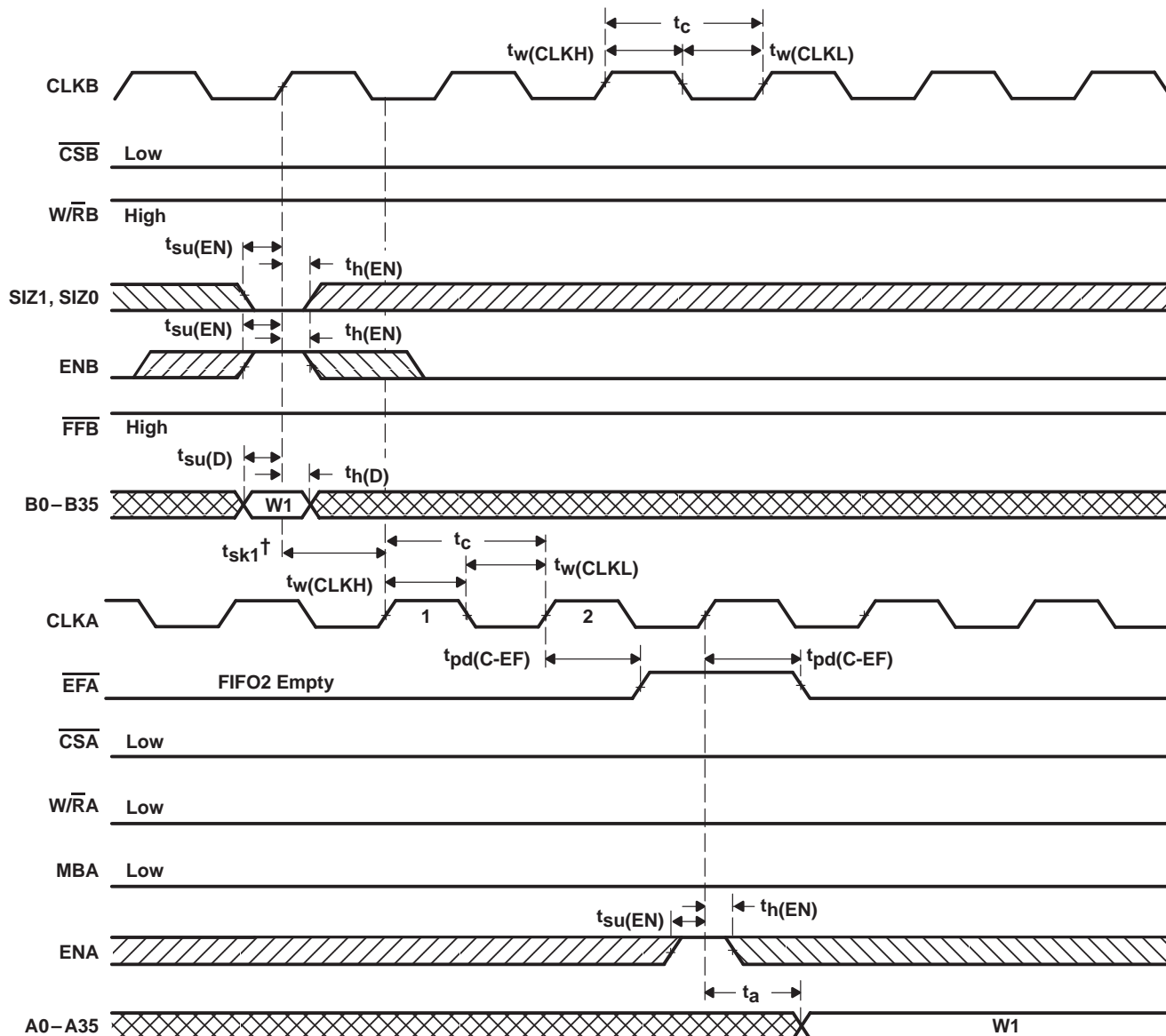
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, the transition of $\overline{EFA}$ high may occur one CLKA cycle later than shown.

NOTE A: Port-B size of the long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

Figure 14. $\overline{EFA}$-Flag Timing and First Data Read When FIFO2 Is Empty
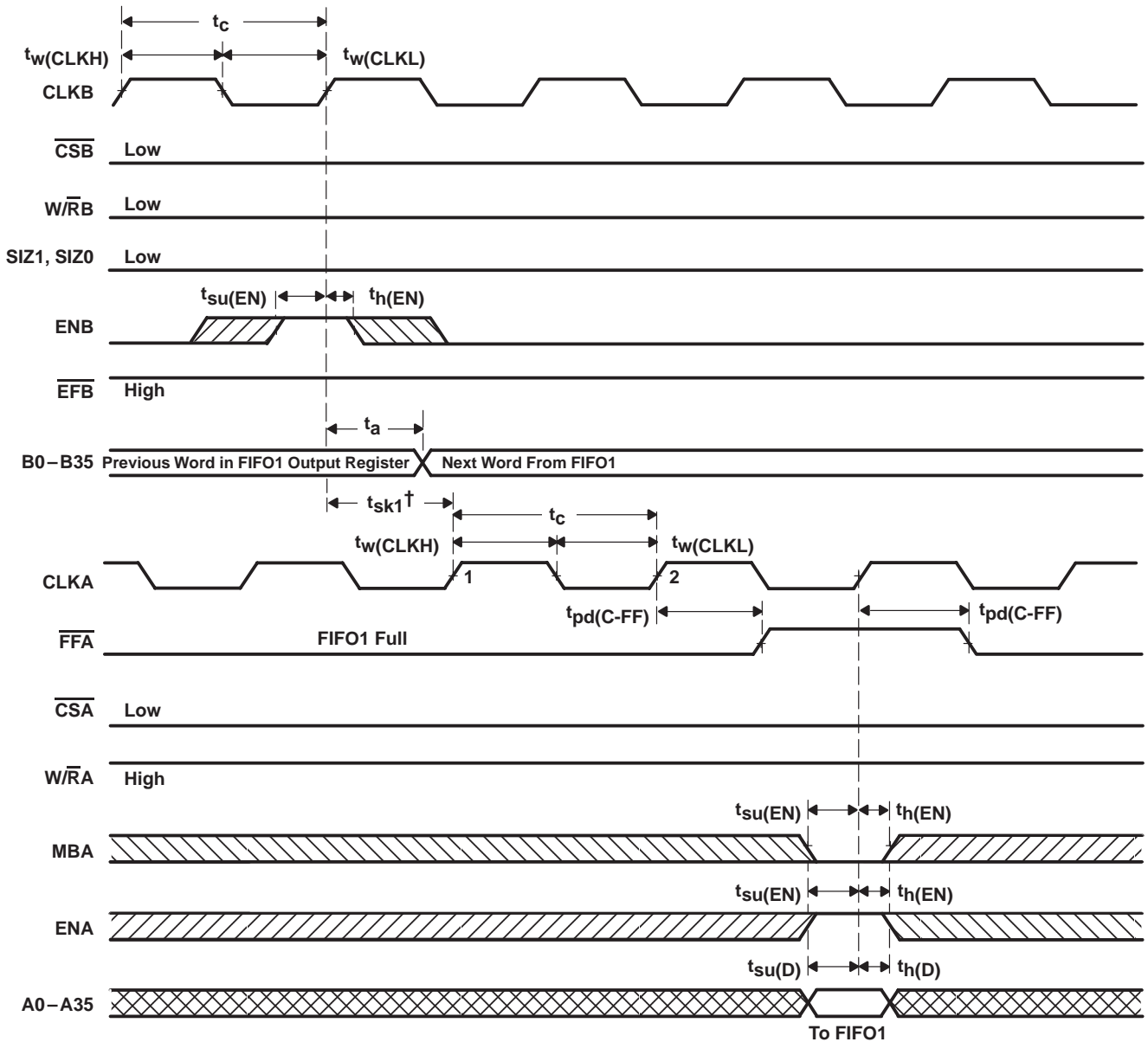
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, $\overline{FFA}$ may transition high one CLKA cycle later than shown.
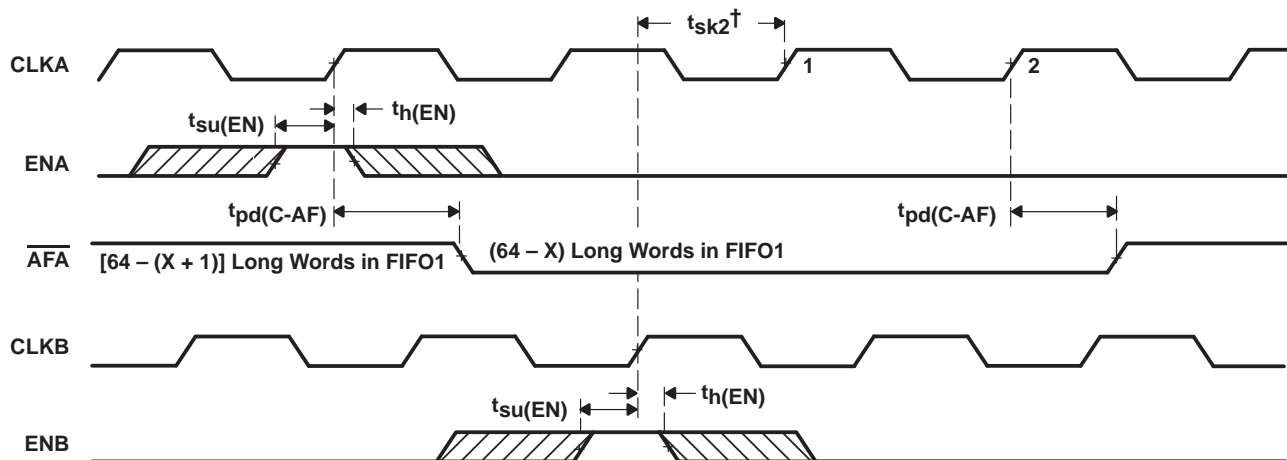
NOTE A: Port-B size of the long word is selected for the FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced from the rising CLKB edge that reads the first word or byte of the long word, respectively.

Figure 15. $\overline{FFA}$-Flag Timing and First Available Write When FIFO1 Is Full
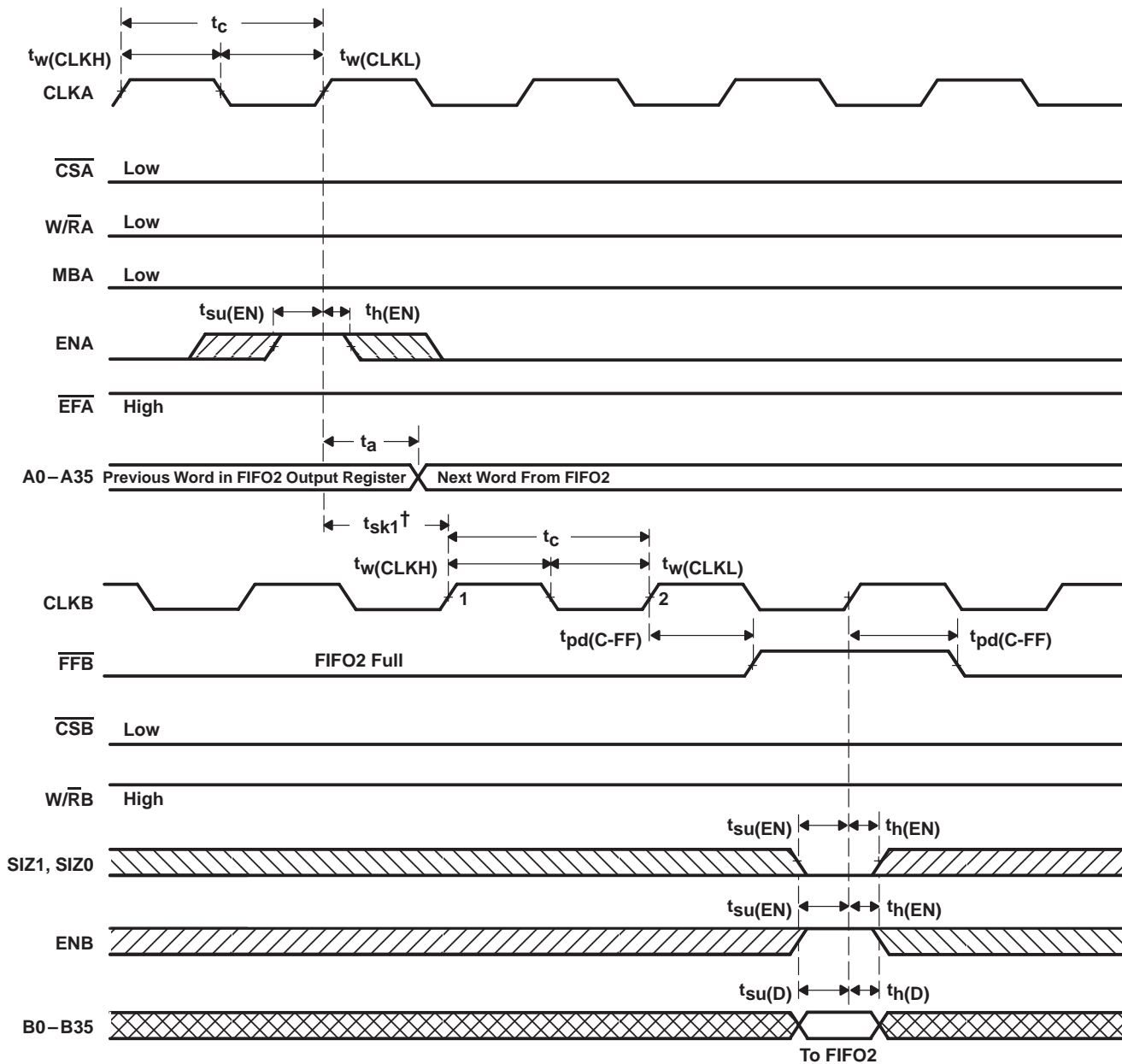
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, $\overline{FFB}$ may transition high one CLKB cycle later than shown.

NOTE A: Port-B size of the long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{FFB}$ is set low by the last word or byte write of the long word, respectively.

Figure 16. $\overline{FFB}$-Flag Timing and First Available Write When FIFO2 Is Full
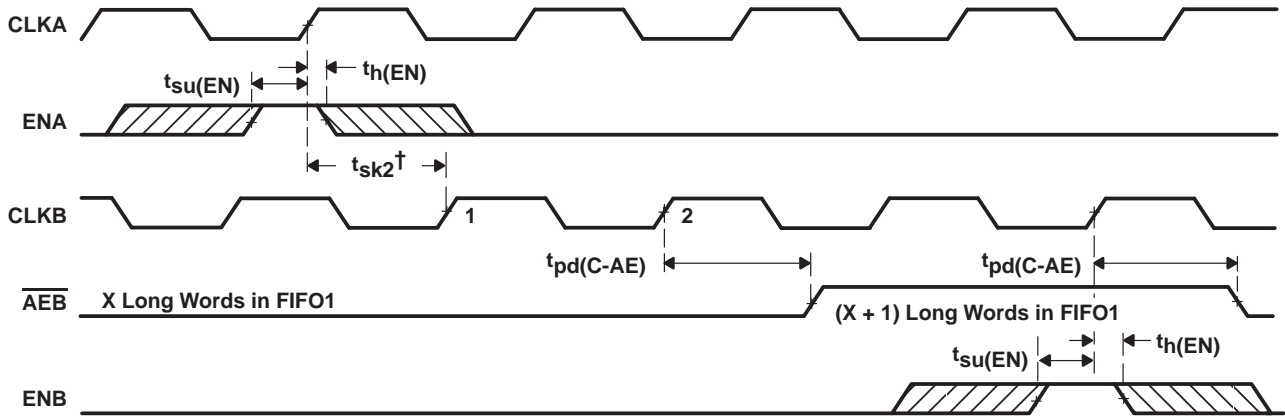
† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L)

B. Port-B size of the long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AEB}$ is set low by the first word or byte read of the long word, respectively.

**Figure 17. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty**
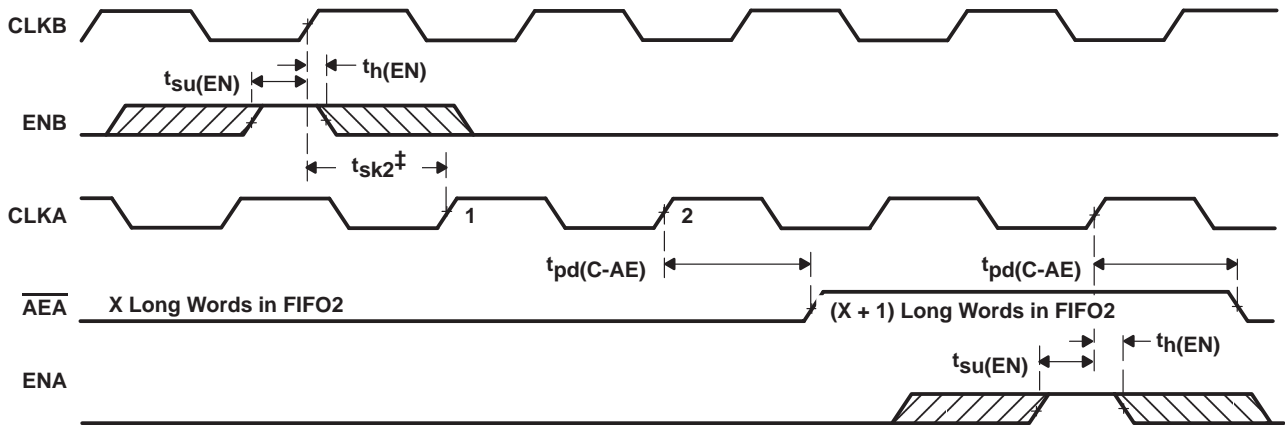
‡ t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTES: A. FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L)

B. Port-B size of the long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the rising CLKB edge that writes the last word or byte of the long word, respectively.

Figure 18. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty

† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L)
        B. Port-B size of the long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the first word or byte read of the long word, respectively.

Figure 19. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full
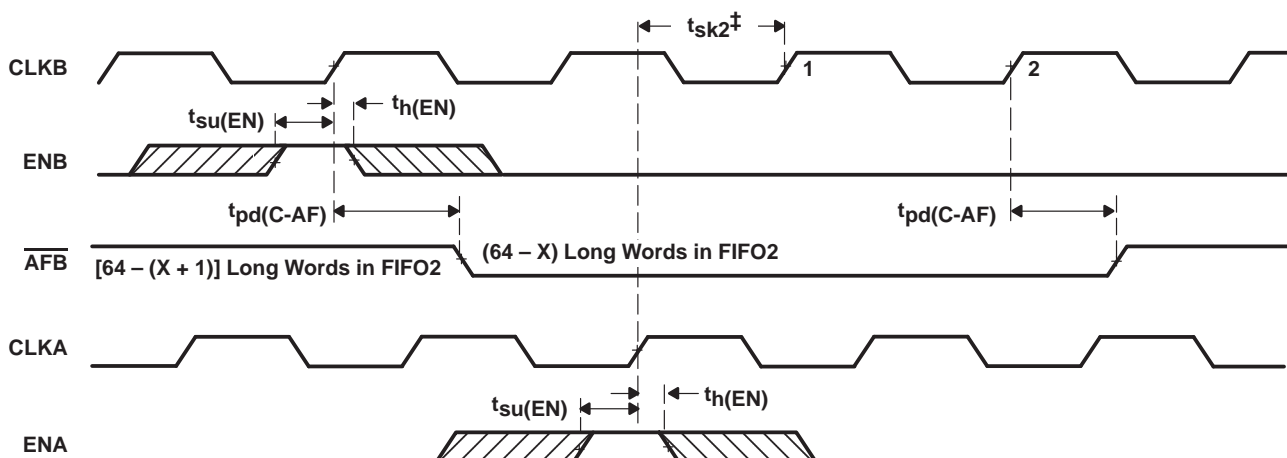
‡ t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AFB}$ may transition high one CLKA cycle later than shown.

NOTES: A. FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$= H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L)
        B. Port-B size of the long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AFB}$ is set low by the last word or byte write of the long word, respectively.

Figure 20. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full
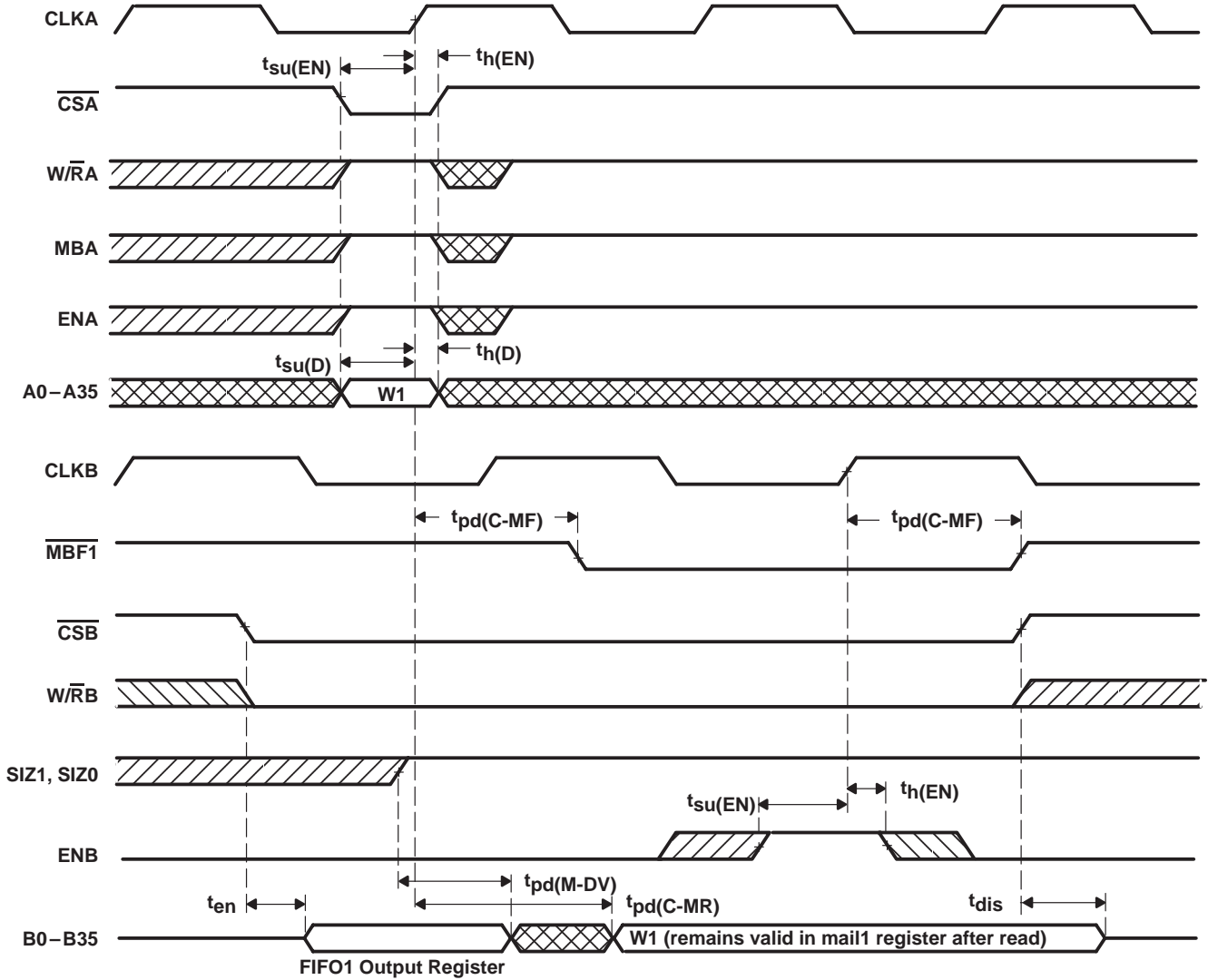
NOTE A: Port-B parity generation off (PGB = L)

Figure 21. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag
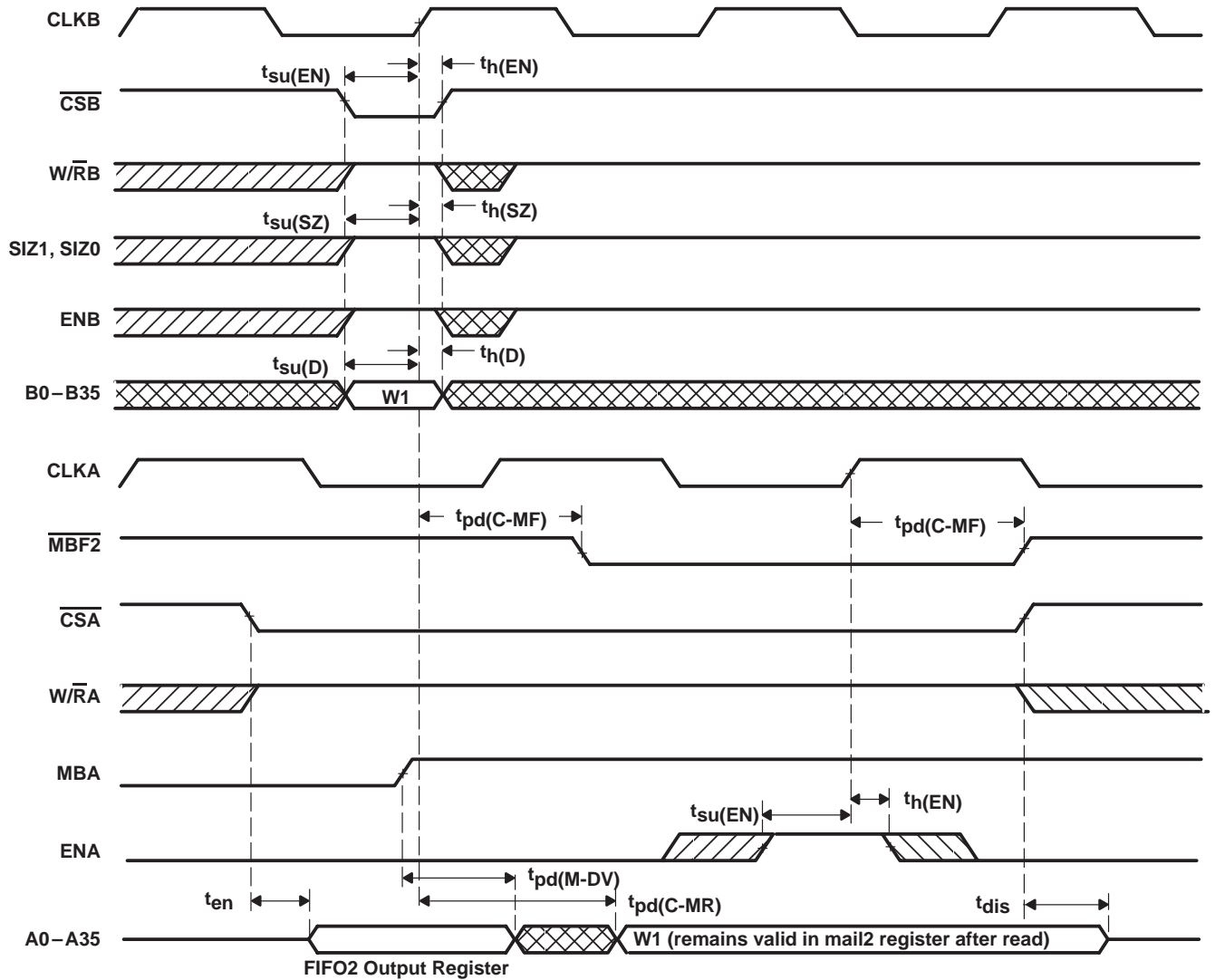
NOTE A: Port-A parity generation off (PGA = L)

Figure 22. Timing for Mail2 Register and MBF2 Flag
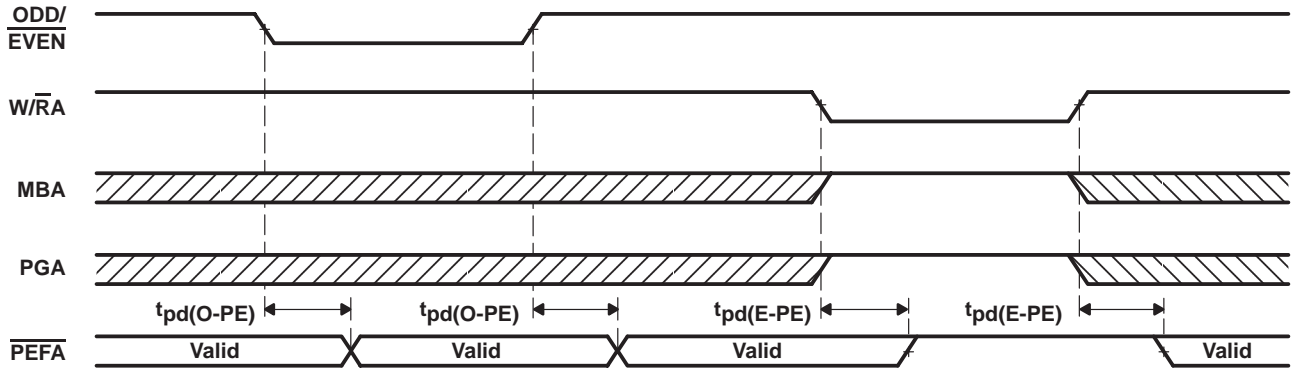
Figure 23. ODD/$\overline{\text{EVEN}}$, W/$\overline{\text{RA}}$, MBA, and PGA to $\overline{\text{PEFA}}$ Timing
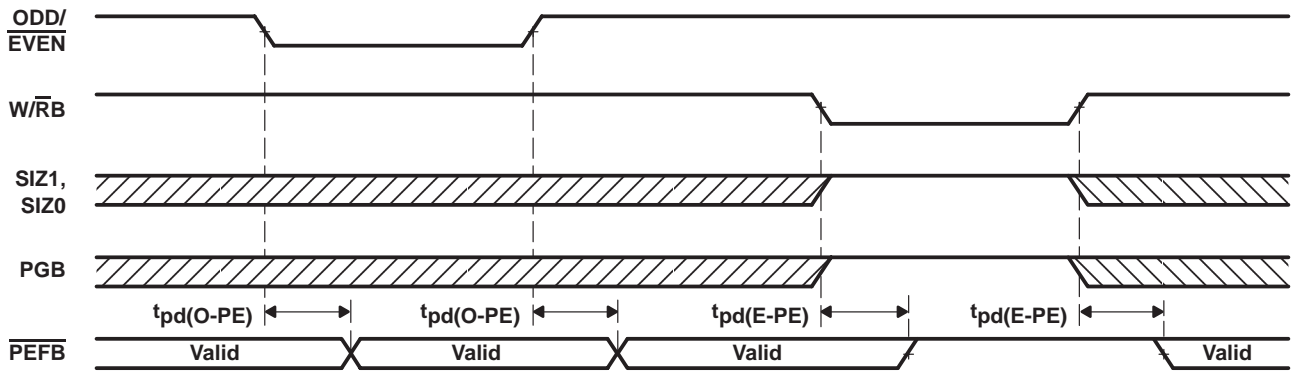
Figure 24. ODD/$\overline{\text{EVEN}}$, W/$\overline{\text{RB}}$, SIZ1, SIZ0, and PGB to $\overline{\text{PEFB}}$ Timing

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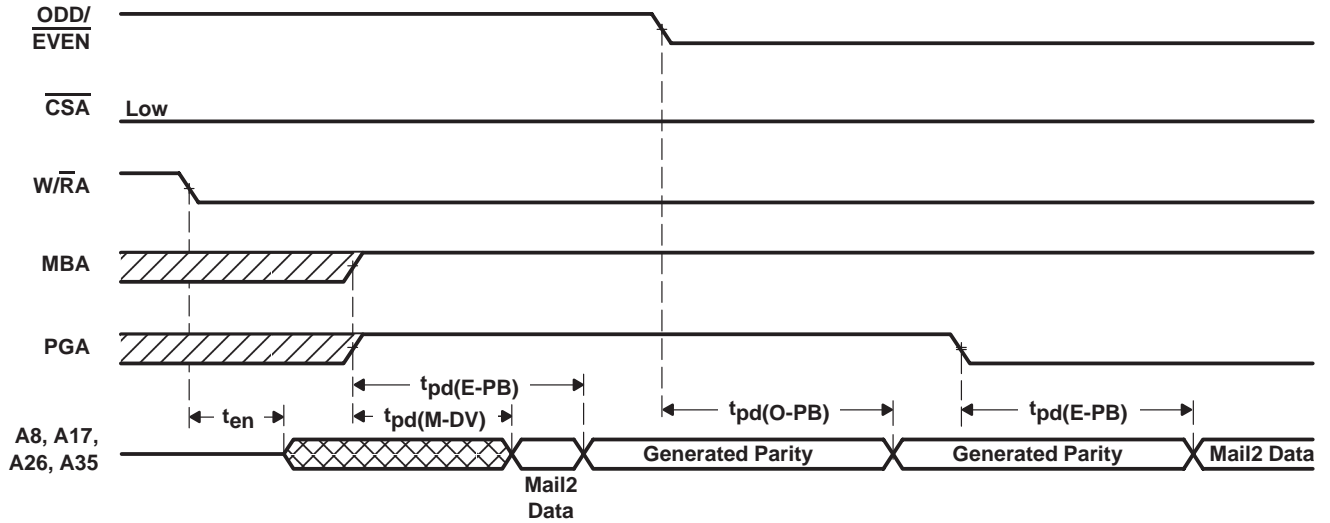
Figure 25. Parity-Generation Timing When Reading From the Mail2 Register
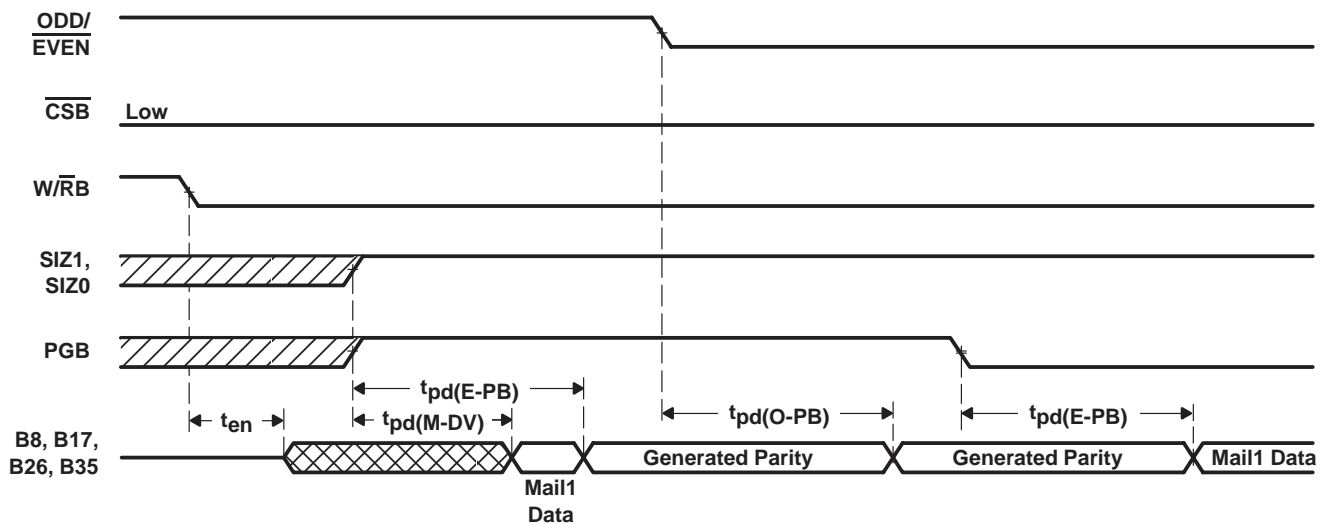
Figure 26. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±500 mA
Package thermal impedance, θ_{JA} (see Note 2): PCB package .... 28°C/W
                                                      PQ package .... 46°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.
        2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±50	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA, V_I = V_{CC} or GND	Outputs high			30	mA
			Outputs low			130	
			Outputs disabled			30	
C_i	V_I = 0,	f = 1 MHz			4		pF
C_o	V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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64 × 36 × 2 CLOCKED BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY
WITH BUS MATCHING AND BYTE SWAPPING

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 4 through 27)

		'ABT3614-15		'ABT3614-20		'ABT3614-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB before CLKB↑	5		5		6		ns
$t_{su(SZ)}$	Setup time, SIZ0, SIZ1, and $\overline{BE}$ before CLKB↑	4		5		6		ns
$t_{su(SW)}$	Setup time, SW0 and SW1 before CLKB↑	5		7		8		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑†	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB after CLKB↑	1		1		1		ns
$t_{h(SZ)}$	Hold time, SIZ0, SIZ1, and $\overline{BE}$ after CLKB↑	2		2		2		ns
$t_{h(SW)}$	Hold time, SW0 and SW1 after CLKB↑	0		0		0		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑†	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	4		4		4		ns
t_{sk1}§	Skew time between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8		8		10		ns
t_{sk2}§	Skew time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9		16		20		ns

† Applies only for a clock edge that does a FIFO read
‡ Requirement to count the clock edge as one of at least four needed to reset a FIFO
§ Skew time is not a timing constraint for proper device operation and is included only to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 4 through 27)

PARAMETER		'ABT3614-15 MIN	'ABT3614-15 MAX	'ABT3614-20 MIN	'ABT3614-20 MAX	'ABT3614-30 MIN	'ABT3614-30 MAX	UNIT
f_{max}		66.7		50		33.4		MHz
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C-FF)}$	Propagation delay time, CLKA↑ to $\overline{FFA}$ and CLKB↑ to $\overline{FFB}$	2	10	2	12	2	15	ns
$t_{pd(C-EF)}$	Propagation delay time, CLKA↑ to $\overline{EFA}$ and CLKB↑ to $\overline{EFB}$	2	10	2	12	2	15	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	2	10	2	12	2	15	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	2	10	2	12	2	15	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35[†] and CLKB↑ to A0–A35[‡]	3	11	3	13	3	15	ns
$t_{pd(C-PE)}$[§]	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	11	2	12	2	13	ns
$t_{pd(M-DV)}$	Propagation delay time, MBA to A0–A35 valid and SIZ1, SIZ0 to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D-PE)}$	Propagation delay time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
$t_{pd(O-PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O-PB)}$[¶]	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	2	14	ns
$t_{pd(E-PE)}$	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
$t_{pd(E-PB)}$[¶]	Propagation delay time, MBA or PGA to parity bits (A8, A17, A26, A35); SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ to ($\overline{MBF1}$, $\overline{MBF2}$) high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and W/$\overline{RB}$ high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or W/$\overline{RB}$ low to B0–B35 at high impedance	1	8	1	9	1	11	ns

[†] Writing data to the mail1 register when the B0–B35 outputs are active and SIZ1, SIZ0 are high
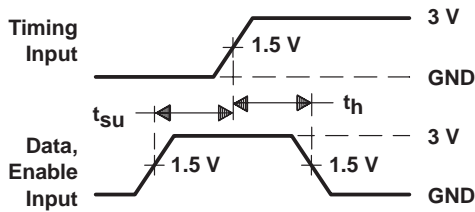[‡] Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high
[§] Applies only when a new port-B bus size is implemented by the rising CLKB edge
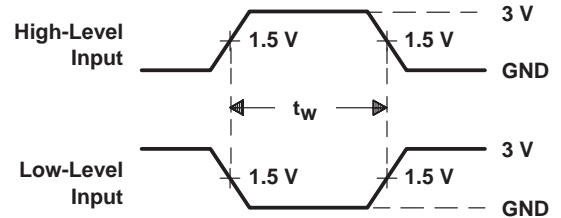[¶] Applies only when reading data from a mail register

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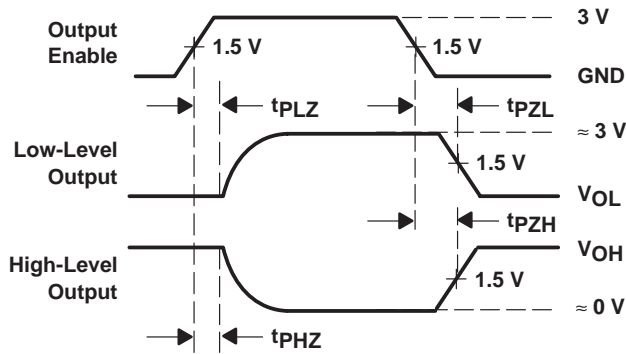## PARAMETER MEASUREMENT INFORMATION
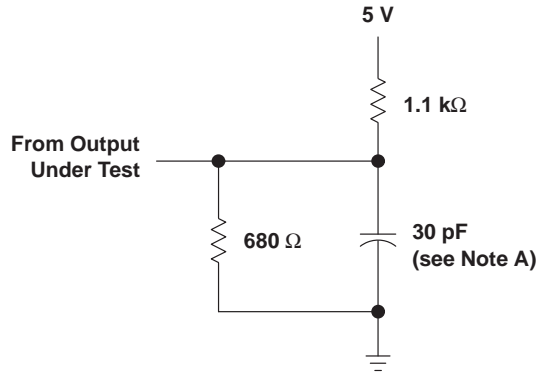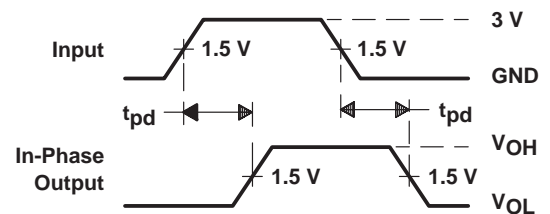
LOAD CIRCUIT

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. Includes probe and jig capacitance
        B. t_{PZL} and t_{PZH} are the same as t_{en}.
        C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Figure 27. Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

Figure 28

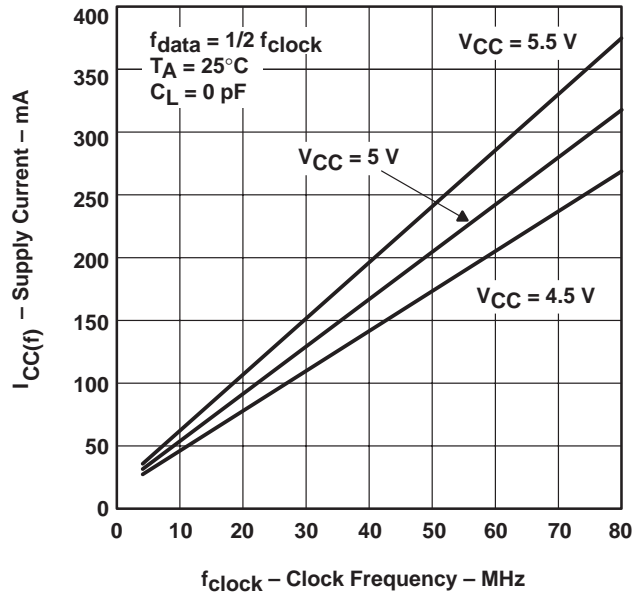TEXAS
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