Click here to ask about the production status of specific part numbers.

MAX22199

Octal Industrial Digital Input

General Description

The MAX22199 is an IEC 61131-2 compliant industrial digital input device. The MAX22199 translates eight 24V current-sinking industrial inputs to a serialized SPI-compatible output that interfaces with 3V to 5.5V logic. It can operate as eight Type 1/Type 3 digital inputs or four Type 2 digital inputs. The device provides diagnostic functions, including thermal shutdown, 24V under voltage alarm, 24V missing voltage alarm, and SPI and CRC communication error detection. All of the faults can be configured to generate an interrupt using the $\overline{\text{FAULT}}$ pin.

For robust operation in industrial environments, each input includes a programmable glitch filter. Noise filters on each channel can be independently programmed to one of eight values between 50µs and 20ms or filter bypass.

The MAX22199 has a 4-pin SPI interface and, in addition, uses the $\overline{\text{LATCH}}$ input for synchronizing input data sampling across multiple devices.

The MAX22199 field-side accepts a single 7V to 65V supply to the V_{DD24} pin. When powered by the field supply, the MAX22199 generates a 3.3V output from an integrated LDO regulator, which can provide up to 25mA of current for external loads in addition to powering the MAX22199. Alternatively, the MAX22199 can be powered from a 3.0V to 5.5V logic side supply connected to the V_{DD} pin. For flexibility, the SPI interface operates at 3.3V or 5V logic levels as controlled by the V_L pin.

Applications

- Programmable Logic Controllers
- Distributed Control System
- Motor Control
- Building Automation

Benefits and Features

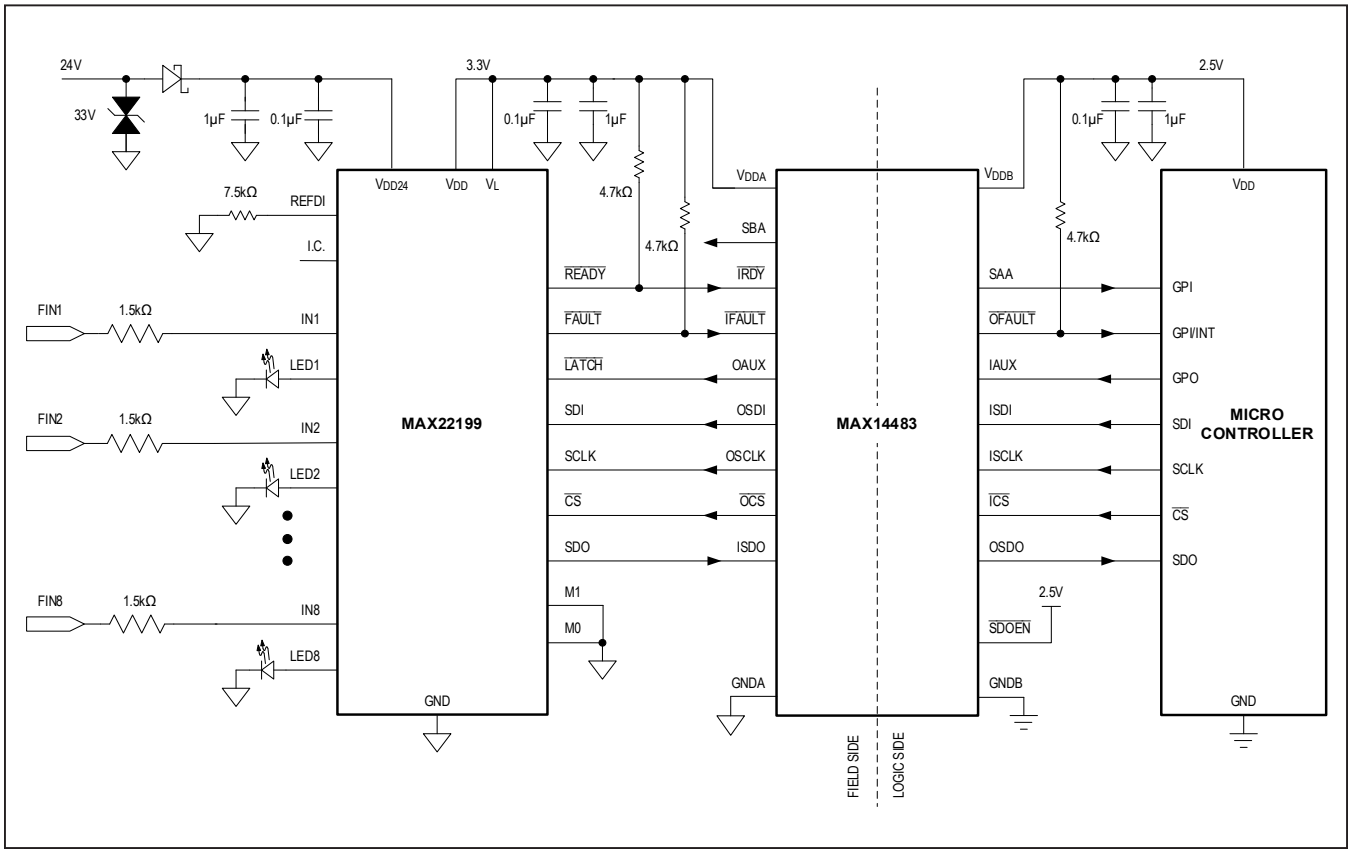
- High Integration Reduces BOM Count and Board Space
  - Eight Input Channels with Serializer
  - Operates Directly from Field Supply (7V to 65V)
  - Compatible with 3.3V or 5V Logic
  - 5mm x 5mm TQFN Package
- Reduced Power and Heat Dissipation
  - 0.6mA (typ) Supply Current
  - ±11% Accurate Input-Current Limiters
  - Energyless Field-Side LED Drivers
  - Low Power Dissipation with Negative Input Voltage
- Fault Tolerant
  - Input Protection to ±40V
  - Integrated Field-Supply Voltage Monitors
  - 5-Bit CRC SPI Error Detection
- Configurability Enables Wide Range of Applications
  - Configurable Input Current from 0.5mA to 3.4mA
  - Selectable Input Debounce Filtering
  - Current Sources Can Be Disabled
  - Supports Daisy-Chain SPI and Direct SPI
- Robust Design
  - ±8kV Contact ESD and ±15kV Air-Gap ESD Using Minimum 1kΩ Resistor
  - ±2kV Surge Tolerant Using Minimum 1kΩ Resistor
  - -40°C to +125°C Ambient Operating Temperature
- Advanced Diagnostics Can Be Provided by **MAX22190**
  - Pin-to-Pin Compatible
  - Register Compatible

***Ordering Information* appears at end of data sheet.**

19-101135; Rev 0; 5/21

maxim integrated™

Isolated Octal Type 1/3 Digital Input



Absolute Maximum Ratings

V_L, V_{DD} to GND .....-0.3V to +6V
V_{DD24} to GND.....-0.3V to +70V
SCLK, $\overline{CS}$, SDI, M0, M1 to GND.....-0.3V to +6V
$\overline{LATCH}$, $\overline{FAULT}$, $\overline{READY}$ to GND .....-0.3V to +6V
REFDI to GND.....-0.3V to (V_{DD} + 0.3V)
SDO to GND.....-0.3V to (V_L + 0.3V)
IN1–IN8 to GND .....-40V to +40V
LED1–LED8 to GND .....-0.3V to +6V

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate at 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range
Ambient Temperature .....+125°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN	
Package Code	T3255+6
Outline Number	**21-0140**
Land Pattern Number	**90-0603**
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, C_L = 15pF, unless otherwise noted. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, $V_{IN\_}$ = +24V, and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Logic Supply Voltage	V_L			3.0		5.5	V
Logic Supply Current	I_L	V_L = 5.5V	$\overline{CS}$ = V_L, All logic pins static		13	30	µA
Supply Voltage	V_{DD24}	Normal operation		7		65	V
	V_{DD}	Powered from an external supply		3.0		5.5	V
Supply Current of V_{DD24}	I_{DD24}	V_{DD24} = 24V	IN1–IN8 = 0V, LED1–LED8 = GND, SPI static, REFDI = 7.5kΩ		0.6	1.2	mA
Supply Current Powered From V_{DD}	I_{DD}	V_{DD} = 3.3V	IN1–IN8 = 0V, LED1–LED8 = GND, SPI static, REFDI = 7.5kΩ		0.6	1.2	mA

DC Electrical Characteristics (continued)

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, C_L = 15pF, unless otherwise noted. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, $V_{IN\_}$ = +24V, and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Undervoltage-Lockout Threshold	V_{UVLO}	V_{DD} rising	2.4		2.9	V
V_{DD} Undervoltage-Lockout Threshold Hysteresis	V_{UVHYST}			0.07		V
V_{DD24} Undervoltage-Lockout Threshold	V_{UVLO24}	V_{DD24} rising	6		6.8	V
V_{DD24} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST24}$			0.5		V
V_L Undervoltage-Lockout Threshold	V_{UVLOVL}	V_L rising	0.9		1.6	V
V_L Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYSTVL}$			0.07		V
Regulator Output Voltage	V_{DD}	I_{LOAD} = 1mA, V_{DD24} ≥ 7V	3.0	3.3	3.6	V
Line Regulation	dV_{DDLINE}	I_{LOAD} = 1mA, V_{DD24} = 12V to 24V		0		mV
Load Regulation	dV_{DDLOAD}	I_{LOAD} = 1mA to 10mA, V_{DD24} = 24V		4		mV
Regulator Current Capability	I_{DD_CC}				25	mA
Short-Circuit Current	I_{DD24_SC}	V_{DD24} current when V_{DD} shorted to GND	28		50	mA
$\overline{READY}$ Threshold	V_{READY}	V_{DD} rising, V_{DD24} = 0V	2.4		2.9	V
$\overline{READY}$ Threshold Hysteresis	V_{READY_HYST}			0.07		V
$\overline{READY}$ Delay	$\overline{READY}_{DELAY}$	V_{DD} valid to $\overline{READY}$ low		1		ms
SUPPLY ALARMS						
V_{DD24} UV Alarm On/Off	$V_{ALRMOFFUV}$	V_{DD24} rising, under voltage			17	V
V_{DD24} UV Alarm Off/On	$V_{ALRMONUV}$	V_{DD24} falling, under voltage	15			V
Glitch Filter for V_{DD24} UV				3		µs
V_{DD24} VM Alarm On/Off	$V_{ALRMOFFVM}$	V_{DD24} rising, missing voltage			13.9	V
V_{DD24} VM Alarm Off/On	$V_{ALRMONVM}$	V_{DD24} falling, missing voltage	12.1			V
Glitch Filter for V_{DD24} VM				3		µs
TEMPERATURE ALARM						
Thermal-Shutdown Threshold	T_{SHDN}	OTSHDN bit set in FAULT2 register		165		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			10		°C
IN_ INPUTS						
Input Threshold Low-to-High	V_{THIN+}	All inputs, IN1 to IN8			6	V
Input Threshold High-to-Low	V_{THIN-}	All inputs, IN1 to IN8	4.4			V
Input Threshold Hysteresis	V_{INHYST}	All inputs, IN1 to IN8		0.8		V

DC Electrical Characteristics (continued)

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, C_L = 15pF, unless otherwise noted. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, $V_{IN\_}$ = +24V, and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DI Leakage	I_{DI_LEAK}	Channel disabled, EN_ = 0	IN1 to IN8 = 36V		73		µA
			IN1 to IN8 = 24V		42		µA
LED_ OUTPUTS							
LED On-State Current	I_{LEDON}	R_{REFDI} = 7.5kΩ, V_{LED} = 3V		1.5			mA
REFDI							
REFDI Pin Voltage	V_{REFDI}	R_{REFDI} = 5.2kΩ to 36kΩ			0.61		V
IN_ INPUT CURRENT							
Input Current Limit	I_{INLIM}	28V > $V_{IN\_}$ > 5V	R_{REFDI} = 7.5kΩ	2.10	2.35	2.60	mA
			R_{REFDI} = 5.2kΩ	3.05	3.39	3.71	
FIELD INPUT TYPE 1, 3: EXTERNAL SERIES RESISTOR $R_{IN\_}$ = 1.5kΩ, R_{REFDI} = 7.5kΩ							
Field Input Threshold Low-to-High	V_{THFIN+}	R_{REFDI} = 7.5kΩ, external series resistor $R_{IN\_}$ = 1.5kΩ				9.9	V
Field Input Threshold High-to-Low	V_{THFIN-}	R_{REFDI} = 7.5kΩ, external series resistor $R_{IN\_}$ = 1.5kΩ		7.4			V
Field Input Threshold Hysteresis	$V_{FINHYST}$	R_{REFDI} = 7.5kΩ, external series resistor $R_{IN\_}$ = 1.5kΩ			0.9		V
FIELD INPUT TYPE 2: EXTERNAL SERIES RESISTOR $R_{IN\_}$ = 1kΩ, R_{REFDI} = 5.2kΩ							
Field Input Threshold Low-to-High	V_{THFIN+}	R_{REFDI} = 5.2kΩ, external series resistor $R_{IN\_}$ = 1kΩ				9.9	V
Field Input Threshold High-to-Low	V_{THFIN-}	R_{REFDI} = 5.2kΩ, external series resistor $R_{IN\_}$ = 1kΩ		7.4			V
Field Input Threshold Hysteresis	$V_{FINHYST}$	R_{REFDI} = 5.2kΩ, external series resistor $R_{IN\_}$ = 1kΩ			0.9		V
INPUT FILTER							
Input Filter Delay (See bits DELAY_[2:0] in FLT_ register)	t_{BOUNCE}	FBP_ = 1: bypass filtering			2		µs
		FBP_ = 0, DELAY_ = 0			0.05		ms
		FBP_ = 0, DELAY_ = 1			0.1		
		FBP_ = 0, DELAY_ = 2			0.4		
		FBP_ = 0, DELAY_ = 3			0.8		
		FBP_ = 0, DELAY_ = 4			1.6		
		FBP_ = 0, DELAY_ = 5			3.2		
		FBP_ = 0, DELAY_ = 6			12.8		
		FBP_ = 0, DELAY_ = 7			20		

DC Electrical Characteristics (continued)

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, C_L = 15pF, unless otherwise noted. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, $V_{IN\_}$ = +24V, and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Input (IN_) Sampling Rate	f_{IN}	Input Filter Bypass mode		1000		kHz
		Input Filter Non-Bypass mode		200		
Minimum Detectable IN_ Pulse Width	t_{PW}	No external capacitors on input pins IN1 to IN8		3		µs
$\overline{LATCH}$ Delay		Assertion of $\overline{LATCH}$ or $\overline{CS}$ until input data is frozen		50		ns
$\overline{FAULT}$ Minimum Pulse Width	$t_{\overline{FAULT}\_PW}$	$\overline{FAULT}$ low, pullup 4mA	0.8			µs
LOGIC INTERFACE						
Input Logic-High Voltage	V_{IH}	SCLK, $\overline{CS}$, SDI, $\overline{LATCH}$, M0, M1 relative to GND	0.7 x V_L			V
Input Logic-Low Voltage	V_{IL}	SCLK, $\overline{CS}$, SDI, $\overline{LATCH}$, M0, M1 relative to GND			0.3 x V_L	V
Output Logic-High Voltage	V_{OH}	SDO, sourcing 4mA	V_L - 0.4			V
Output Logic-Low Voltage	V_{OL}	SDO, $\overline{FAULT}$, $\overline{READY}$ sinking 4mA			0.4	V
Input Pullup Resistance $\overline{CS}$, $\overline{LATCH}$	R_{PU}			195		kΩ
Input Pulldown Resistance SCLK, SDI, M1, M0	R_{PD}			195		

Dynamic Electrical Characteristics

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, C_L = 15pF, unless otherwise noted. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, $V_{IN\_}$ = +24V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI CHARACTERISTICS						
SCLK Pulse Width-High	t_{SCLKH}	See Figure 1	20			ns
SCLK Pulse Width-Low	t_{SCLKL}	See Figure 1	20			ns
SCLK Clock Period	t_{SCLK}	See Figure 1	100			ns
SCLK Clock Frequency	f_{SCLK}				10	MHz
$\overline{CS}$ Pulse Width	t_{CSBPW}	See Figure 1	20			ns
SDI-to-SCLK Setup Time	t_{DINSU}	See Figure 1	5			ns
SDI-to-SCLK Hold Time	t_{DINH}	See Figure 1	15			ns
$\overline{CS}$-Fall-to-SCLK-Rise Time	t_{CLK_SU}	See Figure 1	80			ns
SCLK-Rise-to-$\overline{CS}$-Rise Time	t_{CSBH}	Rising edge of SCLK to rising edge of $\overline{CS}$ (Figure 1)	40			ns
SDO Enable Time	$t_{CSB\_SDOVALID}$	$\overline{CS}$ falling to SDO valid (Figure 1)			50	ns
SDO Disable Time	t_{CSB_SDOTRI}	$\overline{CS}$ rising to SDO tristate (Figure 1)			50	ns
Output Data Propagation Delay	t_{DO}	SCLK falling edge-to-SDO valid (Figure 1)			50	ns
Rise/Fall Time SDO	$t_{R/F}$	SDO 10% to 90% rising, 90% to 10% falling		4		ns

Note 1: All specifications are production tested at T_A = 25°C. Specifications over temperature are guaranteed by design.

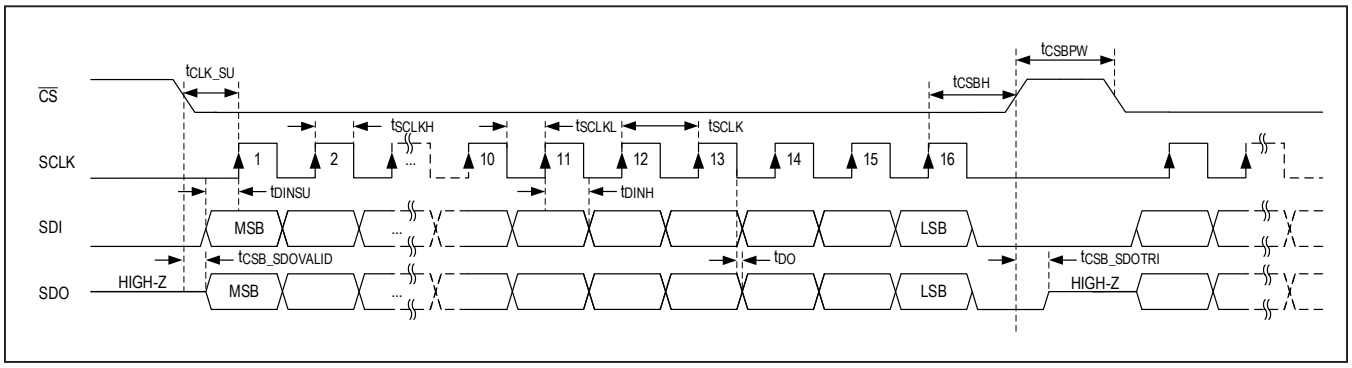


Figure 1. SPI Timing Diagram

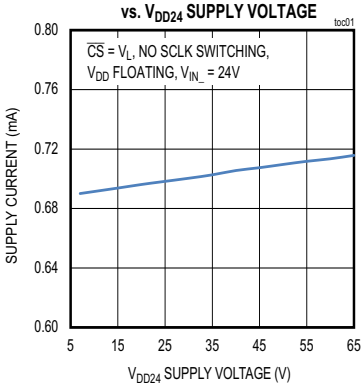
ESD and EMC Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Surge	Line-to-Line	IEC 61000-4-5, 1.2/50µs pulse, minimum 1kΩ resistor in series with IN1–IN8	±2	kV
	Line-to-Ground	IEC 61000-4-5, 1.2/50µs pulse, minimum 1kΩ resistor in series with IN1–IN8	±2	
ESD	Human Body Model	All pins	±2	
	Contact	IEC 61000-4-2, minimum 1kΩ resistor in series with IN1–IN8	±8	
	Air-Gap	IEC 61000-4-2, minimum 1kΩ resistor in series with IN1–IN8	±15	

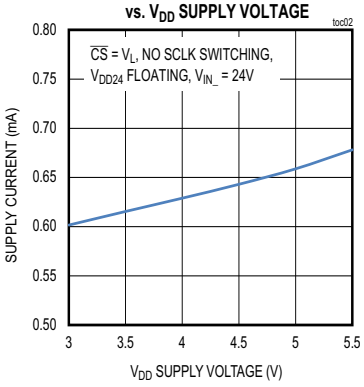
Typical Operating Characteristics

(V_{DD24} = 24V, V_{DD} = V_L = 3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{IN} = 1.5kΩ, EN_ = 1, $V_{FIN\_}$ = voltage measured at the field side, $V_{IN\_}$ = voltage measured at the pin, unless otherwise noted.)

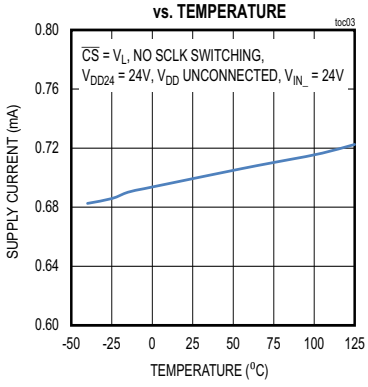
V_{DD24} SUPPLY CURRENT vs. V_{DD24} SUPPLY VOLTAGE



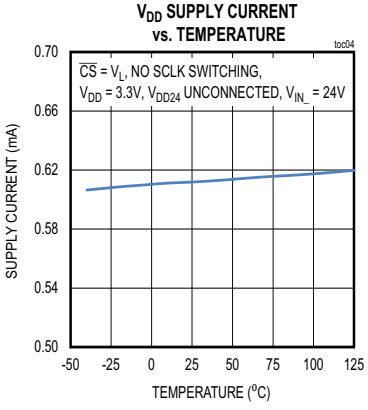
V_{DD} SUPPLY CURRENT vs. V_{DD} SUPPLY VOLTAGE



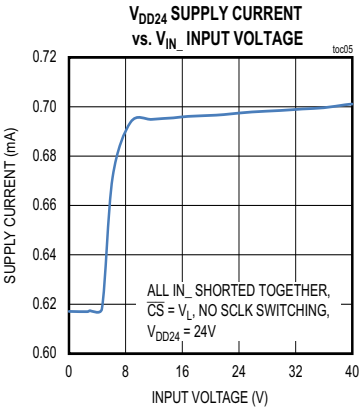
V_{DD24} SUPPLY CURRENT vs. TEMPERATURE



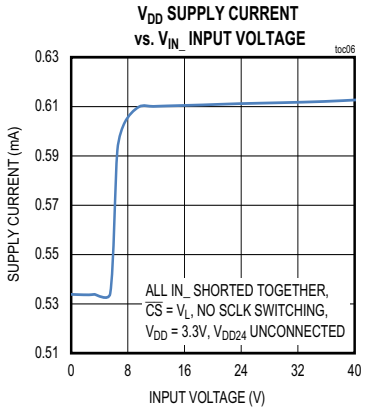
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



V_{DD24} SUPPLY CURRENT vs. $V_{IN\_}$ INPUT VOLTAGE



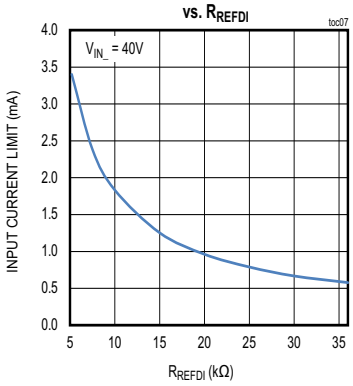
V_{DD} SUPPLY CURRENT vs. $V_{IN\_}$ INPUT VOLTAGE



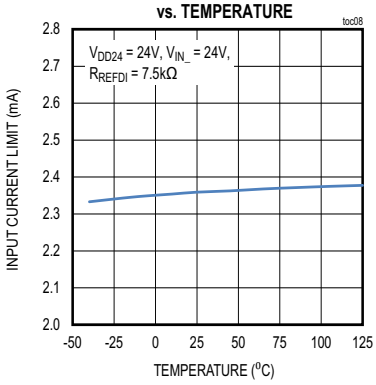
Typical Operating Characteristics (continued)

(V_{DD24} = 24V, V_{DD} = V_L = 3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{IN} = 1.5kΩ, EN_ = 1, $V_{FIN\_}$ = voltage measured at the field side, $V_{IN\_}$ = voltage measured at the pin, unless otherwise noted.)

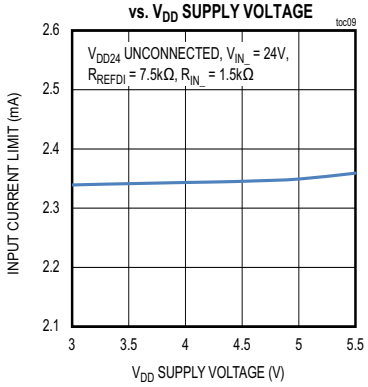
INPUT CURRENT LIMIT I_{INLIM} vs. R_{REFDI}



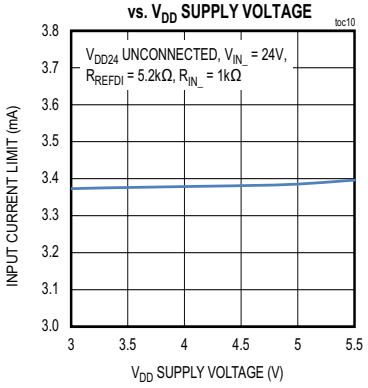
INPUT CURRENT LIMIT I_{INLIM} vs. TEMPERATURE



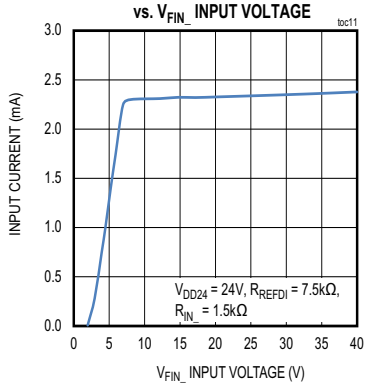
INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD} SUPPLY VOLTAGE



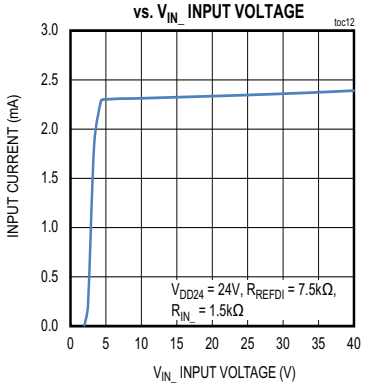
INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD} SUPPLY VOLTAGE



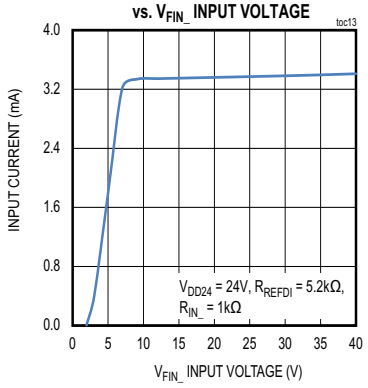
INPUT CURRENT $I_{IN\_}$ vs. $V_{FIN\_}$ INPUT VOLTAGE



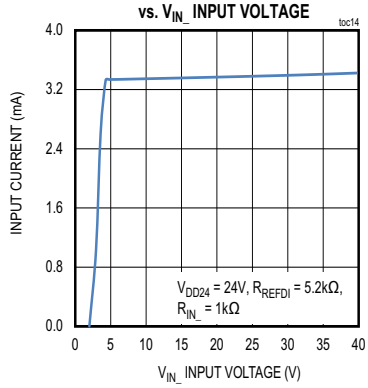
INPUT CURRENT $I_{IN\_}$ vs. $V_{IN\_}$ INPUT VOLTAGE



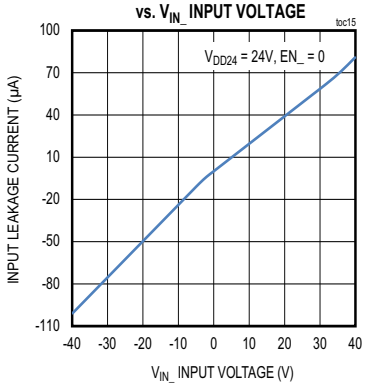
INPUT CURRENT $I_{IN\_}$ vs. $V_{FIN\_}$ INPUT VOLTAGE



INPUT CURRENT $I_{IN\_}$ vs. $V_{IN\_}$ INPUT VOLTAGE

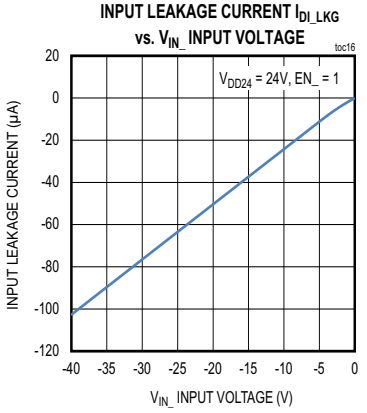


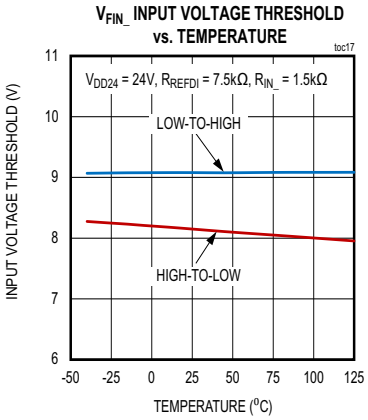
INPUT LEAKAGE CURRENT I_{DI_LKG} vs. $V_{IN\_}$ INPUT VOLTAGE

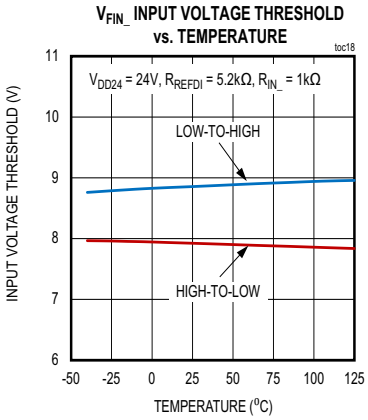


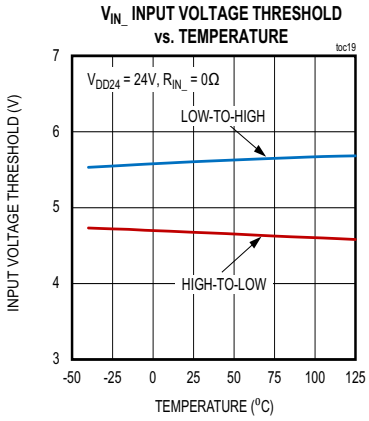
Typical Operating Characteristics (continued)

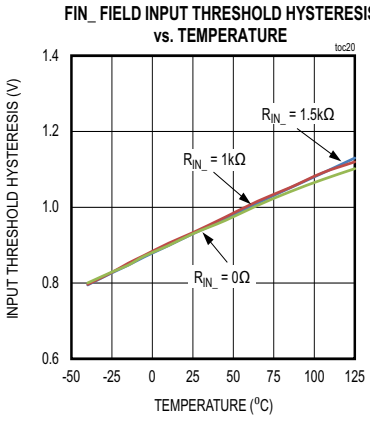
(V_{DD24} = 24V, V_{DD} = V_L = 3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{IN} = 1.5kΩ, EN_ = 1, $V_{FIN\_}$ = voltage measured at the field side, $V_{IN\_}$ = voltage measured at the pin, unless otherwise noted.)

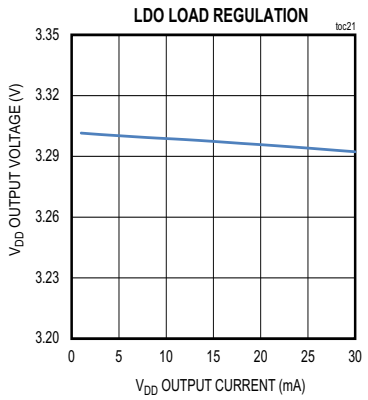


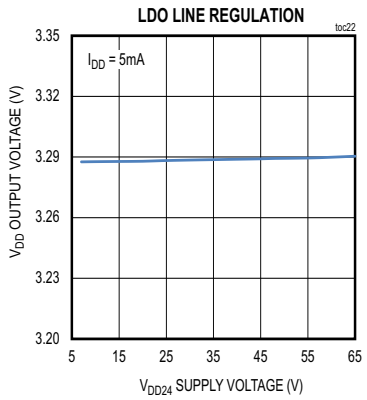


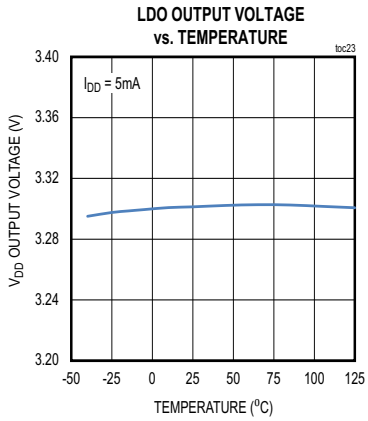


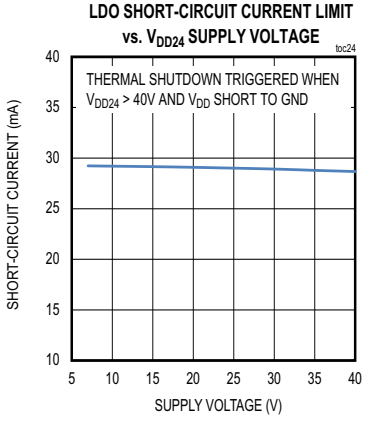






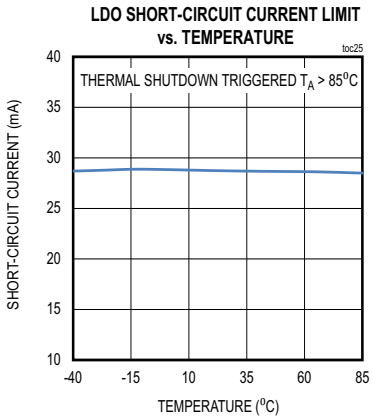


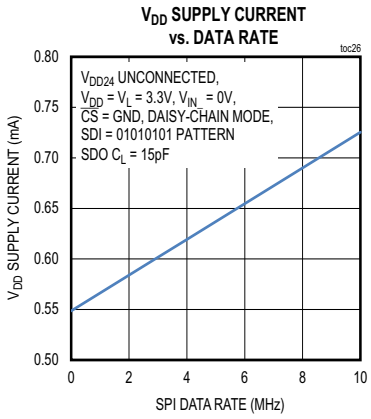




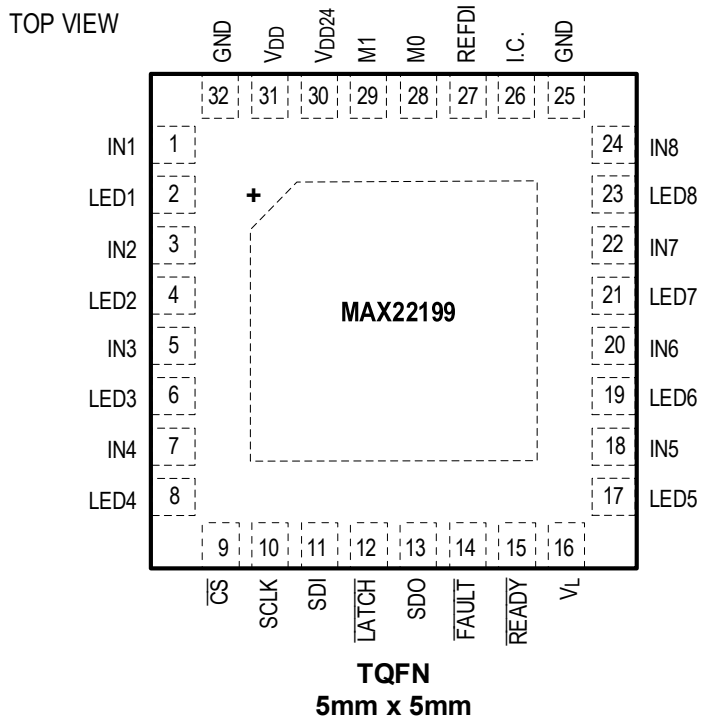
Typical Operating Characteristics (continued)

(V_{DD24} = 24V, V_{DD} = V_L = 3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{IN} = 1.5kΩ, EN_ = 1, $V_{FIN\_}$ = voltage measured at the field side, $V_{IN\_}$ = voltage measured at the pin, unless otherwise noted.)





Pin Configuration

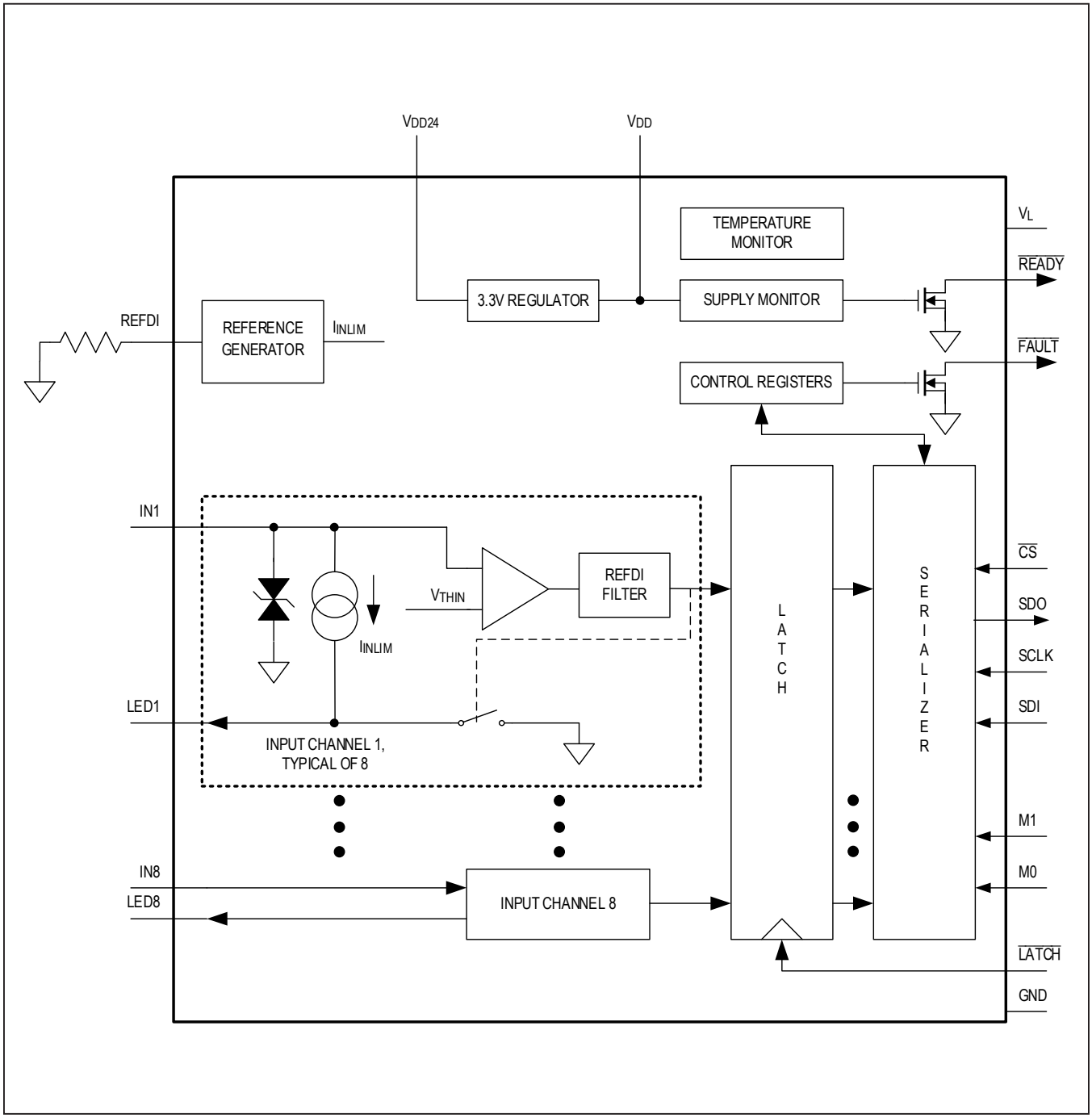


TQFN
5mm x 5mm

Pin Description

PIN	NAME	FUNCTION
POWER SUPPLY		
16	V_L	Logic Interface Supply, 3.0V to 5.5V. Bypass to GND with a 0.1µF capacitor in parallel with a 1µF capacitor.
25, 32	GND	Ground return for all field inputs and the field power supply.
30	V_{DD24}	24V field supply. Bypass to GND with 0.1µF capacitor in parallel with 1µF capacitor.
31	V_{DD}	3.3V Output from integrated LDO when powered from V_{DD24}, or 3.0 – 5.5V Supply Input when V_{DD24} not driven. Bypass to GND with 0.1µF capacitor in parallel with 1µF capacitor. If powering the MAX22199 from an external supply on V_{DD}, leave V_{DD24} unconnected.
EP	—	Exposed Pad. Connect to GND. Solder entire exposed pad area to ground plane for best thermal performance.
SPI INTERFACE		
9	$\overline{CS}$	Chip-Select Input. Assert low to latch input states and enable the SPI interface.
10	SCLK	Serial Clock Input.
11	SDI	Serial Data Input. Data is clocked into SDI on the rising edge of SCLK.
12	$\overline{LATCH}$	$\overline{LATCH}$ and $\overline{CS}$ control the data latching at the input of the serializer (after the inputs). The latch is transparent when both $\overline{CS}$ and $\overline{LATCH}$ are high. The data at the input of the serializer is frozen on the falling edge of either $\overline{LATCH}$ or $\overline{CS}$. $\overline{LATCH}$ is typically used to synchronize input channel sampling across multiple MAX22199s.
13	SDO	Serial Data Output. Data is updated on the falling edge of SCLK. When $\overline{CS}$ is high, SDO is high-impedance.
14	$\overline{FAULT}$	Active-Low Fault Indicator. Open-drain output, $\overline{FAULT}$ goes low to indicate that one or more of the flags in the FAULT registers have been set. The faults include supply monitors, thermal shutdown, CRC error, etc.
15	$\overline{READY}$	Open-Drain Output. $\overline{READY}$ goes low indicating that the MAX22199 is powered and ready for operation.
CONFIGURATION PINS		
26	I.C.	Internally Connected. Leave I.C. unconnected or connect to GND.
27	REFDI	Digital Input Current-Limit Reference Resistor. For 24V Type 1 and Type 3 inputs, place a 7.5kΩ resistor from REFDI to GND.
28	M0	SPI Mode Control. Connect M1 to high to enable the SPI daisy-chain mode. Connect M0 to high to disable the CRC error detection. See Table 1 for details.
29	M1	
INPUT PINS		
1, 3, 5, 7, 18, 20, 22, 24	IN1–IN8, respectively	Field inputs. For Type 1 and Type 3 inputs, place a 1.5kΩ resistor between the field input and the IN_ pin. Capacitors for filtering should not be connected to the IN_ pins. See the *Surge Protection of Field Inputs* section for further information.
2, 4, 6, 8, 17, 19, 21, 23	LED1–LED8, respectively	Energyless LED Driver Outputs. Connect to GND if LEDs are not used.

Functional Block Diagram

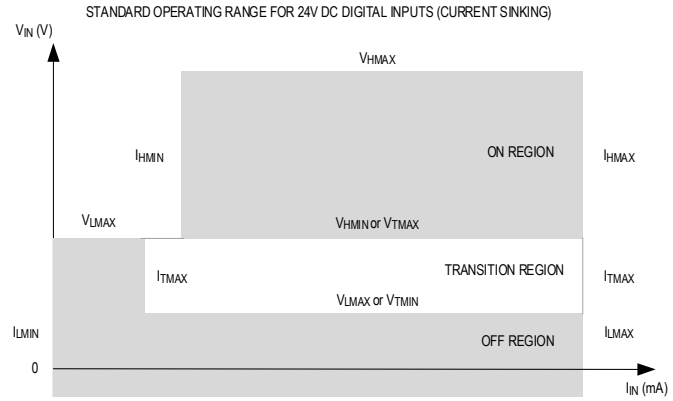


Detailed Description

The MAX22199 senses the state (on, high or off, low) of eight digital inputs. The voltages at the IN1 to IN8 input pins are compared against internal references to determine whether the sensor is on (logic 1) or off (logic 0). All eight inputs are simultaneously latched by the assertion of either $\overline{LATCH}$ or $\overline{CS}$, and the data is made available in a serialized format through the SPI interface. Placing a 7.5kΩ current-setting resistor between REFDI and GND, and a 1.5kΩ resistor between each field input and the corresponding IN_ input pin ensures that the current at the ON and OFF trip points as well as the voltage at the trip points satisfy the requirements of IEC 61131-2 for Type 1 and Type 3 inputs. The current sunk by each input pin rises linearly with input voltage until the level set by the current limiter is reached; any voltage increase beyond this point does not increase the input current. Limiting the input current ensures compliance with IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs.

The current-setting resistor R_{REFDI} can be calculated using this equation:

$$R_{REFDI} = 17.63V \div I_{INLIM}$$



TYPE OF LIMIT	TYPE 1 LIMITS						TYPE 2 LIMITS						TYPE 3 LIMITS					
	OFF REGION		TRANSITION		ON REGION		OFF REGION		TRANSITION		ON REGION		OFF REGION		TRANSITION		ON REGION	
	V_L (V)	I_L (mA)	V_T (V)	I_T (mA)	V_H (V)	I_H (mA)	V_L (V)	I_L (mA)	V_T (V)	I_T (mA)	V_H (V)	I_H (mA)	V_L (V)	I_L (mA)	V_T (V)	I_T (mA)	V_H (V)	I_H (mA)
MAX	15/5	15	15	15	30	15	11/5	30	11	30	30	30	11/5	15	11	15	30	15
MIN	-3	ND	5	0.5	15	2	-3	ND	5	2	11	6	-3	ND	5	1.5	11	2

Figure 2. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24VDC Digital Inputs

Input Filters

The MAX22199 features a digital filter per channel to reduce glitches and noise at the input, making an analog RC filter unnecessary. Capacitors should not be connected to the IN_ pins for filtering. Each input (IN1 to IN8) has a programmable digital filter, input data can be filtered, or it can be bypassed for high-speed sampling. The input is sampled and data is latched at 1MHz (typ) when the input filter is disabled. When the digital filter is enabled, the input is sampled at 200kHz (typ). Bit FBP_ in the corresponding FLT_ register is used to bypass the filter or to enable the filter. One of eight filter delays (50µs, 100µs, 400µs, 800µs, 1.6ms, 3.2ms, 12.8ms, 20ms) can be independently selected for each channel.

Noise rejection is accomplished through a no-rollover up-down counter where the state of the field input controls the counting direction (up or down). The filter uses an up-down counter fed by a 200kHz clock. If the input is high, it counts up; if the input is low, it counts down. The filter output is updated when the counter hits the upper or lower limit, with the upper limit depending on the selected filter delay and the lower limit being zero regardless of the filter delay. The low-to-high transition of the filter occurs when the counter reaches the upper limit. The high-to-low transition occurs when the counter reaches the lower limit. There is no rollover; counting simply stops when the upper or lower limit is hit. The filter delay is the time it takes to reach the upper/lower limit in response to a step input when the counter starts from the lower/upper limit. If the input is not a step function, but is bouncing, as shown in Figure 3, the output changes state after a total delay of:

Total Delay = Filter Delay + 2 x (Total Time at the Old State)

In the example in Figure 3, the filter has a nominal delay of 1.6ms, and the input returns high for two 0.2ms periods after the first transition from high to low. These transitions back to the high state extend the time before the output of the filter switches. Total Delay = 1.6ms + 2 x (0.2ms + 0.2ms) = 2.4ms.

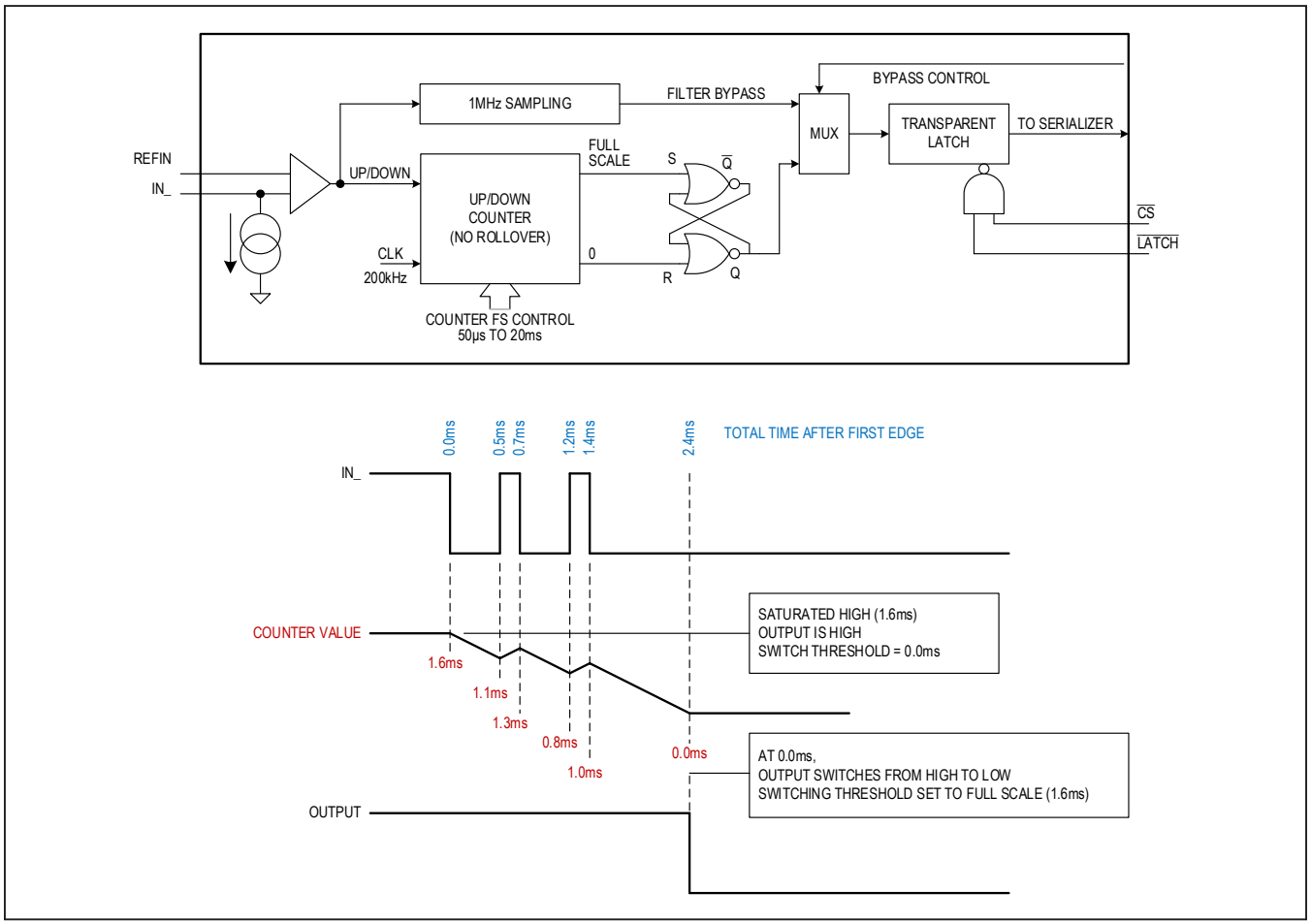


Figure 3. MAX22199 Digital Filter

Energyless LED Drivers

When IN_ is determined to be on, its input current is diverted to the LED_ pin and flows from that pin to GND. Placing an LED between LED_ and GND provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LED_ to GND.

Type 2 Sensor Inputs

The additional input current (6mA min) and associated power dissipation of Type 2 input requires the use of two MAX22199 inputs in parallel. The current of each channel is set to a nominal 3.39mA (6.78mA total) by placing a 5.2kΩ resistor from REFDI to GND. The proper voltage drop across the input resistor is maintained by reducing the resistance from 1.5kΩ to 1kΩ for each MAX22199 channel. For proper surge protection, it is important that each MAX22199 input has its own resistor. Any two MAX22199 channels can be used; they need not be contiguous (Figure 4). Either channel can be read to determine the input state. The additional power dissipation from this Type 2 configuration reduces the maximum ambient operating temperature to 120°C, when all inputs are at 30V, and the MAX22199 is powered from a 30V supply and there is no additional load on V_{DD}.

Thermal Consideration

The MAX22199 operates at an ambient temperature of up to 125°C on a properly designed PCB. Operating at higher voltages, with heavy output loads on V_{DD} while input channels are on increases power dissipation and reduces the maximum allowable operating temperature. See the *Package Information* and *Absolute Maximum Ratings* sections for safety operation temperature and maximum power dissipation.

The MAX22199 is in thermal shutdown when the thermal shutdown temperature threshold (165°C typical) is exceeded. During thermal shutdown, input channels, LED drivers, internal voltage regulator, and SPI interface are all turned off, except that register values are retained. A thermal shutdown event (OTSHDN) can be read back from the FAULT2 register once the device is out of thermal shutdown.

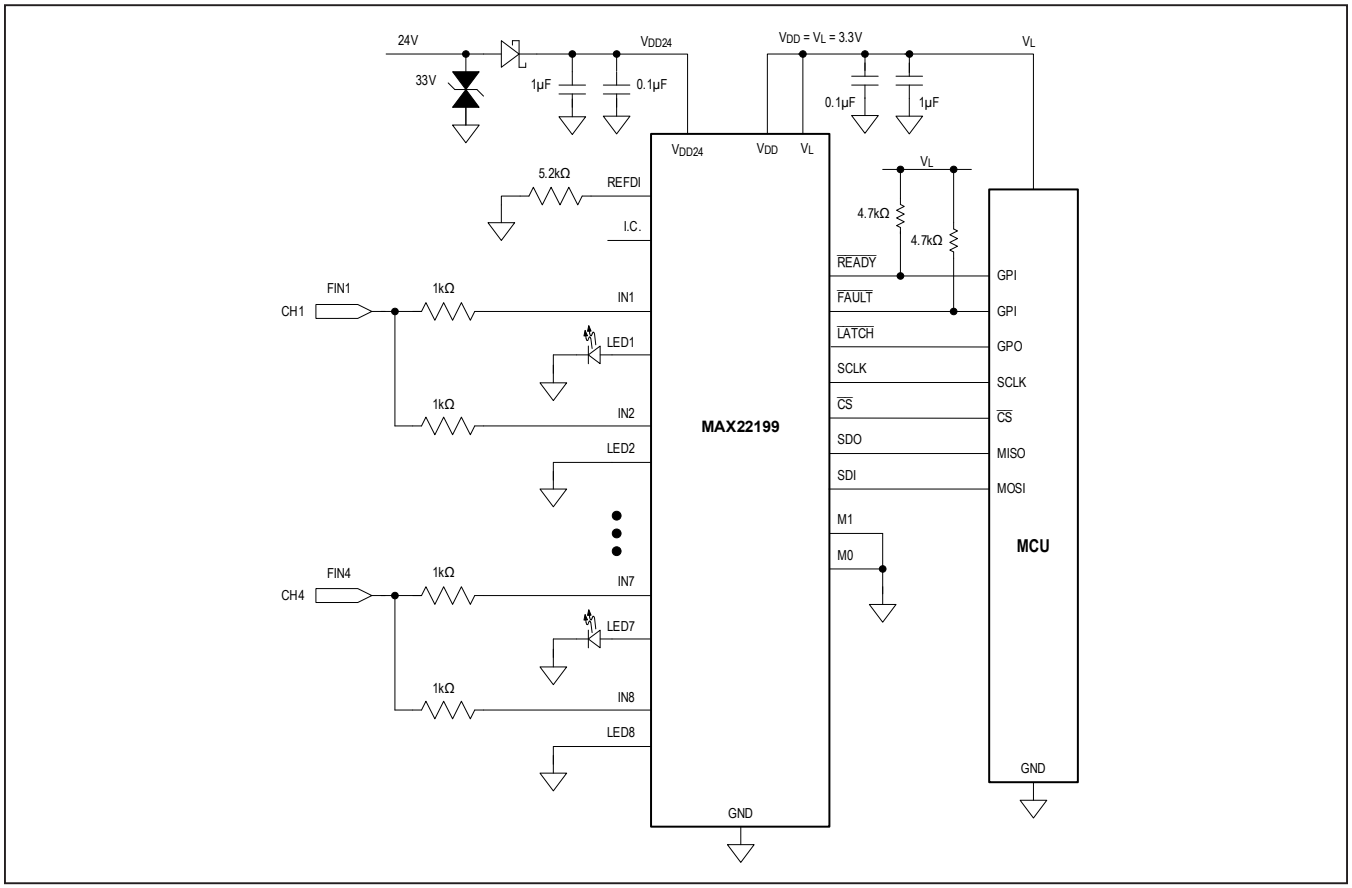


Figure 4. Implementing Type 2 Digital Inputs with the MAX22199

Fault Detection and Monitoring

$\overline{FAULT}$ is an open-drain output that can be wire ORed with other open-drain outputs and used to notify the host processor of a fault. When enabled, $\overline{FAULT}$ goes low to indicate that one or more of the flags in the FAULT1 register have been set. These faults are: V_{DD24} low voltage alarm (24VL), V_{DD24} voltage missing alarm (24VM), CRC error detected on the previous SPI frame (CRC), Power-On-Reset event (POR), and sources from the FAULT2 register.

Flags 24VL and 24VM in the FAULT1 register are latched; they remain set until read even if the fault goes away. The CRC bit is not latched, but remains set until an uncorrupted SPI frame is received. The POR bit indicates a power-on-reset event has happened, and is cleared only if the user writes a “0” to this bit. The FAULT2 bit is the logic OR result of the fault bits in the FAULT2 register, which include FAULT8CK and OTSHDN. The FAULT8CK bit is set when the number of clock pulses in a SPI frame is not equal to a multiple of eight. The OTSHDN bit indicates that the device had a thermal shutdown fault. The FAULT2 bit, and the FAULT8CK and OTSHDN bits are cleared-on-read.

Enable bits in the FAULT1EN and FAULT2EN registers select which flags in the FAULT1 and FAULT2 registers asserts the $\overline{FAULT}$ pin. The enable bits do not affect the flags in the FAULT1 register, they only affect the $\overline{FAULT}$ pin. Figure 5 illustrates various register flags to assert the $\overline{FAULT}$ pin.

The STK bit in the GPO register configures the $\overline{FAULT}$ pin to be sticky or to clear when the fault is removed. For example: if a low voltage condition on V_{DD24} is detected, the 24VL bit in the FAULT1 register is set and $\overline{FAULT}$ asserts low provided bit 24VLE in the FAULT1EN register is set. If V_{DD24} then returns to normal levels, the 24VL bit in the FAULT1 register remains set until read; however the state of the $\overline{FAULT}$ pin depends on the configuration bit STK. If STK = 0, the $\overline{FAULT}$ pin is not sticky and clears when the fault goes away even though the 24VL bit remains set. If STK = 1, then the $\overline{FAULT}$ pin reflects the state of the bit in the FAULT1 register and remains set until the bit is cleared by reading the FAULT1 register. The minimum pulse width for $\overline{FAULT}$ pin asserting low is 1µs (typical). This ensures adequate time for the assertion of $\overline{FAULT}$ to be recognized by the host even if the fault was present for a shorter time.

The power-on default for the FAULT1EN register is to enable CRC and POR. The $\overline{FAULT}$ pin is in the non-sticky mode.

Clearing Bits in FAULT1 Register

The 24VL and 24VM sticky (or latched) bits in the FAULT1 register can be read and cleared either through a direct read of the FAULT1 register, or through a SPI Mode 0 or Mode 2 read or write command. If bit 24VF in the CFG register is equal to 0, SPI Mode 0 and 2 transactions read and clear bits 24VL and 24VM (Table 3). This valid SPI transaction also clears the CRC bit. Note that the CRC bit is only active in Mode 0 and 2 (M0 = 0) since this is the only time a CRC test is performed. The POR bit is only cleared when the user writes a “0” to it.

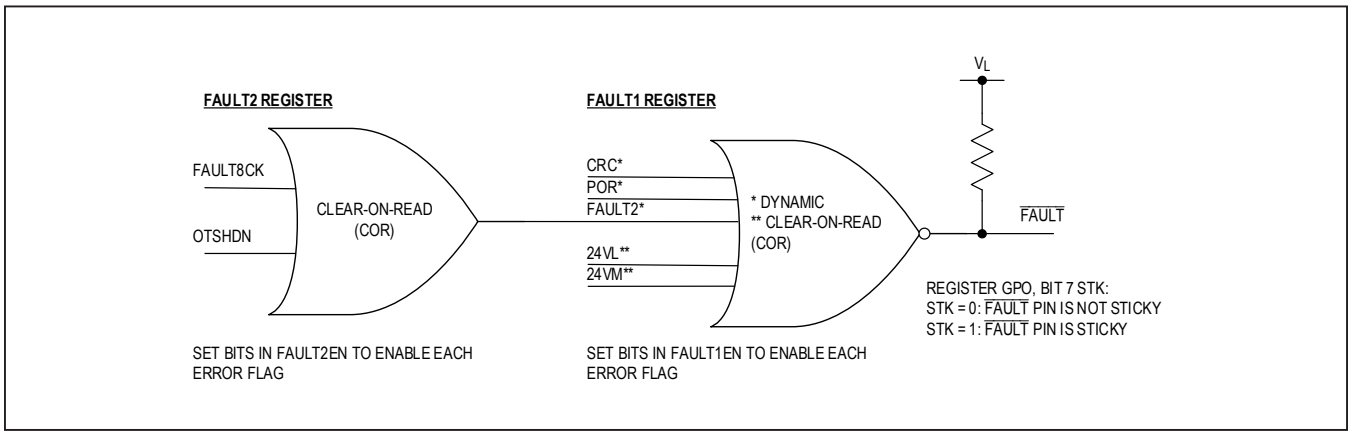


Figure 5. $\overline{FAULT}$ Output Sources

CRC Generation

In the SPI interface Mode 0 and 2, five CRC bits can be used to check the data integrity during transfers between the device and an external microcontroller. In applications where the integrity of data transferred is not of concern, the CRC bits can be disabled by operating in the SPI Mode 1 and 3 (M0 = 1). The CRC uses the following polynomial:

$$P(x) = x^5 + x^4 + x^2 + x^0$$

The 5-bit CRC value is calculated using the first 19 data bits padded with the 5-bit initial word 00111. The 5-bit CRC result is then appended to the original data bits to create the 24-bit SPI data frame. When the MAX22199 receives a data frame with a CRC error, the CRC error flag (CRC) in the FAULT1 register is set and, if CRCE is set, the $\overline{\text{FAULT}}$ pin is asserted. The CRC bit is not sticky, but does remain set until an error-free frame is received. SPI commands within a corrupted frame are ignored. Refer to **AN6798** for CRC algorithm programming example.

SPI Interface

The MAX22199 has an SPI compatible interface used to read input data, read diagnostic data, and configure all of the registers. Each configuration register can be read back to ensure proper configuration. The SPI interface supports direct mode or daisy-chain mode by setting M1 pin to low or high. The CRC error detection can be enabled or disabled by connecting M0 pin to GND or V_L (Table 1). Asserting $\overline{\text{CS}}$ low latches the state of all inputs and enables the SPI interface. For all modes, data at the SDI input is sampled on the rising edge of SCLK and data at SDO is updated on the falling edge of SCLK. The $\overline{\text{READ}}$/WRITE bit is always the first bit of the SPI frame. Transitions of SCLK while $\overline{\text{CS}}$ is deasserted (high) are ignored. SCLK must idle low when $\overline{\text{CS}}$ is asserted.

SPI Protocol

The serial output of the device adheres to the SPI protocol, running with CPHA = 0 and CPOL = 0, as shown in Figure 6. In all modes, the first 8 bits clocked out of SDO after $\overline{\text{CS}}$ is asserted are data bits showing the status of inputs IN8–IN1; this allows for rapid and convenient retrieval of the primary data. For write operations in Mode 0 and 1, the next 8 bits clocked out of SDO are zero. For reads in Mode 0 and 1, the second 8 bits are the data from the specified register.

Table 1. SPI Interface Modes

MODE	M1: M0	FRAME LENGTH	CRC	DAISY CHAIN
0	0 0	24-bit	Yes	No
1	0 1	16-bit	No	No
2	1 0	24-bit	Yes	Yes
3	1 1	16-bit	No	Yes

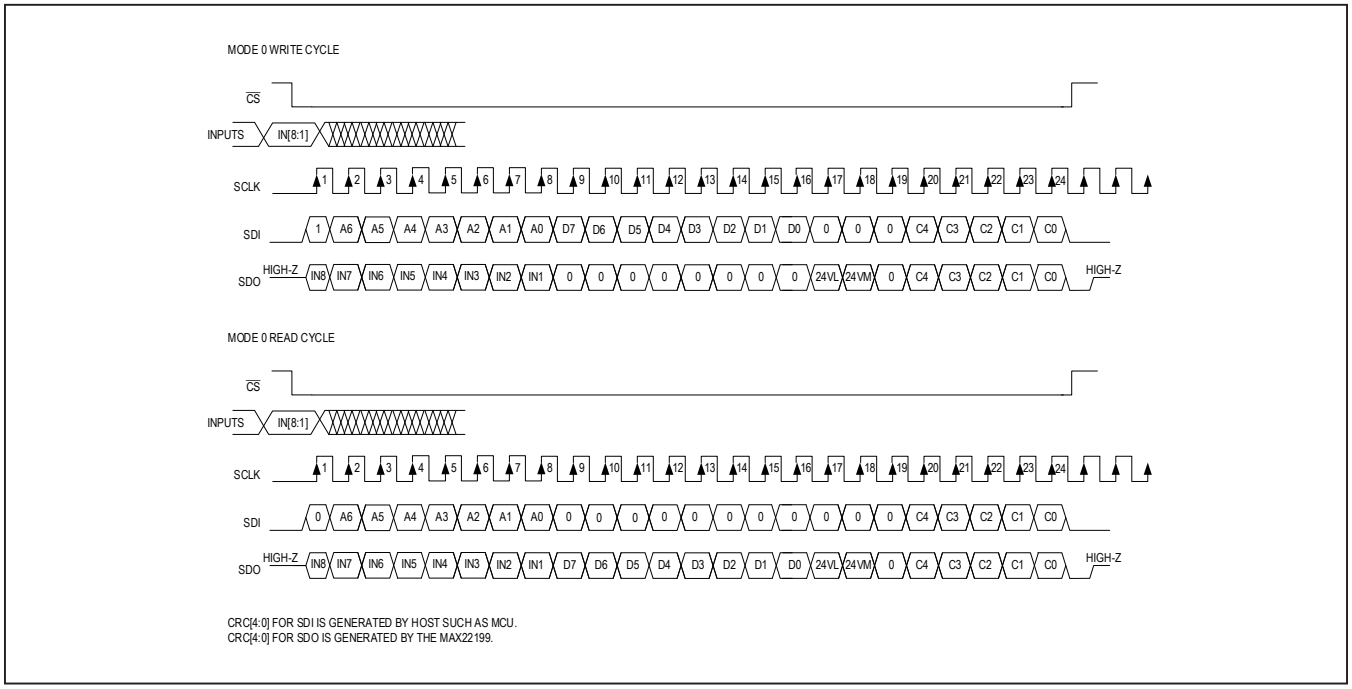


Figure 6. SPI Communication Example–Mode 0 Write and Read

Modes 2 and 3 are more complex, since the content of the second byte is determined by the previous instruction. For non-daisy-chain compatible modes (Mode 0 and 1), the read instruction is decoded on-the-fly as the SPI frame is clocked in. The instruction is immediately executed and data from the specified register is clocked out in the same SPI frame. This is convenient and quick, but not compatible with daisy-chaining. When daisy-chaining, each unit does not know which portion of the bit stream it should decode until $\overline{CS}$ is deasserted (the frame is finished). To accommodate this, all daisy-chainable read instructions require two SPI frames. The first frame contains the read instruction and register address, and the second frame returns the register data as the second byte of the frame. This is true regardless of the instruction being clocked in during the second frame. See Table 3 for detailed Mode 2 and 3 SPI commands.

$\overline{LATCH}$ is used to simultaneously capture the input states of different MAX22199s that are not controlled by the same $\overline{CS}$. This could be multiple MAX22199s in the same digital input module, or MAX22199s in different modules.

Clock Count for Multiples of 8

For each SPI cycle (between $\overline{CS}$ going low and going high), the device counts the number of SCLK pulses. If it is not a multiple of 8, the SPI input data is discarded and bit FAULT8CK is set in the FAULT2 register.

SPI Power Status

Only the SPI port buffers are powered from the V_L supply; internal SPI circuits are powered from the V_{DD} supply. Both V_{DD} and V_L must be valid for SPI communication to take place. In addition to powering the SPI circuits, V_{DD} also sustains the SPI memory (configuration and status registers). If power is being supplied through V_{DD24}, then an auxiliary supply for the memory is also available. The auxiliary supply only sustains memory, it does not allow SPI communication. The auxiliary supply takes over if V_{DD} is lost due to external loading or due to a thermal shutdown event. When the event is over, the device configuration is maintained and fault information is available in the FAULT registers. See Table 2 for the power requirement for SPI communication and register map configuration.

Daisy-Chain Modes

For systems with more than eight sensor inputs, multiple devices can be daisy-chained to allow access to all data inputs through a single serial port. When using a daisy-chain configuration, connect MOSI to SDI of the first device in the chain. Connect MISO to SDO of the last device in the chain. For all middle links, connect SDI to SDO of the previous device and SDO to SDI of the next device. $\overline{CS}$ and SCLK of all devices in the chain should be connected together in parallel, see Figure 7 which illustrates a 16-input application with daisy-chain connection and Figure 8, which shows SPI timing in the daisy-chain mode.

Table 2. SPI Port Power Status

V_{DD24}	V_{DD}	V_L	SPI REGISTER MAP CONFIGURATION	SPI PORT COMMUNICATION
Valid	Valid	Valid	Configuration and fault data maintained	Normal Operation
Not Valid	Valid	Valid	Configuration and fault data maintained	Normal Operation
Valid	Not Valid	X	Configuration and fault data maintained	$\overline{CS}$ ignored, SDO is High-Z
X	Valid	Not Valid	Configuration and fault data maintained	$\overline{CS}$ ignored, SDO is High-Z
Not Valid	Not Valid	X	Configuration and fault data lost	$\overline{CS}$ ignored, SDO is High-Z

Note: X = Don't Care

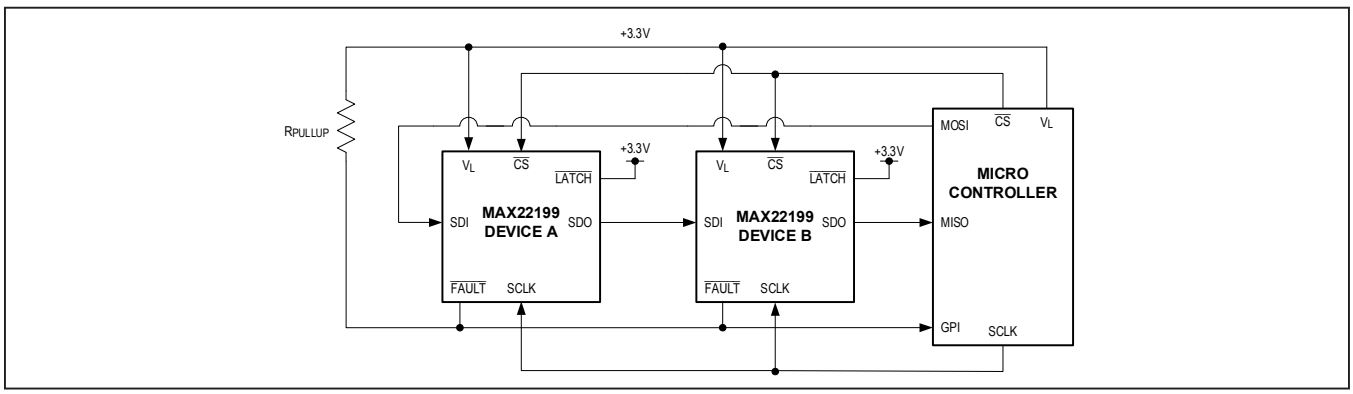


Figure 7. SPI Daisy-Chain Connection

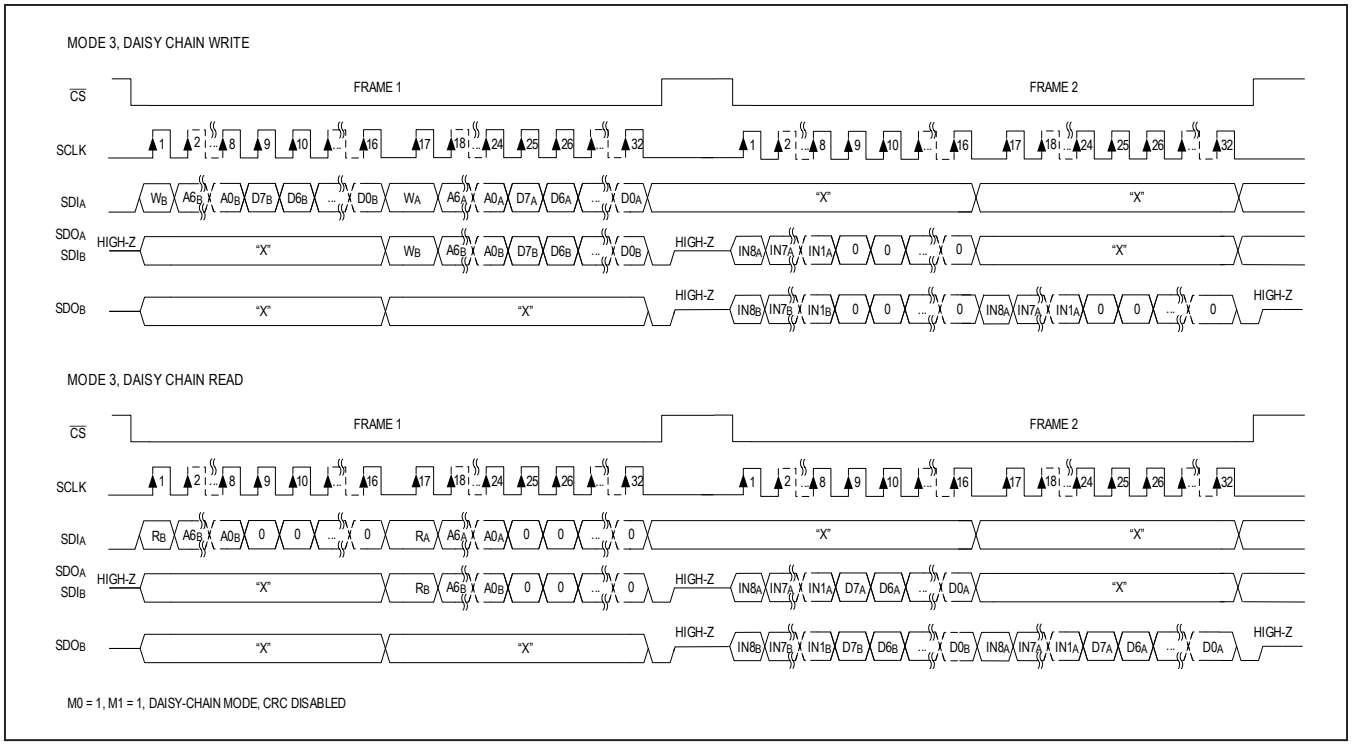


Figure 8. SPI Daisy-Chain Communication Example–Mode 3 Write and Read

Configuration Flowchart

The MAX22199 powers on with default register settings and can be used in the default mode to read the data inputs, or it can be configured to match the individual application requirements. Before any register access for configuration or reading data, the MCU needs to wait until $\overline{\text{READY}}$ goes low indicating that the MAX22199 is powered up and ready for use. Next, the MCU needs to clear the $\overline{\text{FAULT}}$ pin that asserts low after every power-up event due to the default state (high) of the POR flag.

Default Mode (Power-up mode): In this mode, all input channel filters (FLT_ registers) are set to bypass mode, all input channels are enabled, and all fault sources are disabled on $\overline{\text{FAULT}}$ pin except the CRC and POR flags. Upon power-up, the POR flag is set to 1. If the $\overline{\text{FAULT}}$ pin is being used, then a write operation must be performed to the FAULT1 register to reset POR to 0 for normal operating conditions. Now the MAX22199 can be polled to read data from DI register to show the logic state of the 8 input channels.

Configurable Mode: The MAX22199 can be configured for different parameters based upon the application requirements. The MCU can write to the various registers to set the options for input channel filters, enabling different fault sources on the $\overline{\text{FAULT}}$ pin, or disabling specific input channels. In addition, the user can enable features such as making $\overline{\text{FAULT}}$ pin sticky or not. Once the configuration is complete, the MAX22199 can be polled to read from DI register to show the logic state of the 8 input channels. Figure 9 demonstrates an example to configure the MAX22199.

$\overline{\text{FAULT}}$ Asserted: The MAX22199 uses the open-drain $\overline{\text{FAULT}}$ pin to indicate to the MCU that a fault has occurred, often by using this pin to trigger an interrupt function within the MCU. The MCU can determine the source of the fault by reading regsiter FAULT1. If bit 5 of FAULT1 is set, then register FAULT2 is indicating a fault and the FAULT2 register must also be read. Reading the FAULT_ register clears the fault flag unless the fault condition persists, which immediately resets the flag.

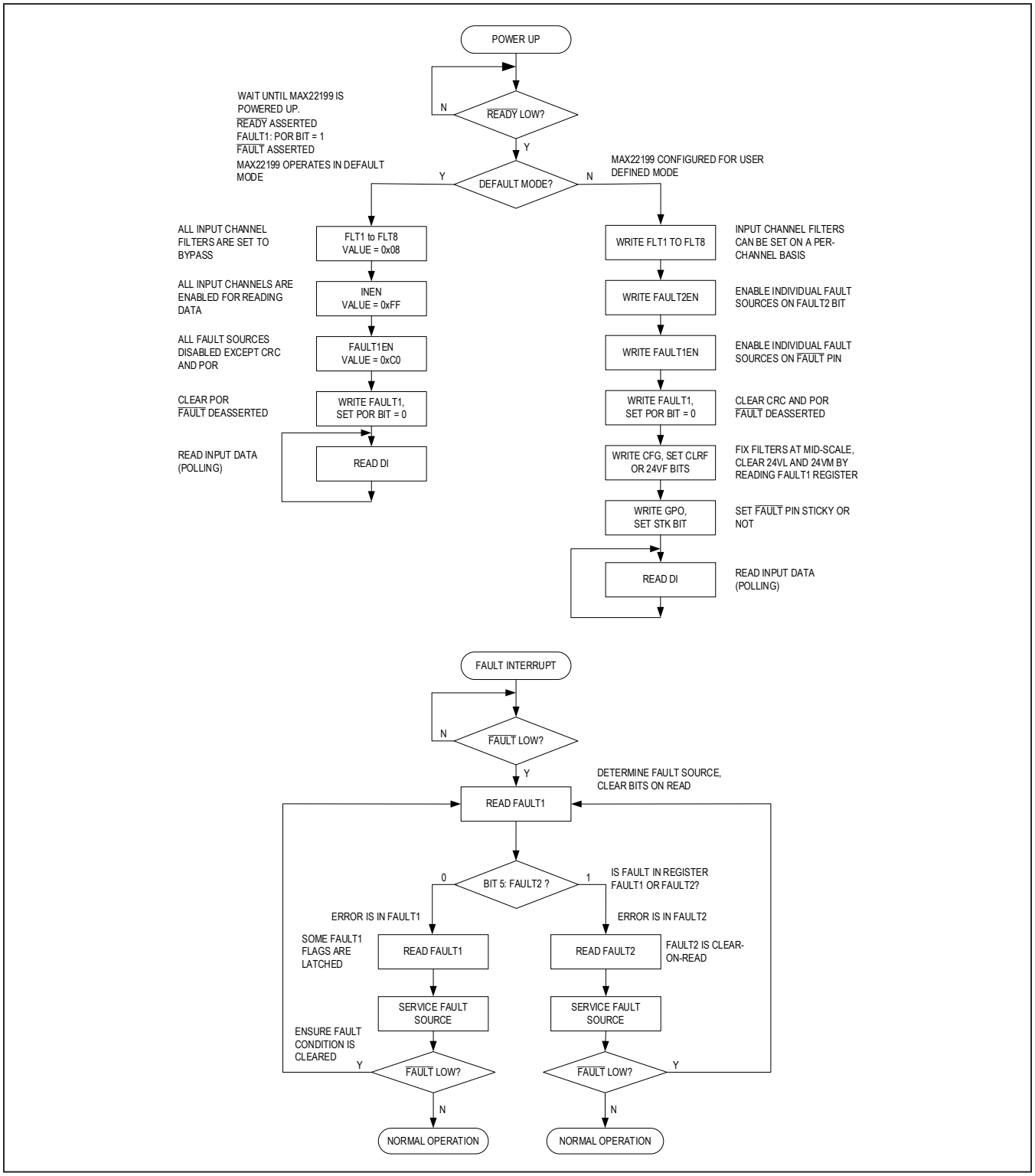


Figure 9. MAX22199 Configuration Flowchart

Table 3. SPI Frames for SPI Modes

Mode 0: M1 = 0, M0 = 0 (CRC Enabled, SPI Direct Mode)

Write

SDI	MSB = 1 1 bit	Register Address 7 bits	Write Data 8 bits	000 Fill Data 3 its			CRC from Host 5 bits
SDO	Input data: IN8–IN1 8 bits		00000000 Fill Data 8 bits	24VL	24VM	0	CRC from MAX22199 5 bits

Read

SDI	MSB = 0 1 bit	Register Address 7 bits	00000000 Fill Data 8 bits	000 Fill Data 3 bits			CRC from Host 5 bits
SDO	Input data: IN8–IN1 8 bits		Register Data: D7–D0 8 bits	24VL	24VM	0	CRC from MAX22199 5 bits

Mode 1: M1 = 0, M0 = 1 (CRC Disabled, SPI Direct Mode)

Write

SDI	MSB = 1 1 bit	Register Address 7 bits	Write Data 8 bits
SDO	Input data: IN8–IN1 8 bits		00000000 Fill Data 8 bits

Read

SDI	MSB = 0 1 bit	Register Address 7 bits	00000000 Fill Data 8 bits
SDO	Input data: IN8–IN1 8 bits		Register Data: D7–D0 8 bits

Mode 2: M1 = 1, M0 = 0 (CRC Enabled, Daisy-Chain Mode)

Write – Preceding frame was a write or no-op

SDI	MSB = 1 1 bit	Register Address 7 bits	Write Data 8 bits	000 Fill Data 3 bits			CRC from Host 5 bits
SDO	Input data: IN8–IN1 8 bits		00000000 Fill Data 8 bits	24VL	24VM	0	CRC from MAX22199 5 bits

Write – Preceding frame was a read

SDI	MSB = 1 1 bit	Register Address 7 bits	Write Data 8 bits	000 Fill Data 3 bits			CRC from Host 5 bits
SDO	Input data: IN8–IN1 8 bits		Register Data: D7–D0 8 bits	24VL	24VM	0	CRC from MAX22199 5 bits

Read – Preceding frame was a write or no-op

SDI	MSB = 0 1 bit	Register Address 7 bits	00000000 Fill Data 8 bits	000 Fill Data 3 bits			CRC from Host 5 bits
SDO	Input data: IN8–IN1 8 bits		00000000 Fill Data 8 bits	24VL	24VM	0	CRC from MAX22199 5 bits

Table 3: SPI Frames for SPI Modes (continued)

Read – Preceding frame was a read

SDI	MSB = 0 1 bit	Register Address 7 bits	00000000 Fill Data 8 bits	000 Fill Data 3 bits			CRC from Host 5 bits
SDO	Input data: IN8–IN1 8 bits		Register Data: D7–D0 8 bits	24VL	24VM	0	CRC from MAX22199 5 bits

Mode 3: M1 = 1, M0 = 1 (CRC Disabled, Daisy-Chain Mode)

Write – Preceding frame was a write or no-op

SDI	MSB = 1 1 bit	Register Address 7 bits	Write Data 8 bits
SDO	Input data: IN8–IN1 8 bits		00000000 Fill Data 8 bits

Write – Preceding frame was a read

SDI	MSB = 1 1 bit	Register Address 7 bits	Write Data 8 bits
SDO	Input data: IN8–IN1 8 bits		Register Data: D7–D0 8 bits

Read – Preceding frame was a write or no-op

SDI	MSB = 0 1 bit	Register Address 7 bits	00000000 Fill Data 8 bits
SDO	Input data: IN8–IN1 8 bits		00000000 Fill Data 8 bits

Read – Preceding frame was a read

SDI	MSB = 0 1 bit	Register Address 7 bits	00000000 Fill Data 8 bits
SDO	Input data: IN8–IN1 8 bits		Register Data: D7–D0 8 bits

Notes:

SDI – CRC generated by external device such as MCU; data D7–D0 clocked out from MCU

SDO – CRC generated by the MAX22199; data D7–D0 clocked out from the MAX22199 register

NO-OP – No Operation, i.e. write cycle with no valid data to specified address

Write Cycle – DI8–DI1 are from internal latches, whose outputs are frozen when $\overline{CS}$ or $\overline{LATCH}$ goes low. Bits 24VL and 24VM are frozen by $\overline{CS}$ going low but not by $\overline{LATCH}$.

Read Cycle – D7–D0 are the register data addressed through SDI. Bits 24VL and 24VM reflect the corresponding bits in the FAULT1 register.

In mode 1 and mode 3, $\overline{CS}$ can be deasserted after eight clock cycles to retreive the input data in a single-byte SPI command. The read or write command is ignored in this case.

Table 4. Register Map

REGISTER	ADDRESS	SYMBOL	TYPE	POR (DEFAULT)	7	6	5	4	3	2	1	0
Digital Input	02h	DI	R	00h	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1
Fault 1	04h	FAULT1	MIXED	46h	CRC	POR	FAULT2	0	0	24VL	24VM	0
Filter IN1	06h	FLT1	RW	08h	0	0	0	X	FBP1	DELAY1[2:0]		
Filter IN2	08h	FLT2	RW	08h	0	0	0	X	FBP2	DELAY2[2:0]		
Filter IN3	0Ah	FLT3	RW	08h	0	0	0	X	FBP3	DELAY3[2:0]		
Filter IN4	0Ch	FLT4	RW	08h	0	0	0	X	FBP4	DELAY4[2:0]		
Filter IN5	0Eh	FLT5	RW	08h	0	0	0	X	FBP5	DELAY5[2:0]		
Filter IN6	10h	FLT6	RW	08h	0	0	0	X	FBP6	DELAY6[2:0]		
Filter IN7	12h	FLT7	RW	08h	0	0	0	X	FBP7	DELAY7[2:0]		
Filter IN8	14h	FLT8	RW	08h	0	0	0	X	FBP8	DELAY8[2:0]		
Configuration	18h	CFG	RW	00h	0	0	0	24VF	CLRF	0	0	X
Input Enable	1Ah	INEN	RW	FFh	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1
Fault 2	1Ch	FAULT2	COR	00h	0	0	FAULT8CK	OTSHDN	0	0	0	0
Fault 2 Enables	1Eh	FAULT2EN	RW	00h	0	0	FAULT8CKE	OTSHDNE	X	X	X	X
GPO	22h	GPO	RW	00h	STK	0	0	0	0	0	0	0
Fault 1 Enables	24h	FAULT1EN	RW	C0h	CRCE	PORE	FAULT2E	X	X	24VLE	24VME	X
No-Op	26h	NOP	NA	–	Dummy register. Contents of register DI are clocked out normally during attempted SPI writes to this register. Useful for daisy-chain mode.							

Register Type Legend:

R: Read only
RW: Read and Write
COR: Clear-On-Read
MIXED: Some bits are Clear-On-Read type, others are cleared differently. See bit descriptions for details.
X: Don’t care. Can be written as 1 or 0.

Register Detailed Description

DI (Read)

Address = 0x02

Default = 0x00

BIT	NAME	DESCRIPTION
7:0	DI8 – DI1	0: Channel x is driven low 1: Channel x is driven high Digital input state. DI_ is the state of the corresponding input pin.

FAULT1 (Mixed)

Address = 0x04

Default = 0x46

BIT	NAME	DESCRIPTION
7	CRC	0: The last received SPI frame was not corrupted. 1: The last received SPI frame was corrupted. It is not cleared upon read, but when an uncorrupted SPI frame is received. CRC is only active in SPI interface Mode 0 and 2.
6	POR	0: Normal operating conditions 1: POR event has reset the register map to its power-on-reset state This bit is cleared only if the user writes “0” to it. Other bits in this register are unaffected by the write access.
5	FAULT2	0: All enabled bits in the FAULT2 register are not set 1: An enabled bit in the FAULT2 register is set This bit is cleared on read only if the FAULT2 register is cleared or the bit is disabled.
4:3	0	Reserved
2	24VL*	0: 24V supply is normal (above the 24VL threshold) 1: 24V supply is low (below the 24VL threshold) Cleared upon reading this register. If bit 4 in the CFG register (24VF) is 0, 24VL can also be cleared after any SPI transaction while operation in Mode 0 or 2.
1	24VM*	0: 24V supply is normal (above the 24VM threshold) 1: 24V supply is missing (below the 24VM threshold) Cleared upon reading this register. If bit 4 in the CFG register (24VF) is 0, 24VM can also be cleared after any SPI transaction while operation in Mode 0 or 2.
0	0	Reserved

**These flags are latched and they remain set until read even if the fault goes away, and are not cleared if the fault condition is still present when the register is read.*

FLT1 to FLT8 (Read/Write)

Address = 0x06 – 0x14 (increments of 2)

Default = 0x08

BIT	NAME	DESCRIPTION
7:5	0	Reserved
4	X	Don't care. Can be written as 1 or 0
3	FBP_	FBP1 to FBP8. 0: Programmable filter on IN_ is used 1: Programmable filter on IN_ is bypassed
2:0	DELAY_ [2:0]	DELAY1 to DELAY8. Programmable filter values for IN_: DELAY_[2:0] = 000 = 50µs DELAY_[2:0] = 001 = 100µs DELAY_[2:0] = 010 = 400µs DELAY_[2:0] = 011 = 800µs DELAY_[2:0] = 100 = 1.6ms DELAY_[2:0] = 101 = 3.2ms DELAY_[2:0] = 110 = 12.8ms DELAY_[2:0] = 111 = 20ms

CFG (Read/Write)

Address = 0x18

Default = 0x00

BIT	NAME	DESCRIPTION
7:5	0	Reserved
4	24VF	0: Flags 24VL and 24VM are cleared after any full frame SPI transaction or by reading the FAULT1 register 1: 24VL and 24VM are cleared only by reading the FAULT1 register Only affects SPI Mode 0 and 2.
3	CLRF	0: All input filters operate normally 1: All input filters are fixed at the mid-scale value for the chosen delay The filters resume normal operation when CLRF is cleared.
2:1	0	Reserved
0	X	Don't care. Can be written as 1 or 0

INEN (Read/Write)

Address = 0x1A

Default = 0xFF

BIT	NAME	DESCRIPTION
7:0	EN8 – EN1	0: EN_ = 0, IN_ is disabled, the current source is set to 0mA, and the DI_ bit in the DI register is set to 0 1: EN_ = 1, IN_ is enabled

FAULT2 (Clear-On-Read)

Address = 0x1C

Default = 0x00

BIT	NAME	DESCRIPTION
7:6	0	Reserved
5	FAULT8CK	0: SPI receives a number of clock pulses equal to a multiple of eight, valid transaction 1: SPI receives a number of clock pulses not equal to a multiple of eight, the SPI command is rejected
4	OTSHDN	0: Normal operating conditions 1: Overtemperature shutdown (the safe operating temperature 165°C typical has been exceeded) Overtemperature Shutdown: all inputs and LED drivers are turned off to reduce power dissipation and protect the device. The SPI interface and internal regulator remain active and if the temperature continues to rise, the regulator is turned off.
3:0	0	Reserved

FAULT2EN (Read/Write)

Address = 0x1E

Default = 0x00

BIT	NAME	DESCRIPTION
7:6	0	Reserved
5	FAULT8CKE	0: Disable bit FAULT2 in FAULT1 register 1: Enable bit FAULT2 in FAULT1 register to be set when FAULT8CK is high
4	OTSHDNE	0: Disable bit FAULT2 in FAULT1 register 1: Enable bit FAULT2 in FAULT1 register to be set when OTSHDN is high
3:0	X	Don’t care. Can be written as 1 or 0

GPO (Read/Write)

Address = 0x22

Default = 0x00

BIT	NAME	DESCRIPTION
7	STK	0: $\overline{\text{FAULT}}$ pin is not sticky. $\overline{\text{FAULT}}$ condition is determined by the logical OR of the unmasked real-time FAULT1 register sources, and not the FAULT1 register bits. 1: $\overline{\text{FAULT}}$ pin is sticky. If at least one bit in the FAULT1 register is set and unmasked, $\overline{\text{FAULT}}$ pin remains low until FAULT1 register is read (Figure 5).
6:0	0	Reserved

FAULT1EN (Read/Write)

Address = 0x24

Default = 0xC0

BIT	NAME	DESCRIPTION
7	CRCE	0: $\overline{\text{FAULT}}$ pin is not asserted when CRC is 1 1: $\overline{\text{FAULT}}$ pin is asserted when CRC is 1
6	PORE	0: $\overline{\text{FAULT}}$ pin is not asserted when POR is 1 1: $\overline{\text{FAULT}}$ pin is asserted when POR is 1
5	FAULT2E	0: $\overline{\text{FAULT}}$ pin is not asserted when FAULT2 is 1 1: $\overline{\text{FAULT}}$ pin is asserted when FAULT2 is 1
4:3	X	Don't care. Can be written as 1 or 0
2	24VLE	0: $\overline{\text{FAULT}}$ pin is not asserted when 24VL is 1 1: $\overline{\text{FAULT}}$ pin is asserted when 24VL is 1
1	24VME	0: $\overline{\text{FAULT}}$ pin is not asserted when 24VM is 1 1: $\overline{\text{FAULT}}$ pin is asserted when 24VM is 1
0	X	Don't care. Can be written as 1 or 0

NOP (N/A)

Address = 0x26

Default = N/A

BIT	NAME	DESCRIPTION
7:0	NOP[7:0]	Dummy register. DI8–DI1 bits are clocked out normally during attempted writes to this register. Useful for daisy-chain mode.

Applications Information

Power Supply Sequencing

The MAX22199 does not require special power supply sequencing. The SPI interface logic level (V_L) is set independently from the field supply (V_{DD24}) or LDO output (V_{DD}) levels.

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DD24}, V_L, and V_{DD} with 0.1µF || 1µF ceramic capacitors to GND, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

Powering the MAX22199 With the V_{DD} Pin

The MAX22199 can alternatively be powered using a 3.0–5.5V supply connected to the V_{DD} pin. In this case a 24V supply is no longer needed and the V_{DD24} pin must be left unconnected. This configuration has lower power consumption and heat dissipation since the on-chip LDO voltage regulator is disabled (the V_{DD24} undervoltage lockout is below threshold and automatically disables the LDO).

In this configuration, the device always indicates a 24V FAULT due to bits 24VL and 24VM in the FAULT1 register, and the $\overline{FAULT}$ pin is always active (low) if the bits are enabled in the FAULT1EN register. To overcome this, set bits 24VLE and 24VME in the FAULT1EN register to 0.

PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the entire EP area with multiple thermal vias for best thermal performance.
- In order to achieve the optimal EFT performance, it is recommended to have the GND plane around the REFDI trace, and isolate the REFDI trace from all input traces as much as possible.

Isolating the SPI Interface

A companion product, the MAX14483 is available, which is optimized to support the MAX22199. The MAX14483 is a 6-channel, 3.75kV_{RMS}, low-power digital isolator ideal for interfacing to low-voltage products such as microcontrollers or FPGAs. Figure 10 demonstrates daisy-chain operation, showing SPI signals, control signals, and power monitoring signals isolated between the field and logic side of the design. A single MAX14483 can be used for multiple MAX22199s.

Figure 11 demonstrates two MAX22199s connected as independent slaves, meaning they have separate chip select ($\overline{CS}$) signals from the master (MCU). The AUX channel of the MAX14483 can be used to isolate the second $\overline{CS}$ signal. Care must be taken to ensure both MAX22199s are not enabled simultaneously to avoid SPI-bus contention.

In both Figure 10 and Figure 11, the $\overline{READY}$ signal from both MAX22199 devices are connected together to the $\overline{IRDY}$ pin of the MAX14483. The $\overline{IRDY}$ is pulled low when one of the MAX22199 devices is ready for operation. Care must be taken with the software to determine if both of the MAX22199s are ready. Alternatively, an OR gate can be used between $\overline{READY}$ signals to guarantee the $\overline{IRDY}$ is only pulled low when both the $\overline{READY}$ signals are low.

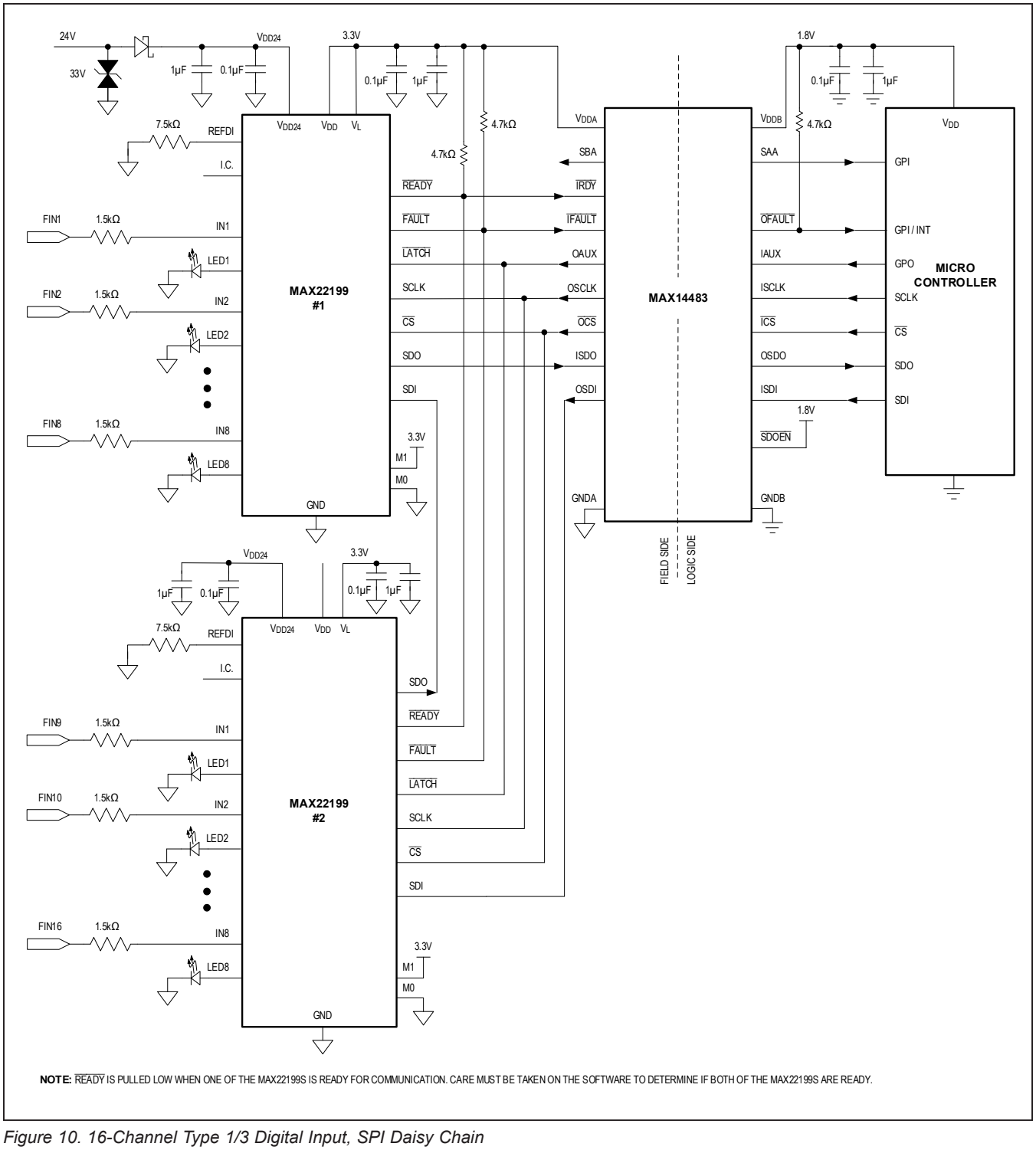


Figure 10. 16-Channel Type 1/3 Digital Input, SPI Daisy Chain

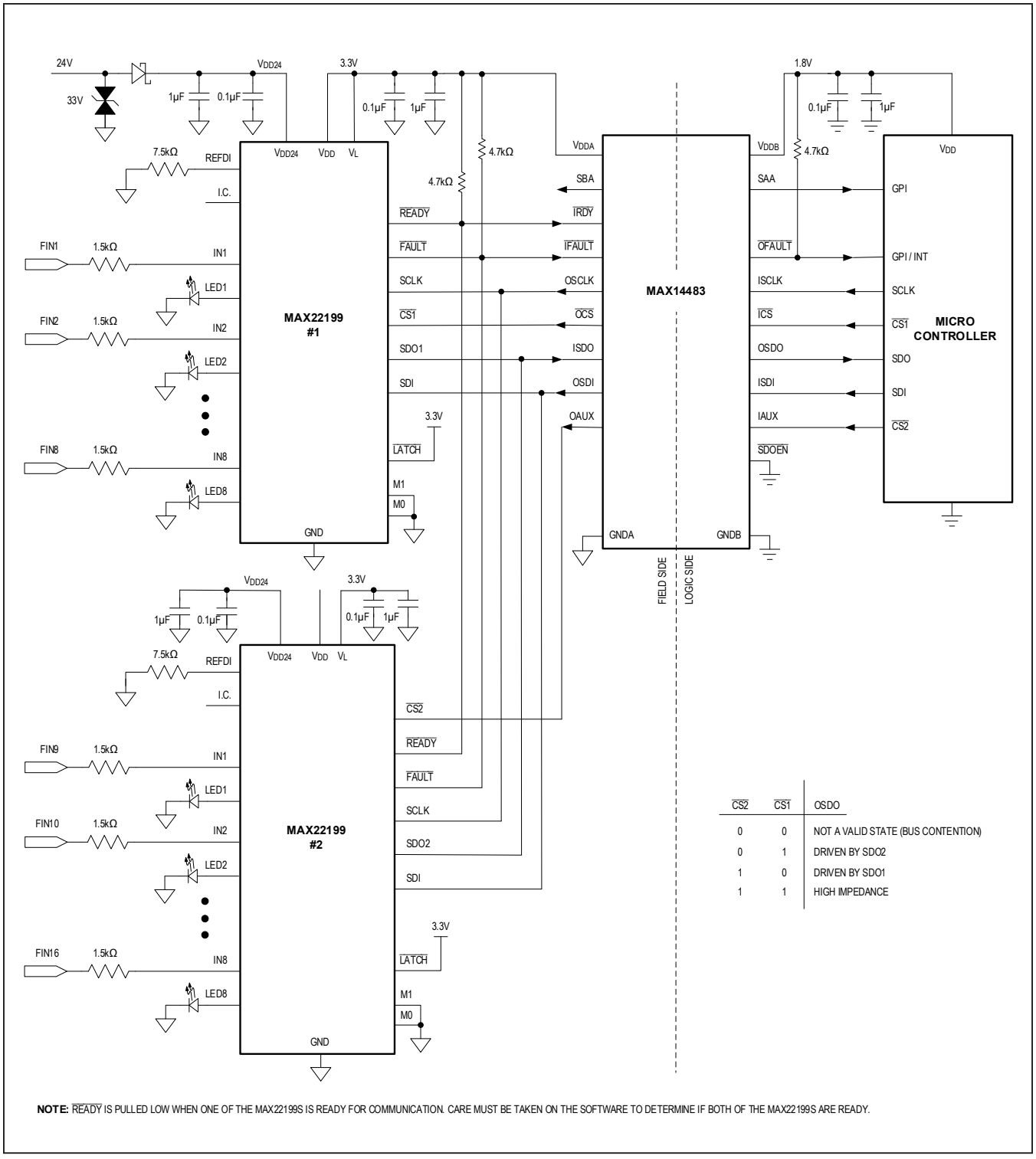


Figure 11. 16-Channel Type 1/3 Digital Input, Independent Slave SPI (Separate $\overline{CS}$ for Each SPI Slave)

IEC 61131-2 EMC Requirement

The MAX22199 is required to operate reliably in harsh industrial environments. The device can meet the transient immunity requirements as specified in IEC 61131-2, including Electrostatic Discharge (ESD) per IEC 61000-4-2, Electrical Fast Transient/Burst (EFT) per IEC 61000-4-4, and Surge Immunity per IEC 61000-4-5. Maxim's proprietary process technology provides robust input channels and field supply with internal ESD structures and high Absolute Maximum Ratings (see the *Absolute Maximum Ratings* section), but external components are also required to absorb excessive energy from ESD and surge transients. The circuit with external components shown in Figure 12 allows the device to meet and exceed the transient immunity requirements as specified in IEC 61131-2 and related IEC 61000-4-x standards. The system shown in Figure 12, using the components shown in Table 5, is designed to be robust against ESD, EFT, and Surge specifications as listed in Table 6. In all these tests, the part or DUT is soldered onto a properly designed application board (e.g., the MAX22199EVKIT#) with necessary external components.

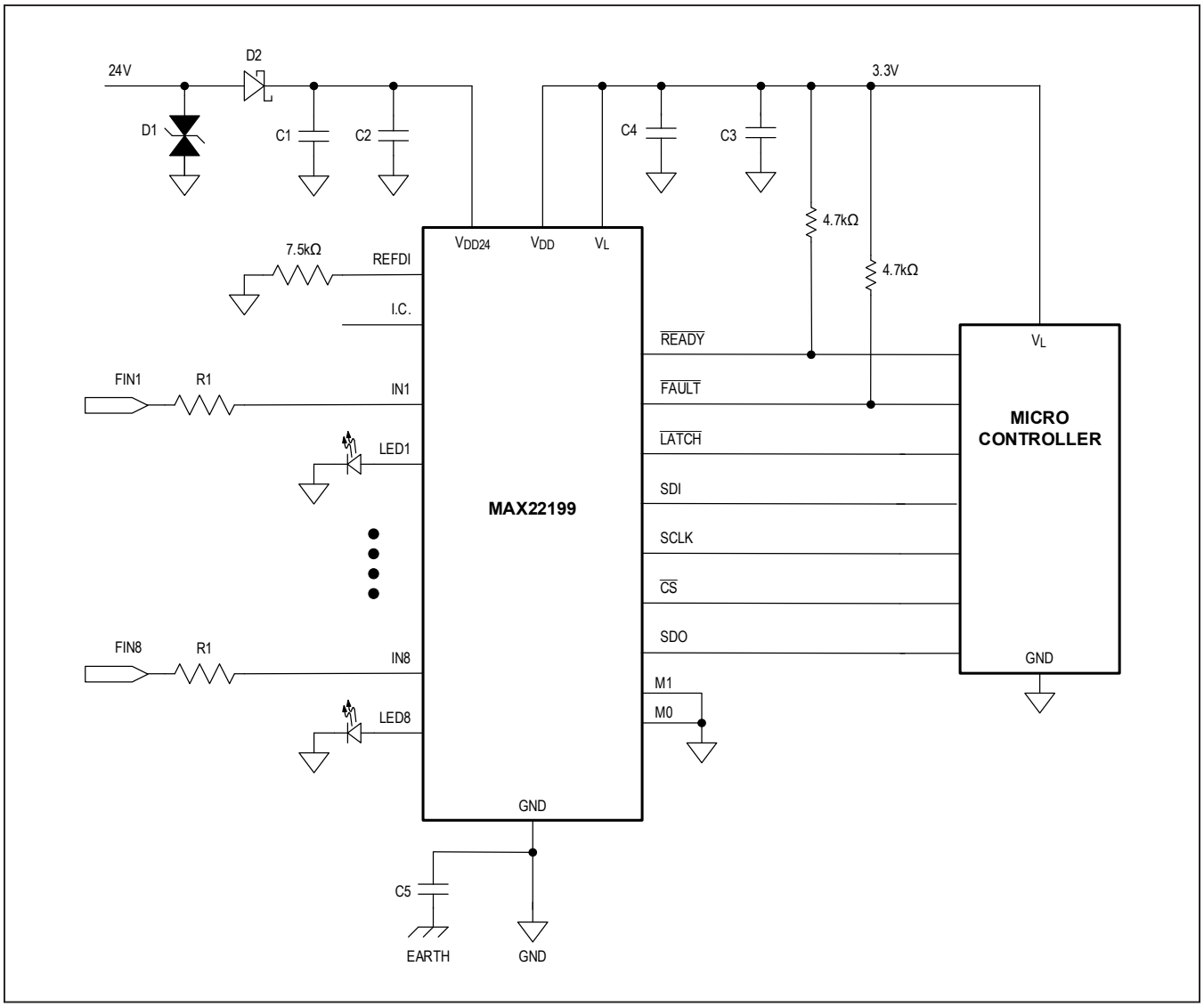


Figure 12. Typical EMC Protection Circuitry for the MAX22199

Table 5. Recommended Components

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED/OPTIONAL
C1	1µF, 100V low ESR ceramic capacitor	Required
C2	0.1µF, 100V low ESR ceramic capacitor	Required
C3	1µF, 10V low ESR ceramic capacitor	Required
C4	0.1µF, 10V low ESR ceramic capacitor	Required
C5	3300pF safety rated Y capacitor (2220)	Recommended
D1	Bidirectional TVS diode, SMAJ33CA (42Ω) or SM30T39CAY (2Ω)	Recommended
D2	Schottky diode for reverse current protection	Recommended
R1	1.5kΩ or 1kΩ, 1W pulse withstanding resistor (CMB0207, RPC2512, CRCW2512-IF or similar)	Required
All other resistors	0603, 0.1W resistors	Required
All LEDs	LED for visual input status indication	Recommended

ESD Protection of Field Inputs

The input resistor limits the energy into the MAX22199 IN_ pins and protects the internal ESD structure from excessive transient energy. An input series resistor is required and should be rated to withstand such ESD levels. The MAX22199 input channels can withstand up to ±8kV ESD contact discharge and ±15kV ESD air-gap discharge with an input series resistor of 1kΩ or larger. The input resistor value shifts the field voltage switching threshold scaled by the input current; thus, it determines the input characteristics of the application. The package of the resistor should be large enough to prevent the arcing across the two resistor pads. Arcing depends on the ESD level applied to the field input and the application's pollution degree.

EFT Protection of Field Inputs

The input channels can withstand up to ±4kV, 5kHz or 100kHz fast transients (Figure 14) with performance criterion A, normal operation within specification limits. A capacitive coupling clamp is used to couple the fast transients (burst) from the EFT generator to the field inputs of the MAX22199 without any galvanic connection to the MAX22199 input pins.

Surge Protection of Field Inputs

In order to protect the IN_ pins against IEC 61000-4-5 surges (Figure 15 and Figure 16), two options exist. The first option is to use a series pulse withstanding resistor as shown in the various application diagrams in the data sheet. A pulse resistor greater or equal to 1kΩ should be used to withstand ±2kV/42Ω, 1.2/50µs surge pulses. The pulse resistor should support dissipation of the surge energy. Examples of suitable resistors are CMB0207 MELF, RPC2512 or CRCW2512-IF thick film as well as others. The required resistor value is defined by the Type 1, 2, 3, or other input characteristics. Capacitors for filtering should not be connected to the IN_ pins.

The second option, which can result in a smaller overall footprint, is to use a bidirectional TVS to GND at the field input with a low-power series resistor, greater or equal to 1kΩ (Figure 17). The TVS must be able to absorb the surge energy and has the function of limiting the peak voltage so that the resistor only sees a low differential voltage. Suitable TVS include SMAJ33CA, SPT02-236 or PDFN3-32 which has a smaller footprint, offering protection against ±1kV/42Ω surges.

Surge Protection of 24V Supply

In order to protect the V_{DD24} pin against 500V/42Ω, 1.2/50µs surges (Figure 15), a SMAJ33CA TVS can be applied to the V_{DD24} pin, along with a series Schottky diode for reverse current protection.

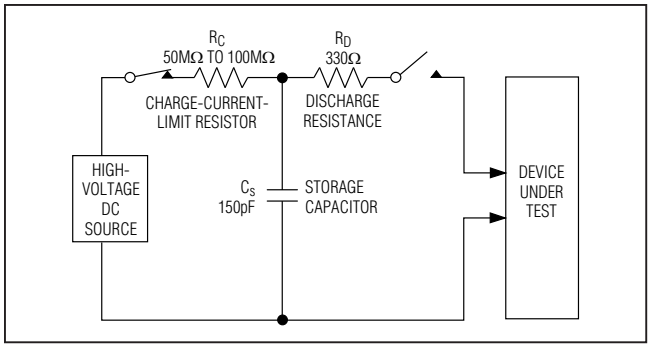


Figure 13a. ESD Test Circuit

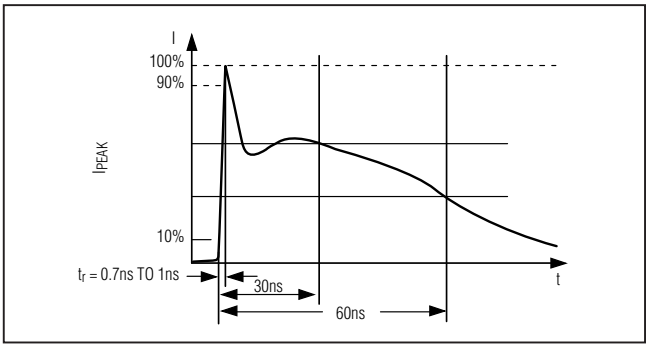


Figure 13b. ESD Contact Discharge Test Waveform

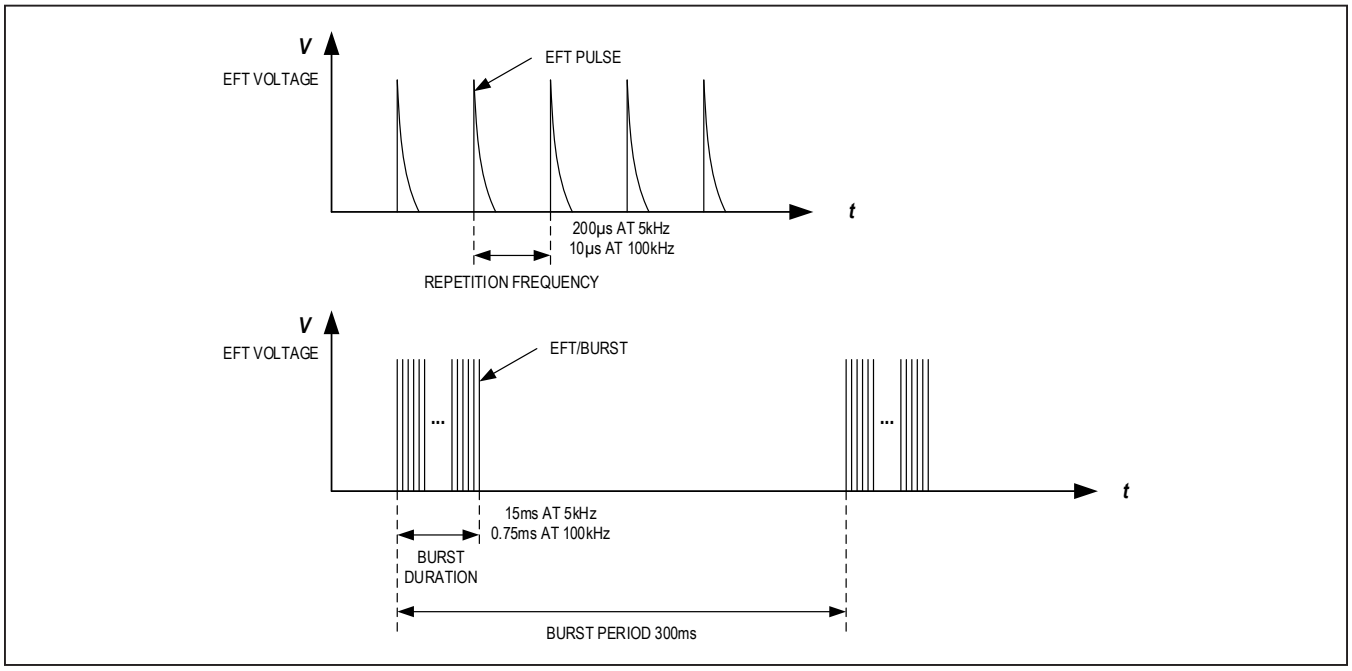


Figure 14. Electrical Fast Transient/Burst Waveform

Table 6. Transient Immunity Test Results

TEST		RESULT
IEC 61000-4-2 Electrostatic Discharge (ESD)	Contact ESD	±8kV
	Air-Gap ESD	±15kV
IEC 61000-4-4 Electrical Fast Transient/Burst (EFT)	Input Line	±4kV
IEC 61000-4-5 Surge Immunity (1.2/50µs, 42Ω)	Line-to-Ground	±2kV
	Line-to-Line	±2kV
	Power Supply	±500V

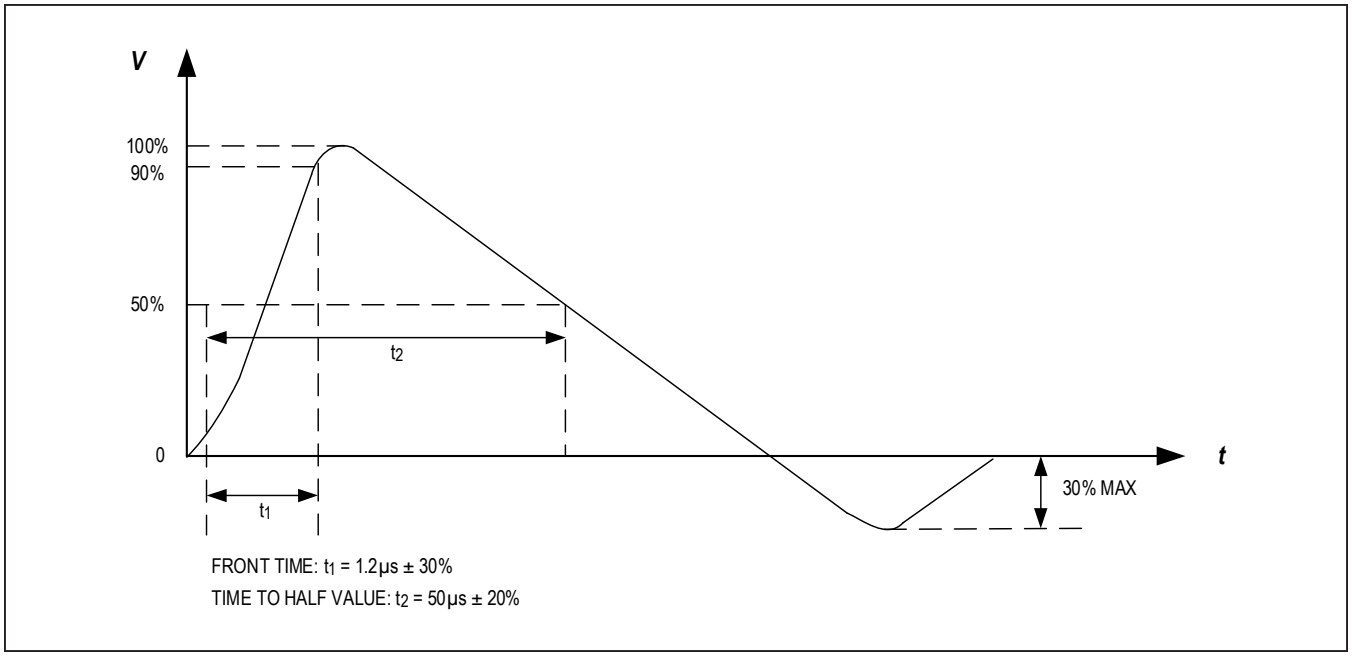


Figure 15. 1.2/50µs Surge Voltage Waveform

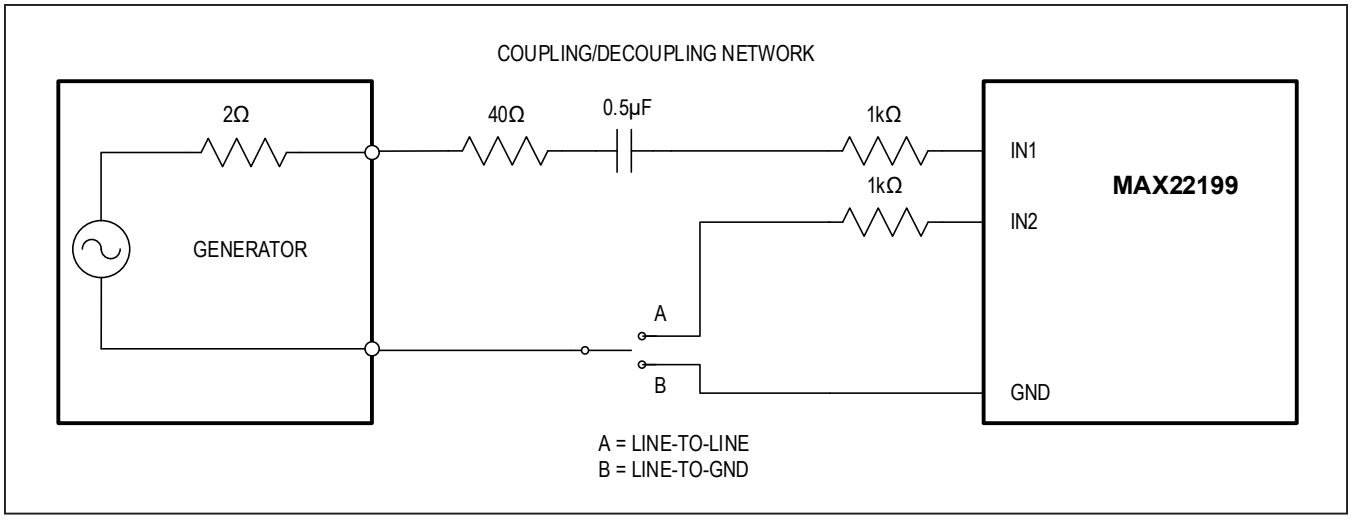


Figure 16. Surge Testing Methods

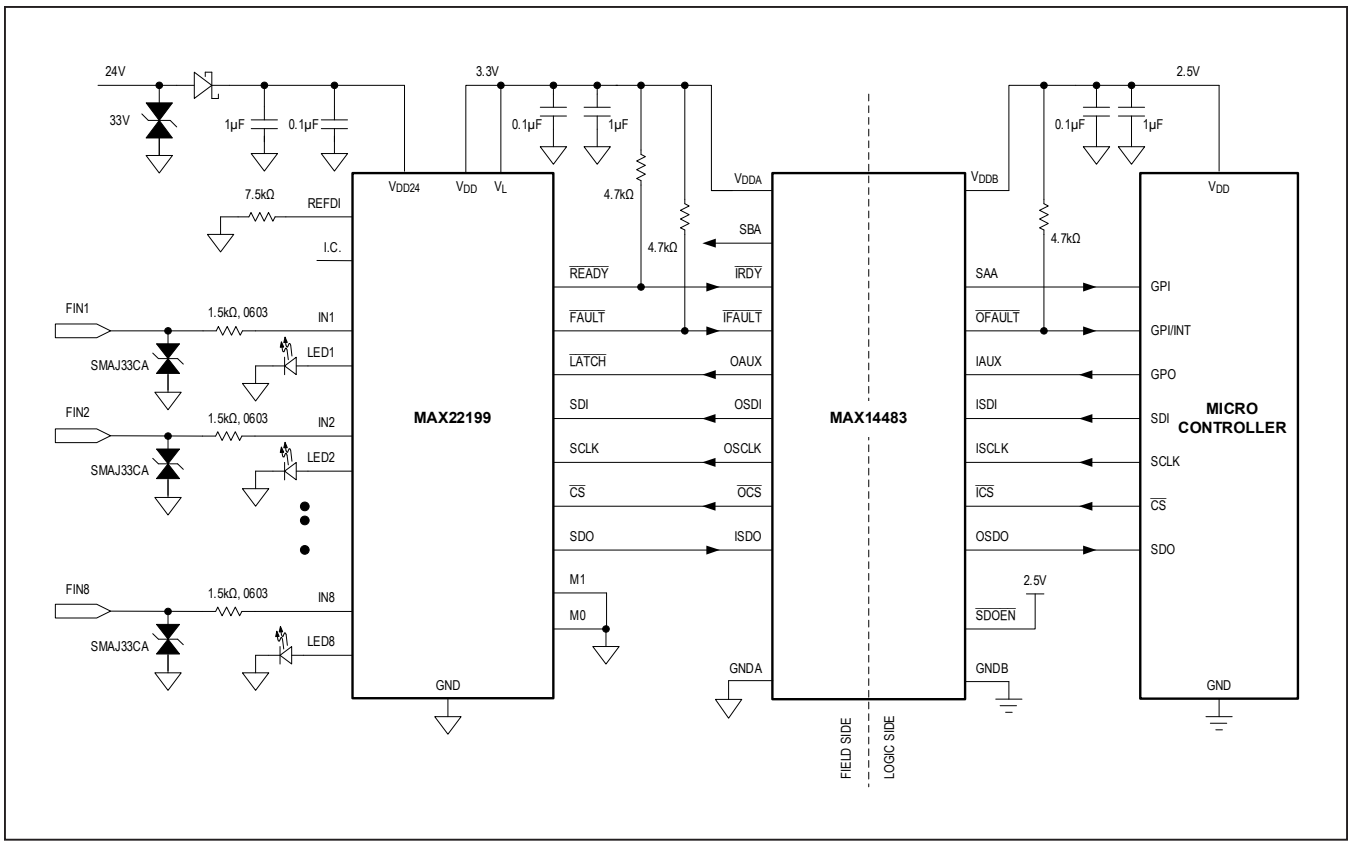


Figure 17. MAX22199 Input Surge Protection with TVS

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX22199ATJ+	-40°C to +125°C	32-TQFN
MAX22199ATJ+T	-40°C to +125°C	32-TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/21	Initial release	—

